Fermilab U.S. DEPARTMENT OF ENERGY | Office of Science

Mu2e II Trigger/TDAQ Summary

B. Echenard, G. Pezzullo

CalTech, Yale

for the Mu2e II Trigger Working group

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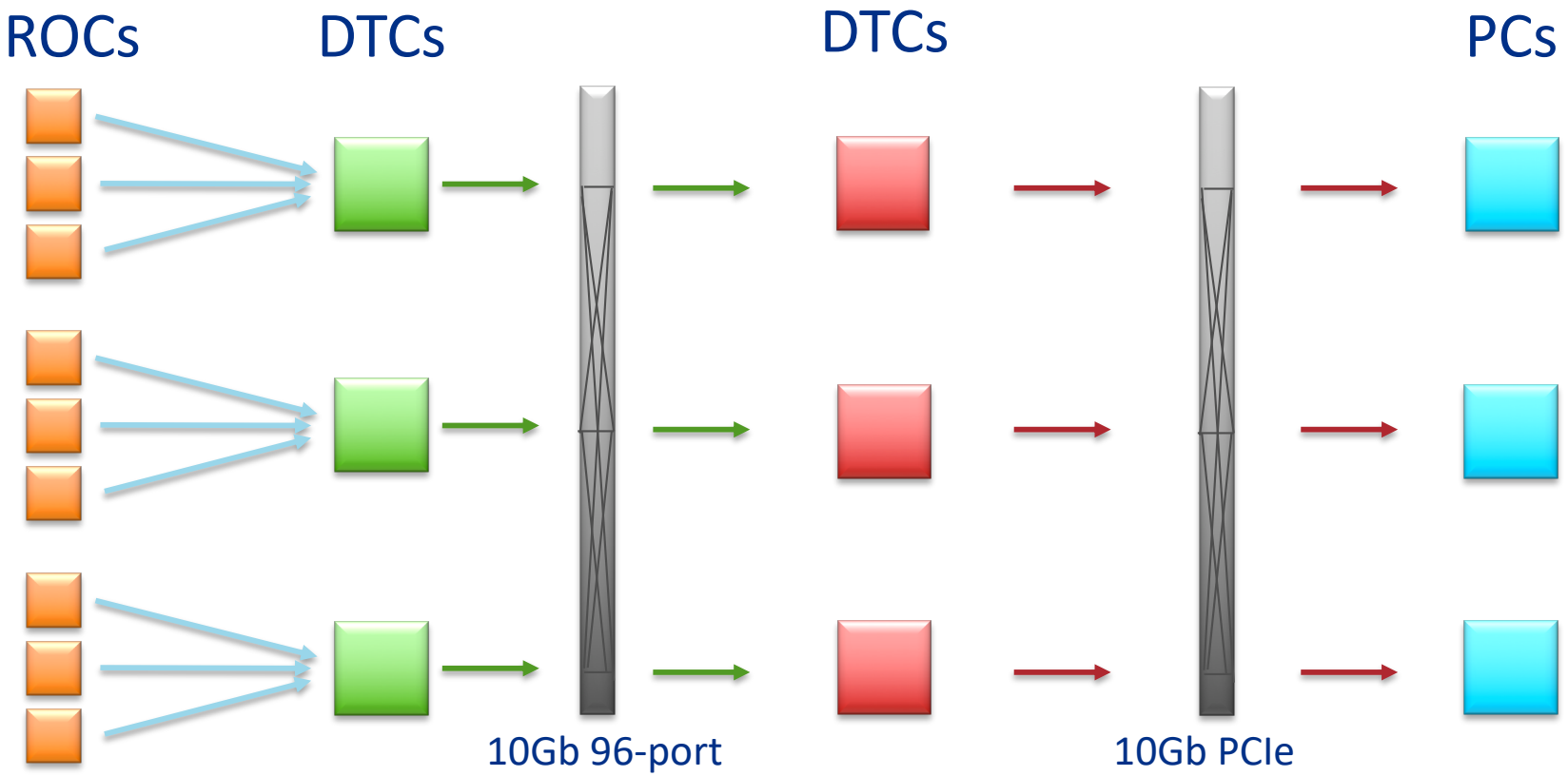
Mu2e II implications for TDAQ architecture

- **Larger detector occupancy & beam-duty cycle**
  - Larger bandwidth needed to handle expected data flux
    - x3-5 in the instantaneous rate, x3 duty cyle
  - Higher rejection needed
    - Guidance: no more than x2 in data storage 14 PB/y
      - we need a factor x5 in the rejection
  - Higher radiation delivered to the ROCs

- **PIP-II beam structure** with no phase shift in timing
  - Consider to lock system clock to 162.5 MHz accelerator clock IF ok with electronics
  - Reduced OFF Spill periods (to no OFF Spill time?) implies less advantage to large front-end buffers for streaming data

Generic Data Readout Applied to Mu2e-I



TDAQ architectures for Mu2e-II

- **Expand current Mu2e architecture (1 level trigger):**
  - assuming x2 gain in tech, extrapolation of Mu2e system requires x5 more hardware
  - larger DAQ room, power and cooling
  - 100 Gb switches (Vs 10 Gb of today system)
  - Will existing algorithm performance scale (now few ms/evt)?
    - With retuning?

- **2 level Trigger**
  - do some processing on FPGA and the remainder on software
    - Where are the boundaries?
    - can we make a L1 trigger decision at FPGA level?
    - Need to develop FPGA algorithms

TDAQ architectures for Mu2e-II (CRV)

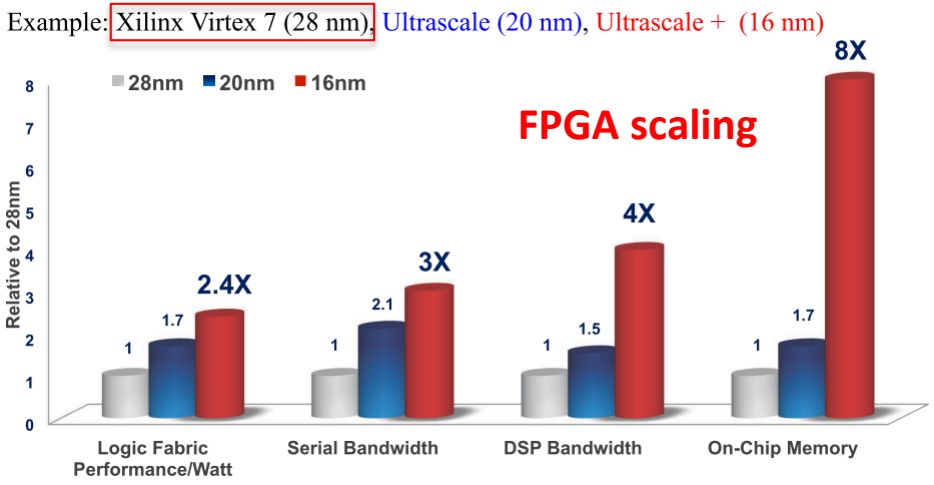
- Independent CRV trigger on FPGA
  - No significant OFF-spill period
  - How much Cosmic data do we need?
  - Develop dedicated CRV trigger?

FPGA considerations (1)

- High Level Synthesis (HLS) is now good enough to rival manual VHDL or Verilog algorithm development.
- Allows physicists to easily develop FPGA algorithms
  - development can take place now – hardware is not needed!
- CMS is heavily investing in HLS
  - hls4ml collaboration developing neural network tools using HLS

```
49    //sum up presamples
50    pedsum_type pedsum = 0;
51    for (int i = 0; i < NUM_PRESAMPLES; i++){
52        pedsum += adc[i];
53    }
54    //find average
55    adc_type pedestal = pedsum / NUM_PRESAMPLES;
56    adc_type peak = 0;
57    for (int i = START_SAMPLES; i < NUM_SAMPLES; i++){
58        if (adc[i] > peak){
59            peak = adc[i];
60        }
61        else{
62            break;
63        }
64    }
65
66    adc_type energy = peak - pedestal;
67    adc_type energy_max_adjusted = ((((energy_max_LSHIFT8 * gain_RSHIFT15) >> 9) *
68                                     inverse_ionization_energy_LSHIFT26) >> 10);
69    adc_type energy_min_adjusted = ((((energy_min_LSHIFT8 * gain_RSHIFT15) >> 9) *
70                                     inverse_ionization_energy_LSHIFT26) >> 10);
71    if (energy > energy_max_adjusted || energy < energy_min_adjusted){
72        failed_energy = 1;//failed
73    }
74    return ((failed_energy<<1) | failed_time);
```

HLS code developed for Mu2e



Current Mu2e timing architecture

Mu2e timing architecture

- Mu2e has chosen a stable 40 MHz clock (system clock) from Clock Fan-Out (CFO) module
  - Mu2e system clock is not locked to the Delivery Ring clock → experiment and beam are asynchronous

- CFO receives electrical signal associated with microbunches (DR turn marker), which is used to tell us…
  - Microbunch timing with precision ~1 ns
  - Timing within spill

See docdb-19095 for details

Mu2ell beam timing

First thoughts on TDAQ thoughts re: beam timing

- Given increase of duty cycle from 25% to 97%…
  - Pre-processing step with FPGA's? "Level-1+HLT" architecture?
  - When to collect cosmic rays?
  - When to perform calibrations?

- Given neither resonant extraction nor Delivery Ring…
  - Implications of smaller pulse-to-pulse variation? (no spill structure)
  - Work out new protocol to communicate "PIP-II beam to Mu2e" (i.e., replacement of DR turn marker)

- Given no phase shift of PIP-II RF…
  - Consider to lock Mu2e-II system clock to 162.5 MHz accelerator clock

- Given that PIP-II timing is based on pulses every 6.15 ns…
  - No action regarding structure within microbunch
  - Don't omit possibility to vary spacing between microbunches

VTRx

- We need rad hard optical link for Tracker and Calo ROCs
- Experiment ”standard” for data transmission between ROCs and DTCs is the VTRx from CERN
- For Mu2e II we can follow CMS development for the next generation of rad hard optical links
- Keep looking for other options as well

Summary / R&D projects

- Two possible architectures to investigate:
  - 1 level: “expanded” Mu2e TDAQ system
  - 2 levels: L1 Trigger + HLT

- Develop trigger algorithms for FPGA:
  - Needed to set requirements on the hardware

- Evaluate performance/costs of the proposed architectures

- Cosmic rays study for CRV trigger

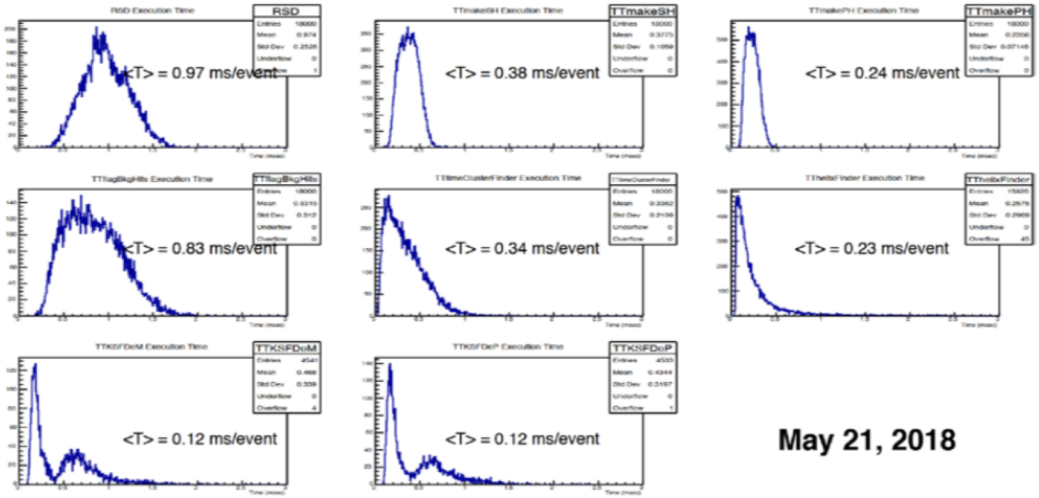
- Sim inputs for evaluating the expected doses in the ROCs

Backup slides

Mu2e expected Trigger performance

Triggers

Track Trigger Timing Status (triggerDev) *D. Brown*



May 21, 2018

- Total time = 3.2 (2.2) msec/event
- Reductions in makeSH, FlagBkgHits, Seed Fits

David Brown, LBNL 4 Trigger WS 27 June, 2018

+ combined track-calo cluster
+ additional triggers

Can still improve, but likely by a factor of a few.

S. diFalco

ECAL Trigger performances: processing time

1000 events on mu2ebuild01

TimeTracker printout (ms)	Min	Avg	Max
CaloClusterFast:CaloClusterFast	0.2	0.4	0.8
FilterEcalMVATrigger	0.008	0.047	2.6

100000 events on grid machines

TimeTracker printout (ms)	Avg
CaloClusterFast:CaloClusterFast	0.5
FilterEcalMVATrigger	0.06

The cpu time/event of ECAL itself is 60 μs!
Previous estimate (1 ms) was dominated by an update of event time offset used for debugging purposes

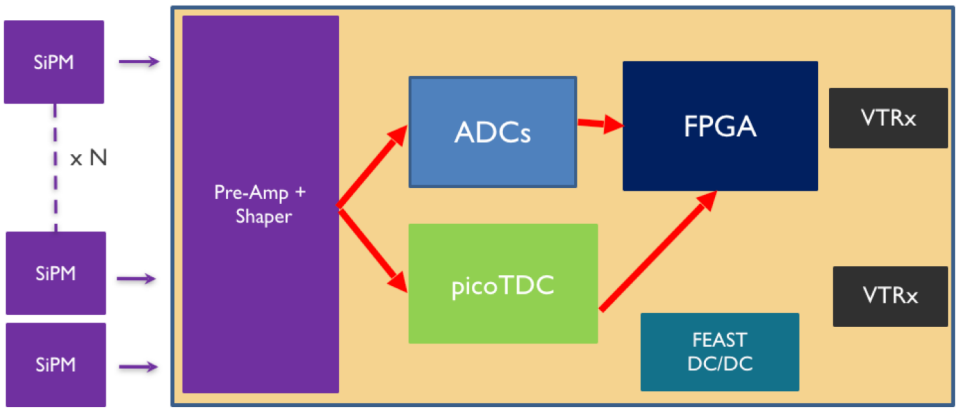
17

	Efficiency on Conversion electrons (CE) (t>700 ns)			
NORMALIZATION	CE hits* on ECAL virtual detectors (no requests on track)	Good quality tracks + CE virtual hit	Good quality tracks matching cluster with E>50 MeV + CE virtual hit	BKG rejection (t>500 ns)
Max eff	73% (±0.3)	86% (±0.4)	93% (±0.2)	120 (±4)
Max rej	70% (±0.3)	83% (±0.3)	90% (±0.3)	300 (±15)

*hit associated to an electron with p>90 MeV/c

Possible ADvanceD-DIRAC

- Instead of sampling the waveform we want to use TDCs for precise time reconstruction
- Rad hard ADC @ 50 MHz for charge reconstruction?
- The **PolarFire** FPGA is supposed to be sufficiently rad hard
- **VTRx** optical transivers
- The board will include also the PreAmp+shaper (thanks to the SiPM high gain)
  - ➡TID reduction & neutron flux by a facto of ~ 10
  - ➡simplified cooling system



Credits:
F. Spinella (INFN Pisa)

Future Tracker ROC?

- We don't know yet the Mu2e II tracker design!
- **Assuming** to use the same technology, we need smaller straws to handle the larger hit rate, thus more channels

  ➡ "bigger" DRAC boards?

  ➡ larger bandwidth required (?)

- BUT, scaling to x10 the expected radiation levels makes majority of the components not well suited

  ➡ R&D to find commercial rad tolerant components

  ➡ possible mitigation strategies in the experimental setup?

  - improved shielding design
  - changes in the beam line