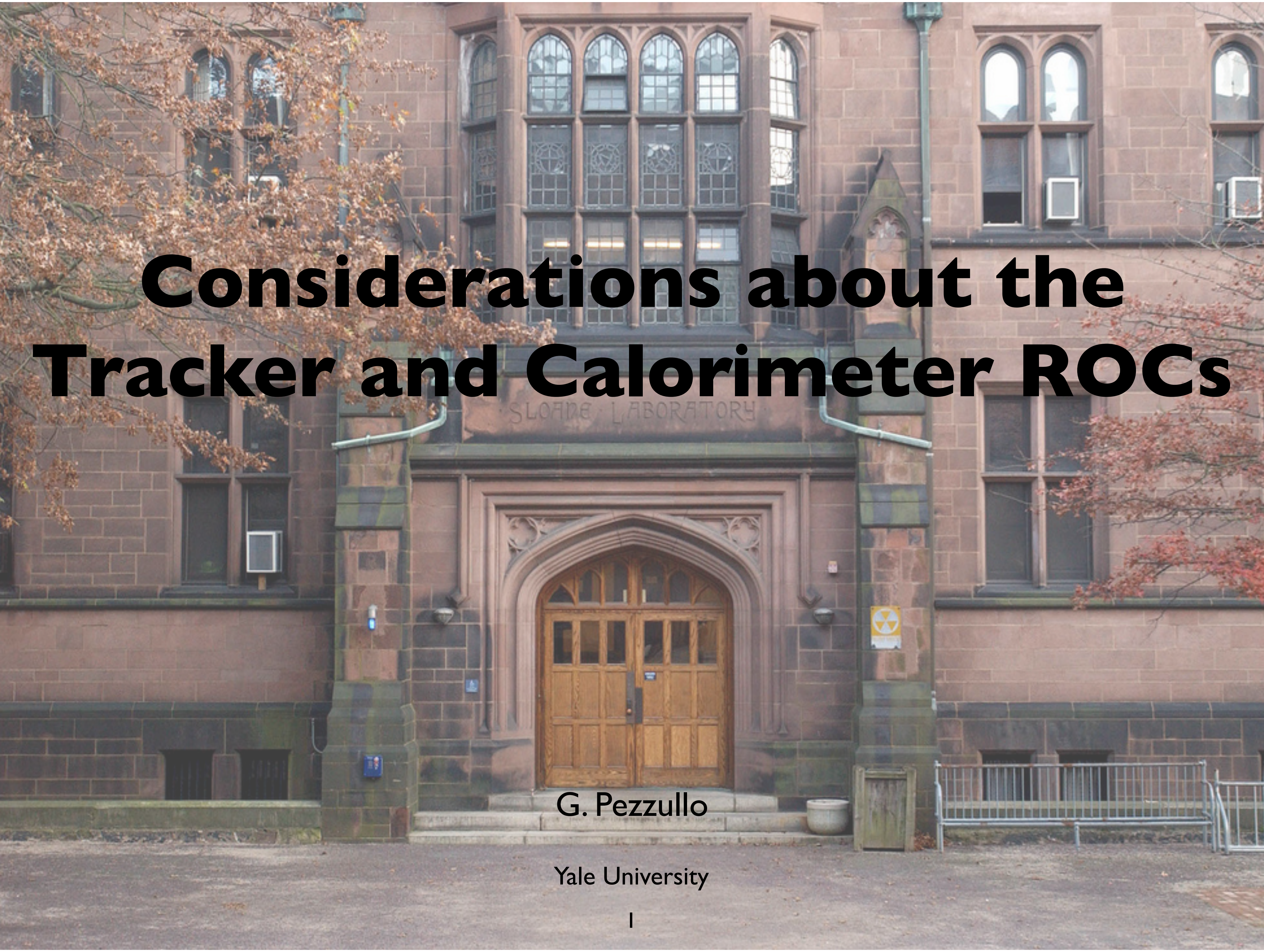

Considerations about the Tracker and Calorimeter ROCs

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Yale University

Outline

- Challenges
- Expected radiation level in Mu2e
- Possible design evolutions and R&D
- Discussion

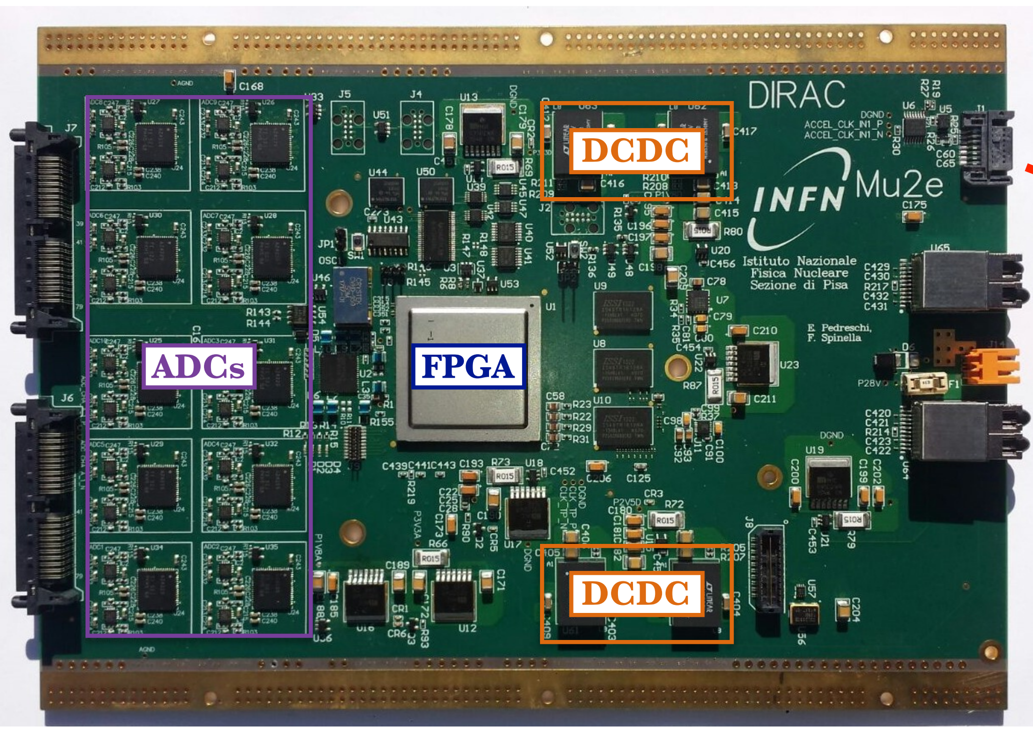
Challenges

- The use of **PIP-II beam** has 2 major consequences:
  - instantaneous rate increases by x3-5 (larger duty factor)
  - x10 improvement in the stopped muon rate

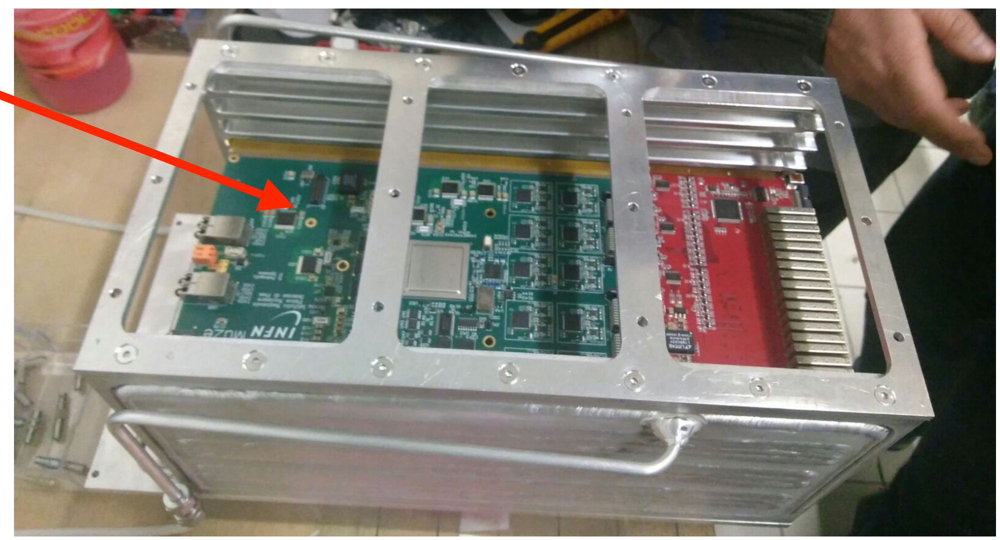
- These result in:
  - x10 (?) ionizing and non-ionizing dose to the electronics
  - larger hit rate to sustain

Calorimeter ROC

- Outer region of the calorimeter houses the DIgitizer ReAdout Controller (DIRAC)
- Digitize inputs (20ch/board) @ 200 MHz + zero suppression



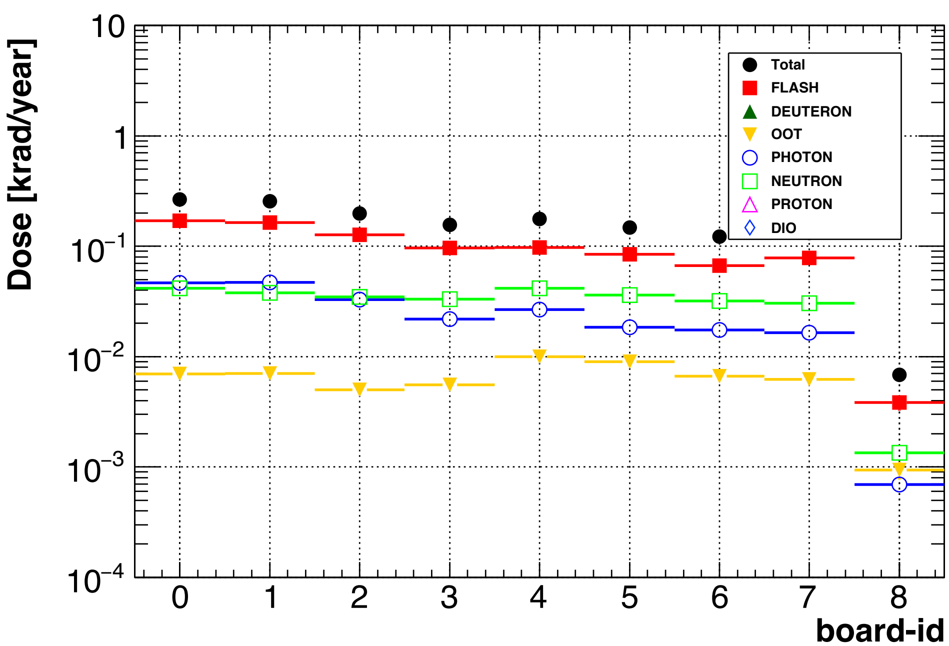
Crates



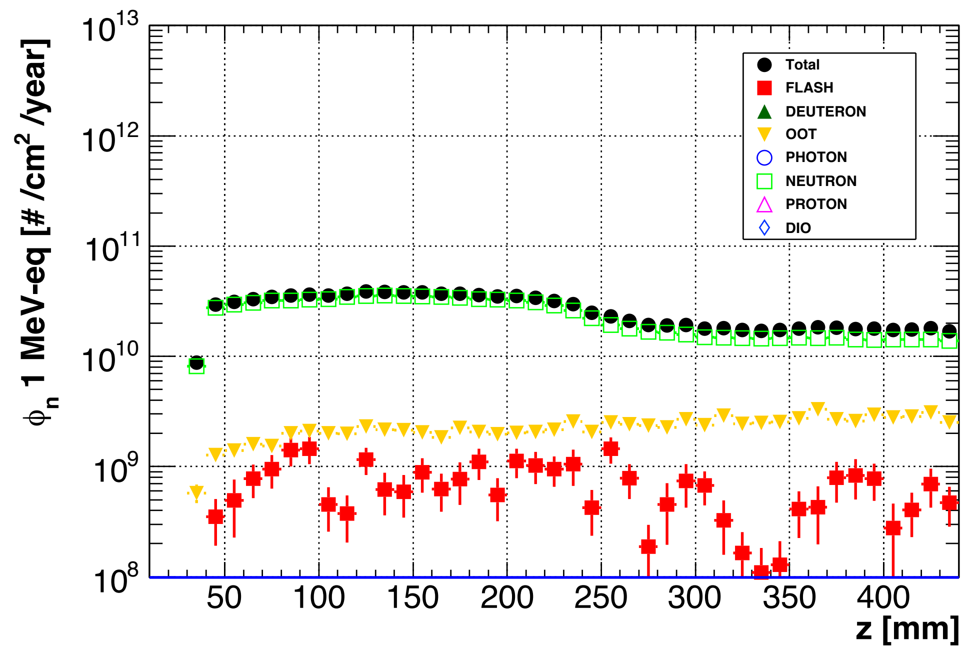
Calorimeter DIRAC Dose

- Detailed Monte Carlo simulations with MARS and GEANT4
- peak dose ~ 0.3 krad/year
- Neutron flux up to 4e10 $n_{1MeVeq}/cm^2/year$

Total Ionizing Dose (TID)



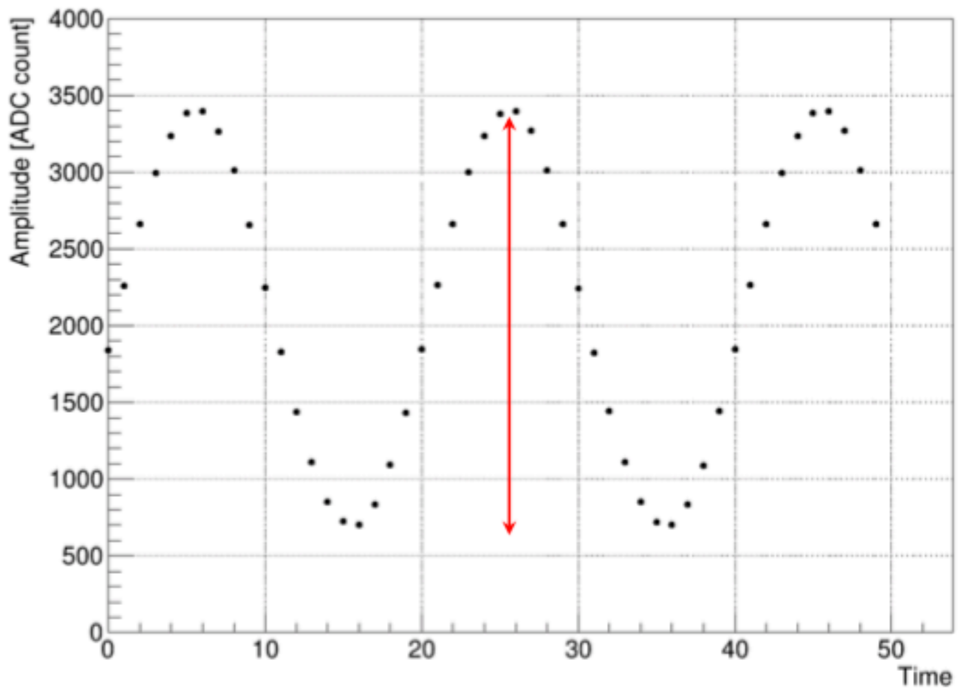
Non Ionizing Energy Loss (NIEL)



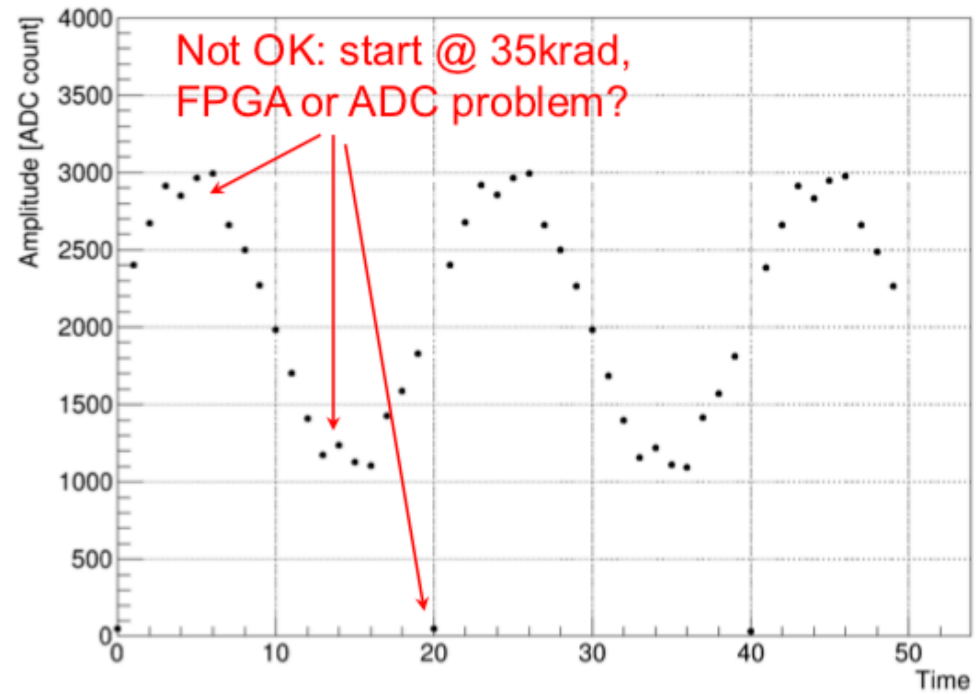
Calorimeter rad tests

- Prototype tested at Casaccia (ENEA facility in Italy) up to ~ 40 krad
- Functionality losses after 35 krad

Before

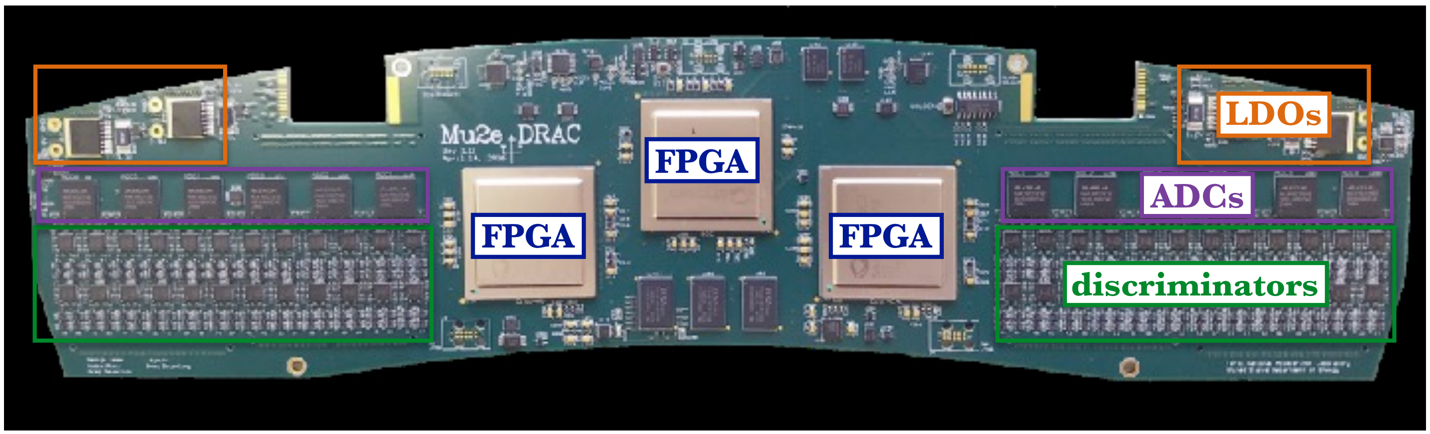


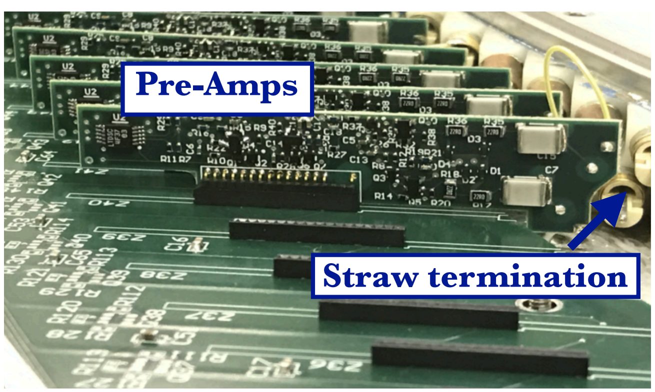
After

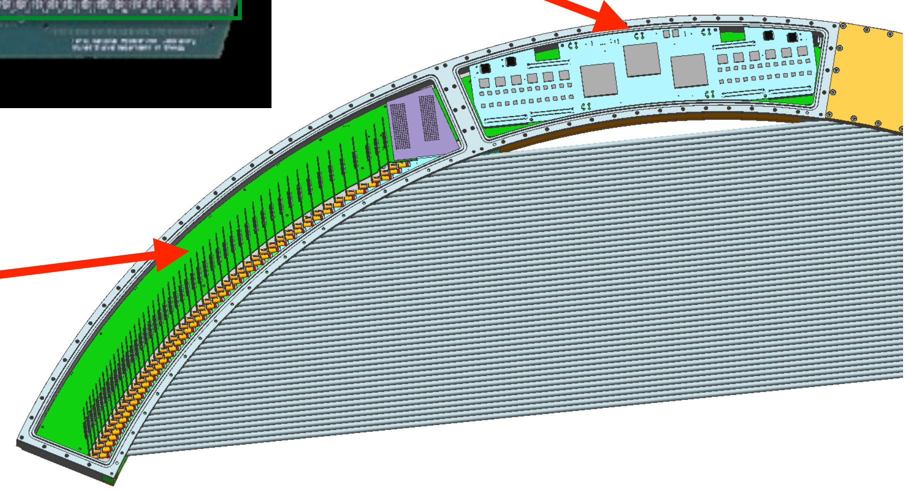


Tracker ROC

- Outer part of the panel houses the FEE and Digitizer Readout & Assembler Controller (DRAC)
- High hit rate sustainability: 15 kHz/cm^2



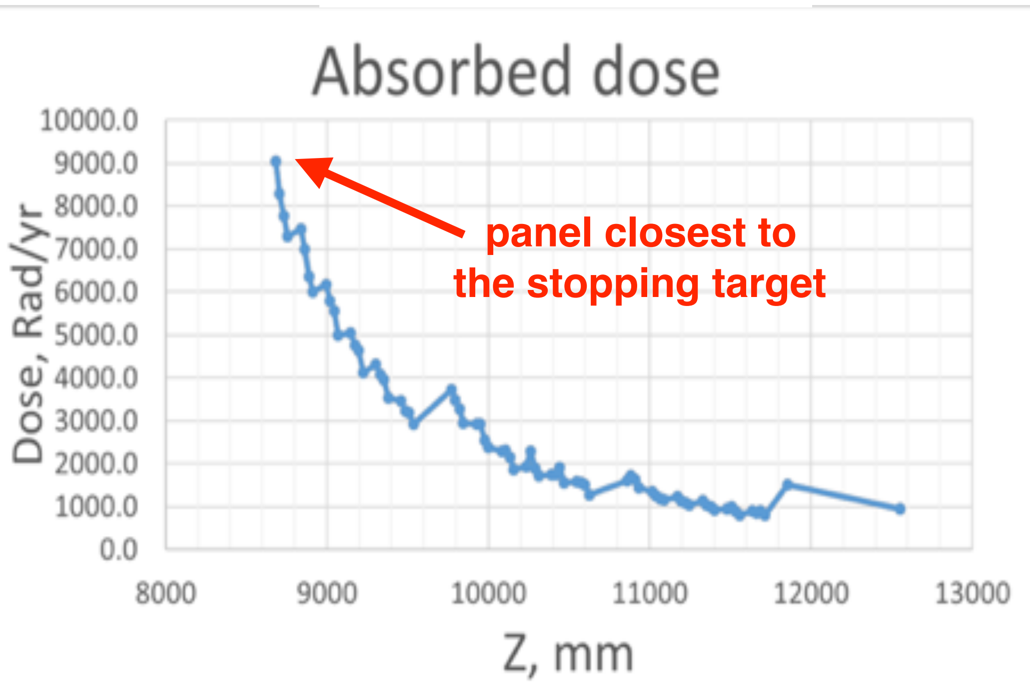




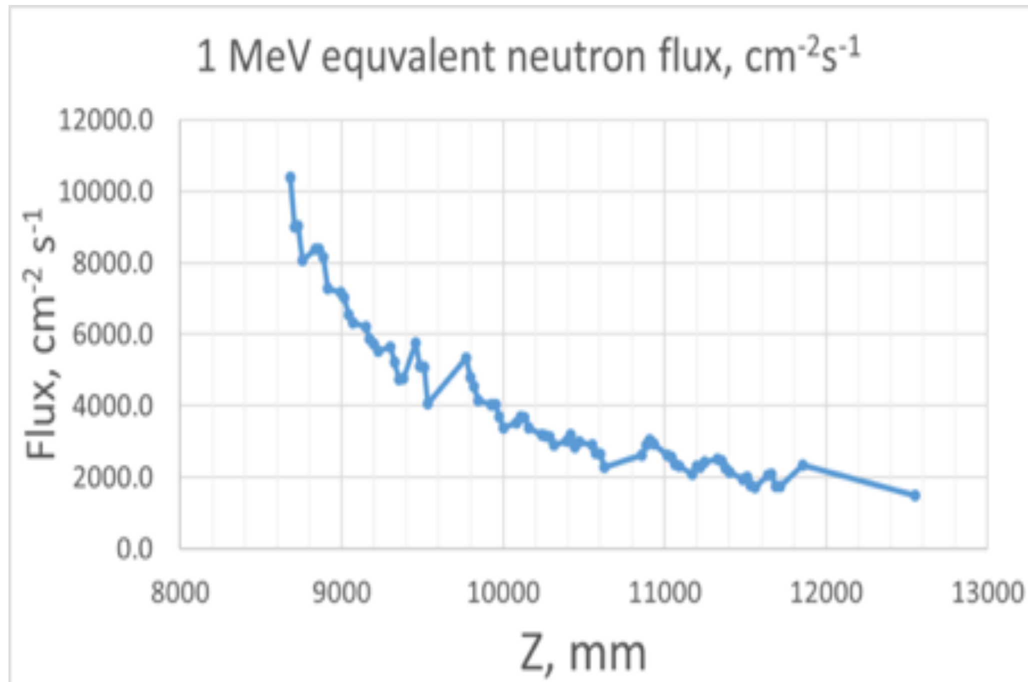
Tracker Dose

- Detailed Monte Carlo simulations with MARS and GEANT4
- peak dose ~ 9 krad/year in the first plane
- Neutron flux up to 2e11 $n_{1MeVeq}/cm^2/year$

Total Ionizing Dose (TID)

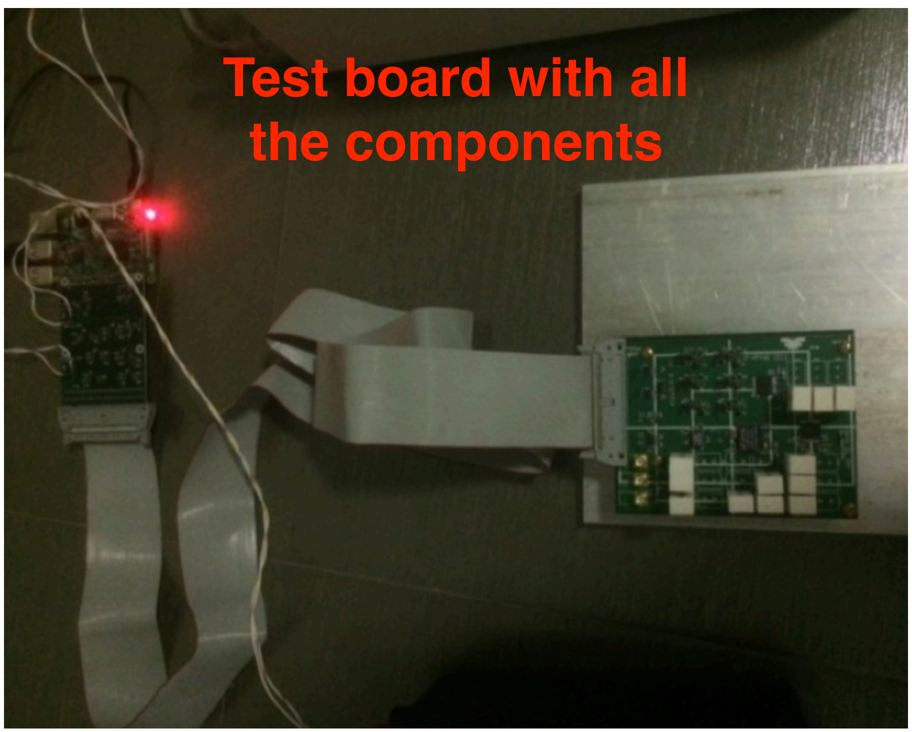


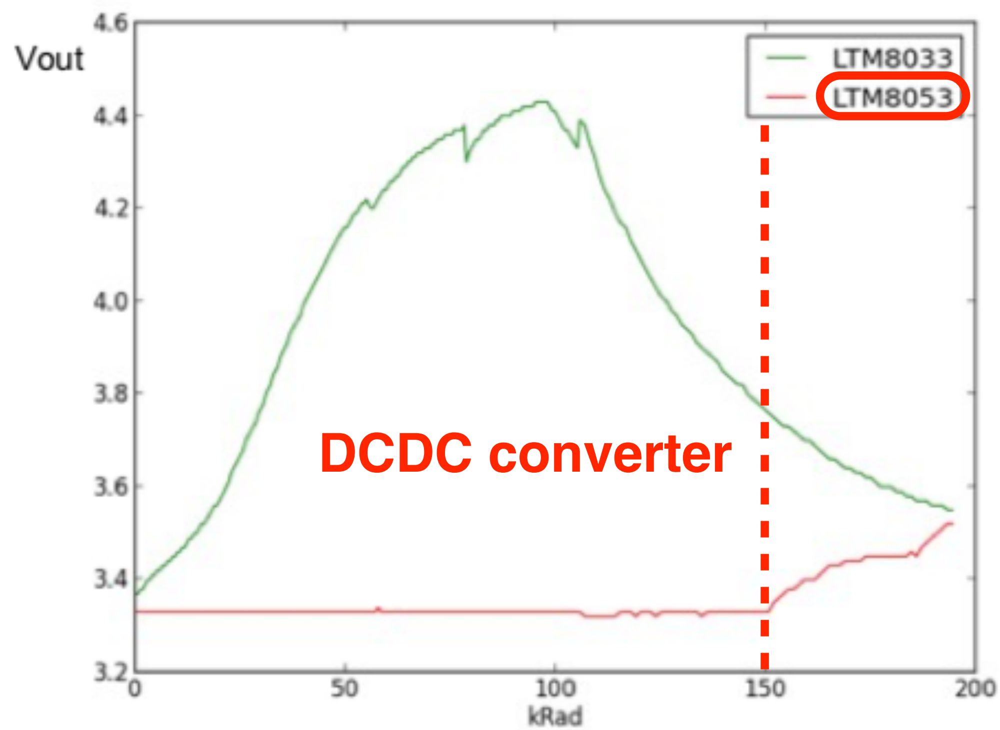
Non Ionizing Energy Loss (NIEL)



Tracker radiation tests

- PolarFire FPGA from Microsemi (tested up to 500 krad)
- rad hard Optical transceiver VTRx from CERN (tested up to 1 Mrad)
- tests campaign to qualify other major components:
  - ✓ TID tests @ local radiotherapy clinic up to 200 krad
  - ✓ NIEL tests @ UC Davis McClellan reactor up tp 2e14 n_{1MeVeq}/cm^2





Future Calorimeter ROC

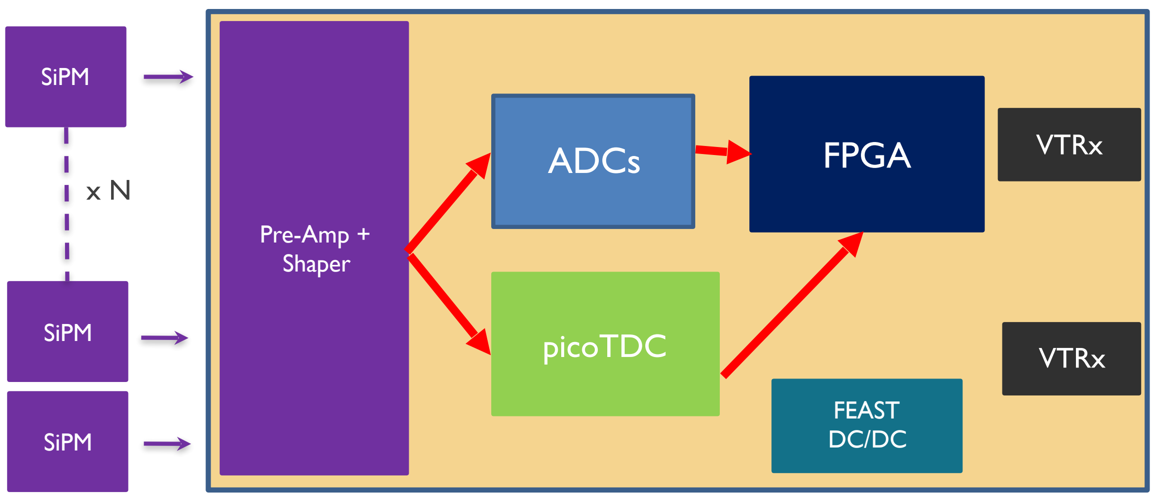
- **Assuming** similar detector design (aka @ of channels), the main issue is represented bu the increase in the occupancy
- Radiation is also a concern, but not as for the Tracker
- In the next slides we propose a possible design that **assumes** a calorimeter technology (crystal+FEE) capable to provide short signals (~20-30 ns) compared to the current one (~ 120 ns)

➡ not so crazy if BaF_2 is going to be adopted!

➡ still… BaF_2 needs a specie R&D for adequate photosensor (not purpose of this talk)

Possible ADvanceD-DIRAC

- Instead of sampling the waveform we want to use TDCs for precise time reconstruction
- Rad hard ADC @ 50 MHz for charge reconstruction?
- The **PolarFire** FPGA is supposed to be sufficiently rad hard
- **VTRx** optical transivers
- The board will include also the PreAmp+shaper (thanks to the SiPM high gain)
  - ➡TID reduction & neutron flux by a facto of ~ 10
  - ➡simplified cooling system



Credits:
F. Spinella (INFN Pisa)

FEAST DC-DC converter

- The current best candidate is the **FEAST** DC/DC converter developed @ CERN:

Features

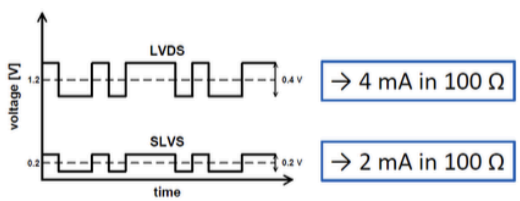
- Input voltage range 5 to 12V
- Continuous 4A load capability
- Integrated Power N-channel MOSFETs
- Adjustable switching frequency 1-3MHz
- Synchronous Buck topology with continuous mode operation
- High bandwidth feedback loop (150KHz) for good transient performance
- Over-Current protection
- Under-voltage lockup
- Over-Temperature protection
- Power Good output
- Enable Input
- Selectable Power Transistor size (5/5th or 2/5th) for improved efficiency at small loads (<600mA)
- Radiation tolerant: TID up to >200Mrad(Si), displacement damage up to $5\text{-}8 \cdot 10^{14}$n/cm^2 (1MeV-equivalent), no destructive SEEs up to >30MeVcm^{2}mg^{-1}, SEFI (reset) cross-section in a 230MeV proton beam ~ $2.8 \cdot 10^{-13}$ cm^2

picoTDC

- The current best candidate is the **picoTDC** under development @ CERN

Interfaces

- Power: 1.2v, ~1.0W (64ch, 3ps),
  ~0.5W (64ch, 12ps)
  ~0.3W (32ch, 12ps)
- Hits: Differential SLVS (LVDS "compatible")
- Time reference: 40MHz SLVS
  - Low jitter reference critical for high time resolution
- Trigger/BX-reset/reset: Sync Yes/No, Encoded protocol
- Control/monitoring: GBT E-link and I2C
- Readout SLVS: 4 readout ports of 1-8 signals
  - To be interfaced with GBTX or FPGA
- Packaging: ~300 FPBGA



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Readout

- 1 or 4 readout ports
  - 4 ports: High rate applications (e.g. non triggered)
    16 TDC channels per port
  - 1 port: Low-medium rate
    64 channels (or 32channels in 32 channel mode)
- Readout data: 32bit words
  - Headers, trailers, TDC data, status, etc.
- Readout ports interface
  - Byte wise:
    - 40, 80, 160, 320 MHz
  - Serial:
    - 8B/10B or 64B/66B encoding
    - Low speed: 40, 80, 160, 320 Mbits/s
    - High speed: 1.28 Gbits/s
- TDC readout bandwidth:
  - Max:
    320MHZ x 8 x 4 = 10Gbits/s (~4Mhits/s per channel without triggering)
    1.28Gbits/s x 4 = 5Gbits/s
  - Min: 1 x 40Mbits/s= 40Mbits/s

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Future Tracker ROC?

- We don't know yet the Mu2e II tracker design!
- **Assuming** to use the same technology, we need smaller straws to handle the larger hit rate, thus more channels
  - ➡ "bigger" DRAC boards?
  - ➡ larger bandwidth required (?)
- BUT, scaling to x10 the expected radiation levels makes majority of the components not well suited
  - ➡ R&D to find commercial rad tolerant components
  - ➡ possible mitigation strategies in the experimental setup?
    - improved shielding design
    - changes in the beam line

Summary

Extrapolating the current detector design in the Mu2e II case:

- The calorimeter ADD-DIRAC would allow to have a negligible impact in the TDAQ load/architecture
- For the Tracker DRAC life could not be as simple (lot of rad!)
- R&D for more rad-hard components might be necessary