Status of front end electronics

Cayetano Santos - On behalf of the IN2P3 group

30 August 2018

APC - Astroparticule et Cosmologie

Current Status

Electrical test OK

All reference voltage levels (2.5 V. Vadj, 3.3 V., etc.) OK

IO spare signals OK

Reference 1.2 V. and - 0.4 V. levels OK.

Comparators and level shifters OK

All S4AM/FMC interface signals OK

Full pinout validated - No surprises there

Issue with 100 Ohms adaptation seems solved - measured, to be confirmed by Bittware

No Jtag available: minor issue, annoying for the developer ...

Firmware: CatiROC controller IP

Validated by experience with few different hardware (slow control, data capture, etc.)

Online under GPL3 at http://bit.ly/2JPJFOa

Firmware: ADC

IPNL example template project running - all setup checked

Under adaptation from 8x8 ADCs to 1x16 ADC - Same component

Difficulties

Firmware upgrade

When mezzanine present, JTAG chain is lost ...

When mezzanine present, FINE uCLinux is lost ...

... so unable to upgrade firmware whith mezzanine

Slow, risky and dangerous.

Simulation

ModelSIM VHDL simulator not available (free version slow)

Use of alternative VHDL simulator, option ?

P0 / P1

Sync of several boards goes throught back plane

P1 taken by clock distribution

P0 only available to the FINe

Opt. 1: slow control through FINe and Stratix IV, how ? data readout using 10 Gbe

Opt. 2: slow control and data readout using 10 Gbe

Still to do: firmware/hardware

Single card mode

Make it work at 1 Gps

Make it work at 10 Gbps

10 Gbps Infrastructure ?

Tune hardware: fix low pass filter bandwidth, etc.

Multi card mode

Check viability of current architecture (S4AM hardware modification, etc.)

Firmware upgrade to multi card

Validate hardware (trigger propagation, etc.)

Still to do: software

Current

Porting of LabView into ... something else; gui ?

Validating code with current functionality

Decoding data on disk and displaying it

Next

Adapting to 1 ADC / 16 channels data format

Validating with new firmware / decoding and displaying

Decoding of CatiROC config file into binary data (code porting from matlab)

Readout of CatiROC binary data and compare

Slow control for ancillary functionality

Multi card mode

Acq

Decouple acq and slow control

Merge acq into main DAQ

1 Gbps / 10 Gbps modes

Conclusion

A lot still to do

Basic hardware almost validated: validate performances (refer to Antonio's talk)

Firmware still under development

DAQ support by IPNL / Slow Control at APC-LAPP

CatiROC Proved, tested and characterized on different projets

uTCA Standard rather time demanding: too many tricks to know ...

Existing example code running + proved firmware IP ...

... but reduced manpower