Commercial Detector Readout Hardware

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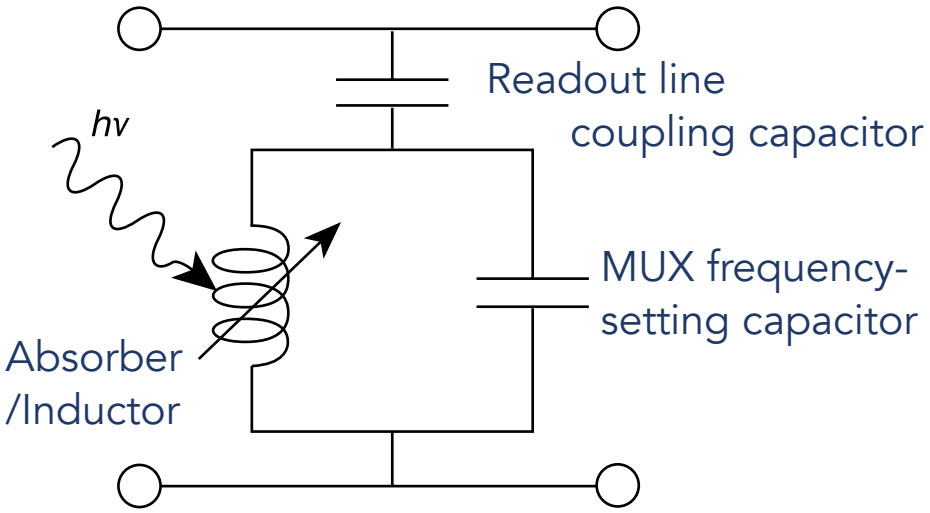
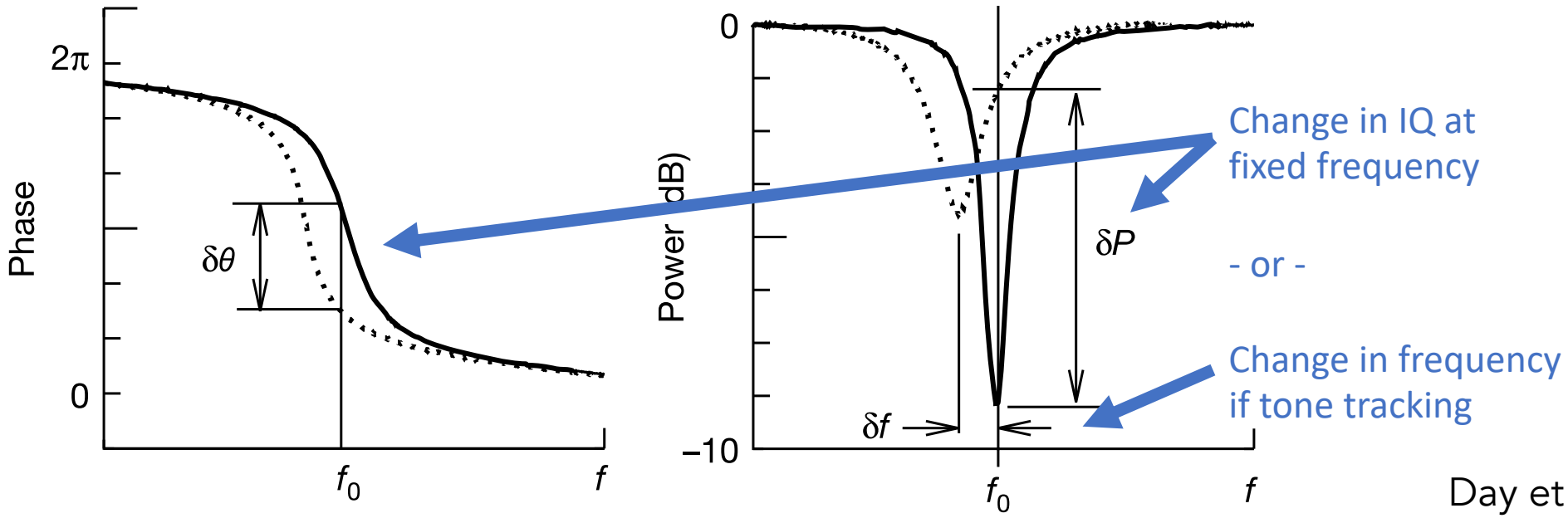
Overview

- RF readout applications
- FFT-based algorithm
- CORDIC-based algorithm
- RFSoC Hardware
- Integrated Analog IF Board

KID Concept

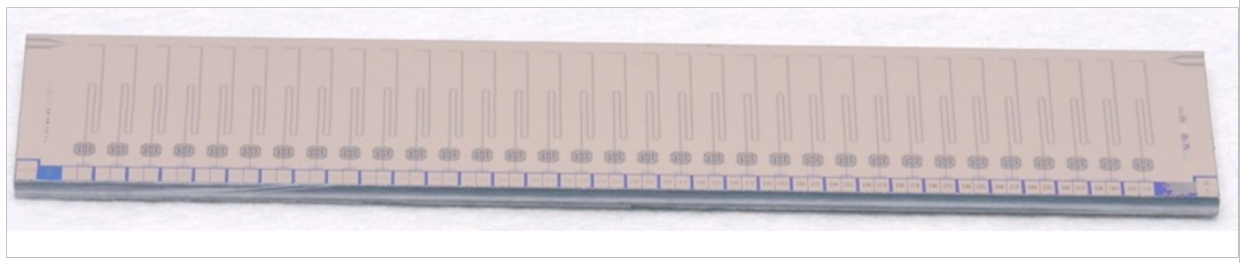
- Incoming mmwave light breaks Cooper pairs
- Change in Cooper pair density changes kinetic inductance
- Resulting frequency shift is monitored from outside the cryostat

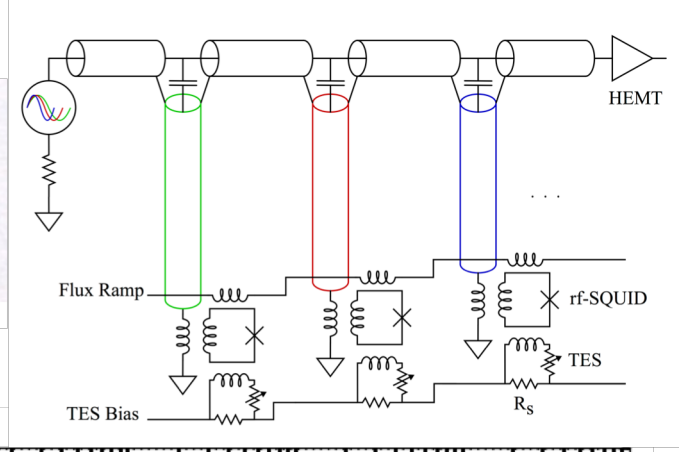




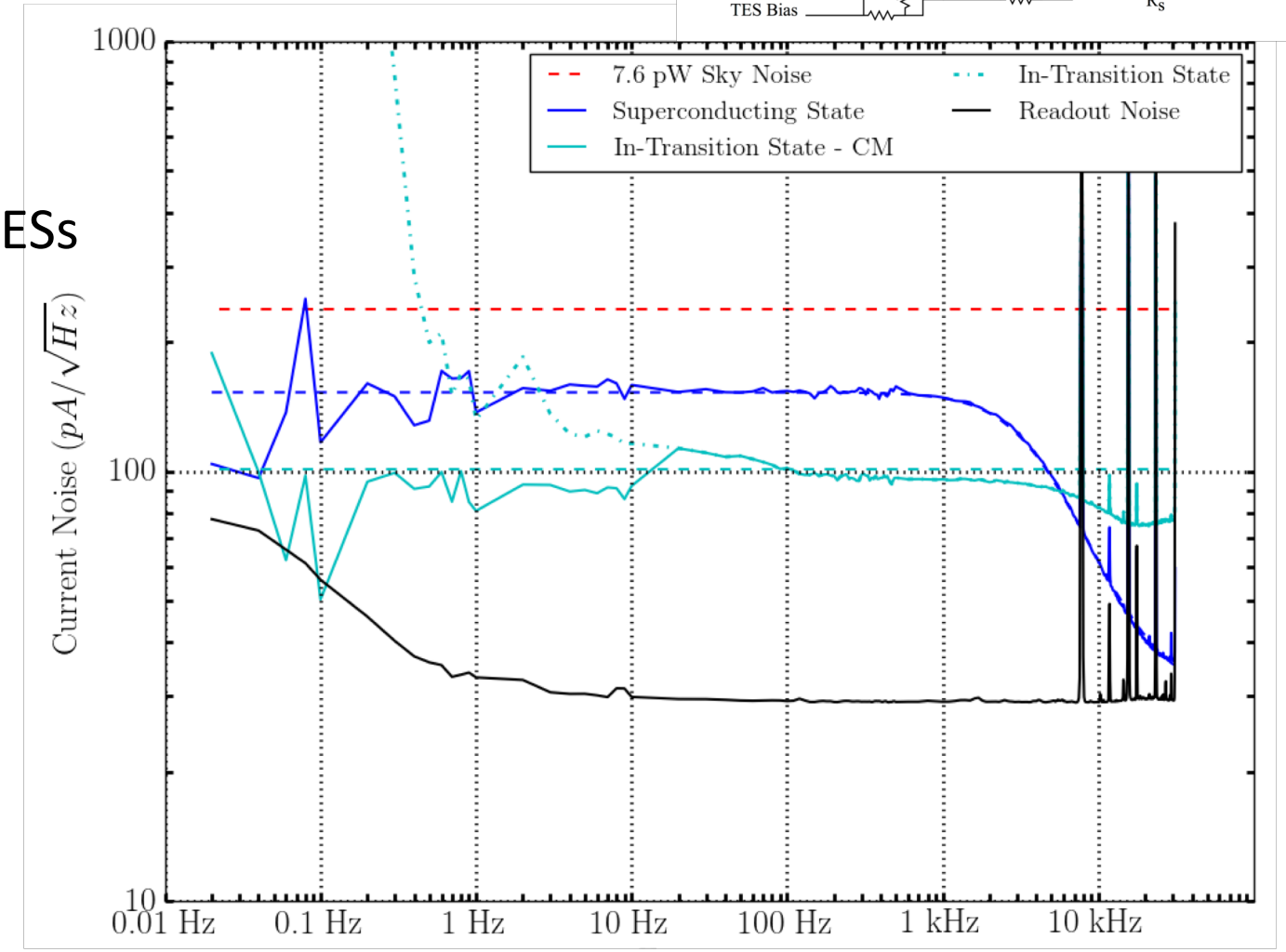
Day et al. 2003

uMUX Readout





- "Best of both worlds"
  - High multiplexing factor of KIDs
  - High science+technical heritage of TESs
- Applications in mm-wave, FIR, X-ray, …
- See other talks in this session and conference



Dober et al. astro-ph/1710.04326

Anatomy of a BLAST-TNG readout module

CASPER
ROACH2 Board

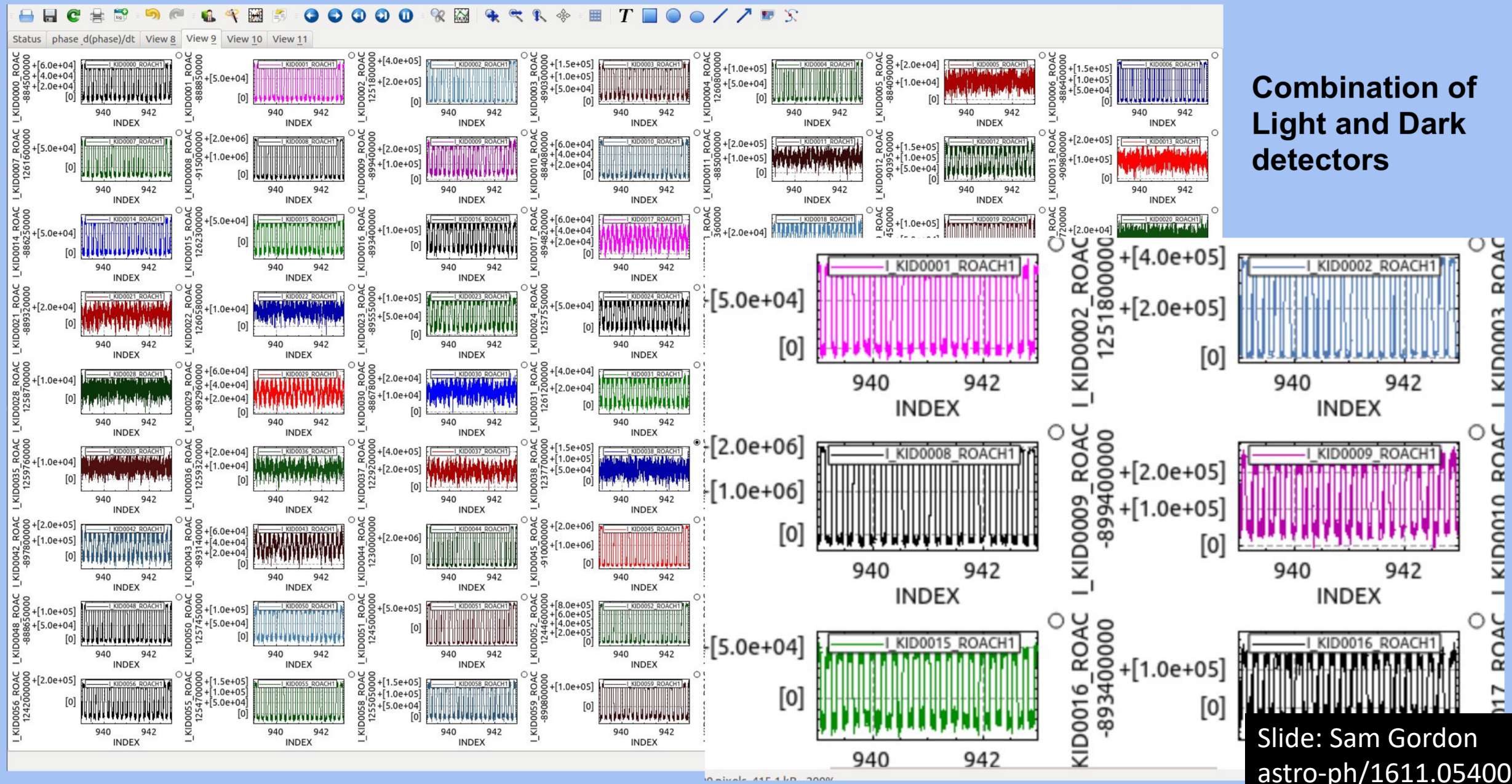
Techne
Instruments
MUSIC
DAC/ADC Board

Front end RF
electronics

Power consumption per
module is ~85 W

Slide: Sam Gordon
astro-ph/1611.05400

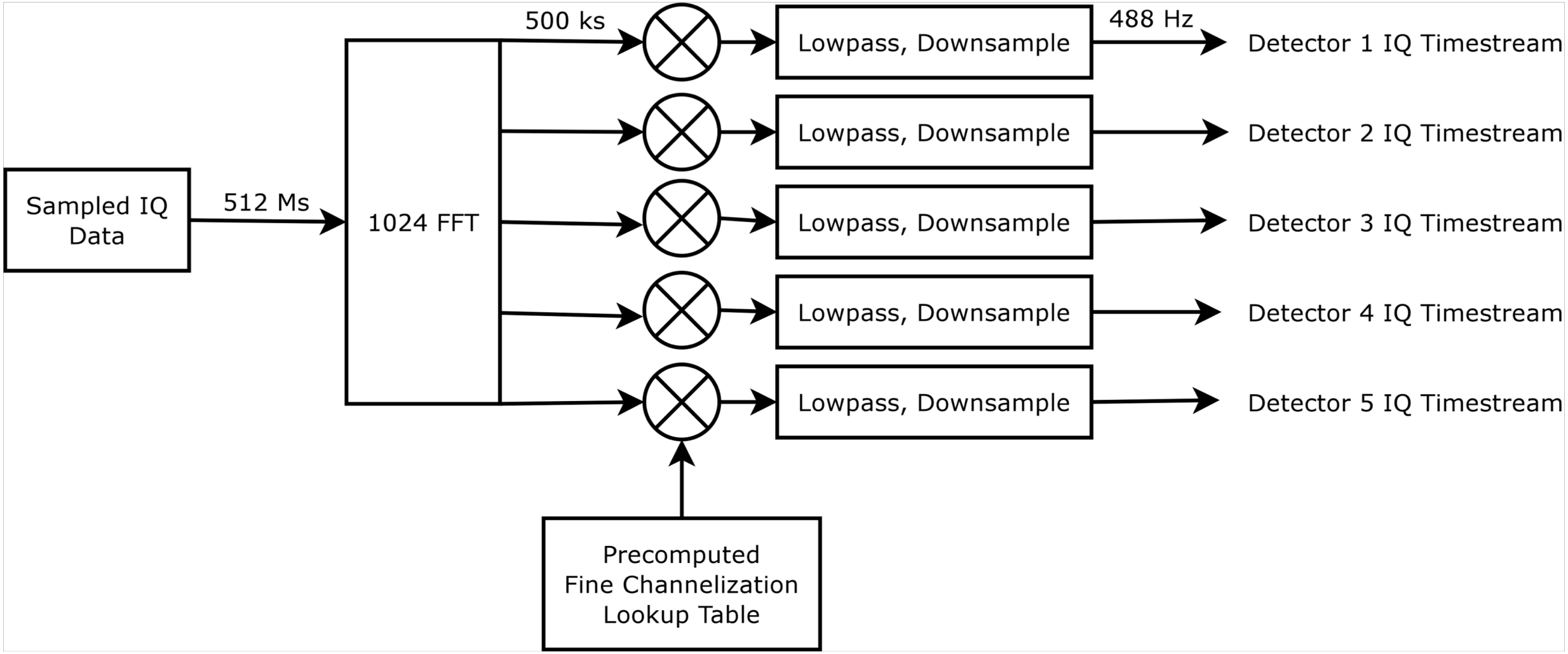
BLAST-TNG 250μm Array: LN2 Chop, UPenn, Feb 2017



Combination of Light and Dark detectors

Slide: Sam Gordon
astro-ph/1611.05400

BLAST-TNG Readout Algorithm



Advantages/Disadvantages

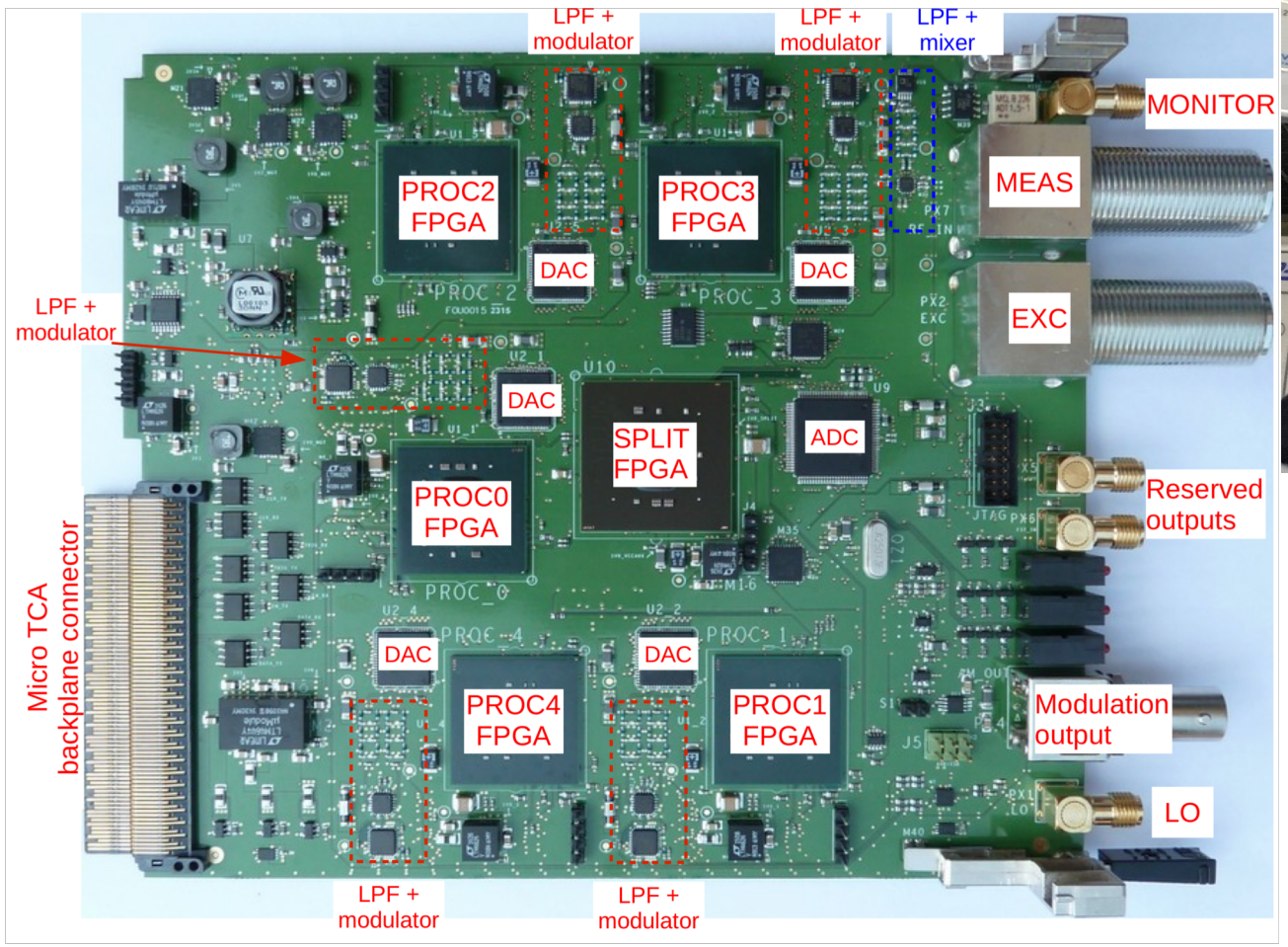
- Uses FFT
- Precomputes tones and efficiently reads from RAM
- No control loop issues
- Soon to have high TRL from successful (!) balloon flight

- Tones precomputed in the CPU and loaded into RAM
  - Can’t naturally track
  - Loses lock if resonator moves more than a linewidth

- Further work needed to study if computing tones on the FPGA could enable tone tracking yet remain efficient

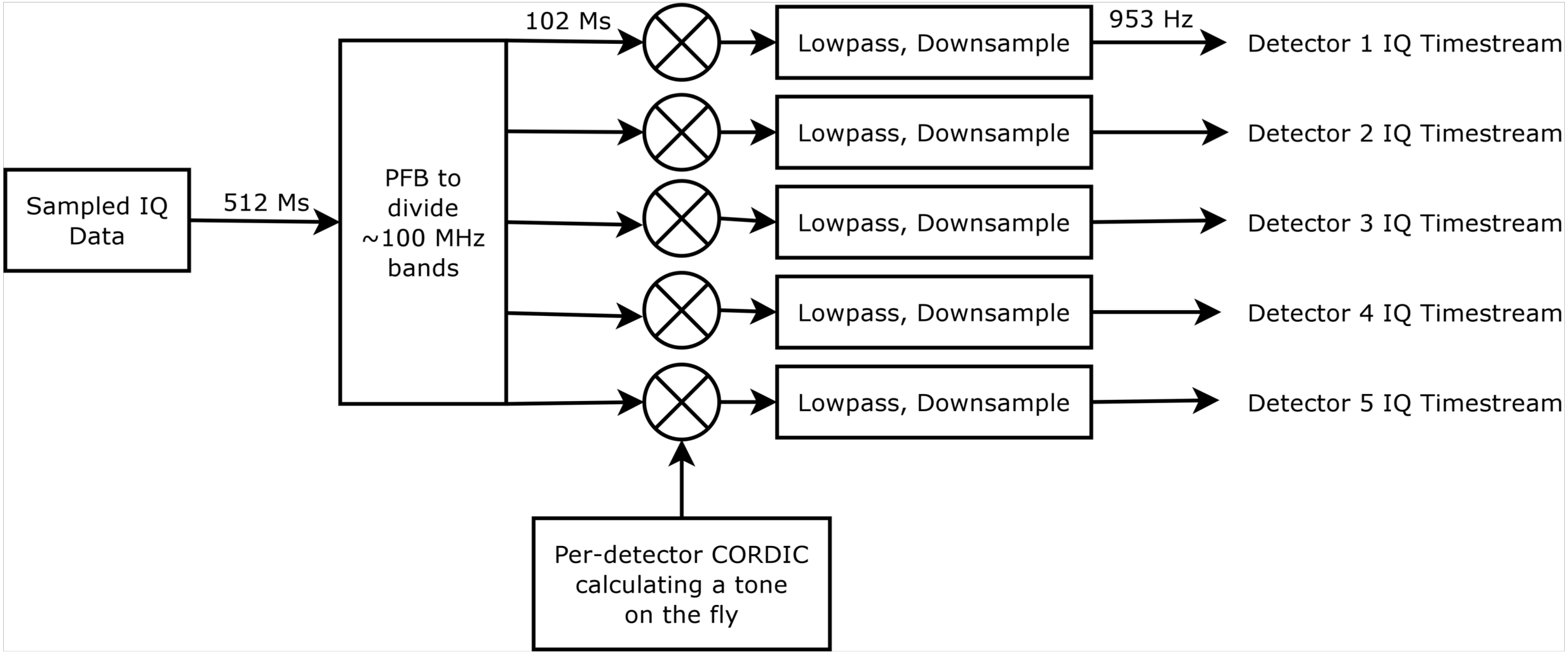
NIKA2 Readout Hardware

astro-ph/1602.01288



(My tourism photos from a visit to NIKA2 on the IRAM 30m)

NIKA2 Readout Algorithm



Advantages/Disadvantages

- Uses modulation to effectively have two tones on each resonator
  - Measures Q and f0 for responsivity monitoring
  - Almost already tone tracking
- Conceptually similar to analog homodyne
  - “Simple” algorithm
- Currently has high TRL from successful deployment on IRAM30

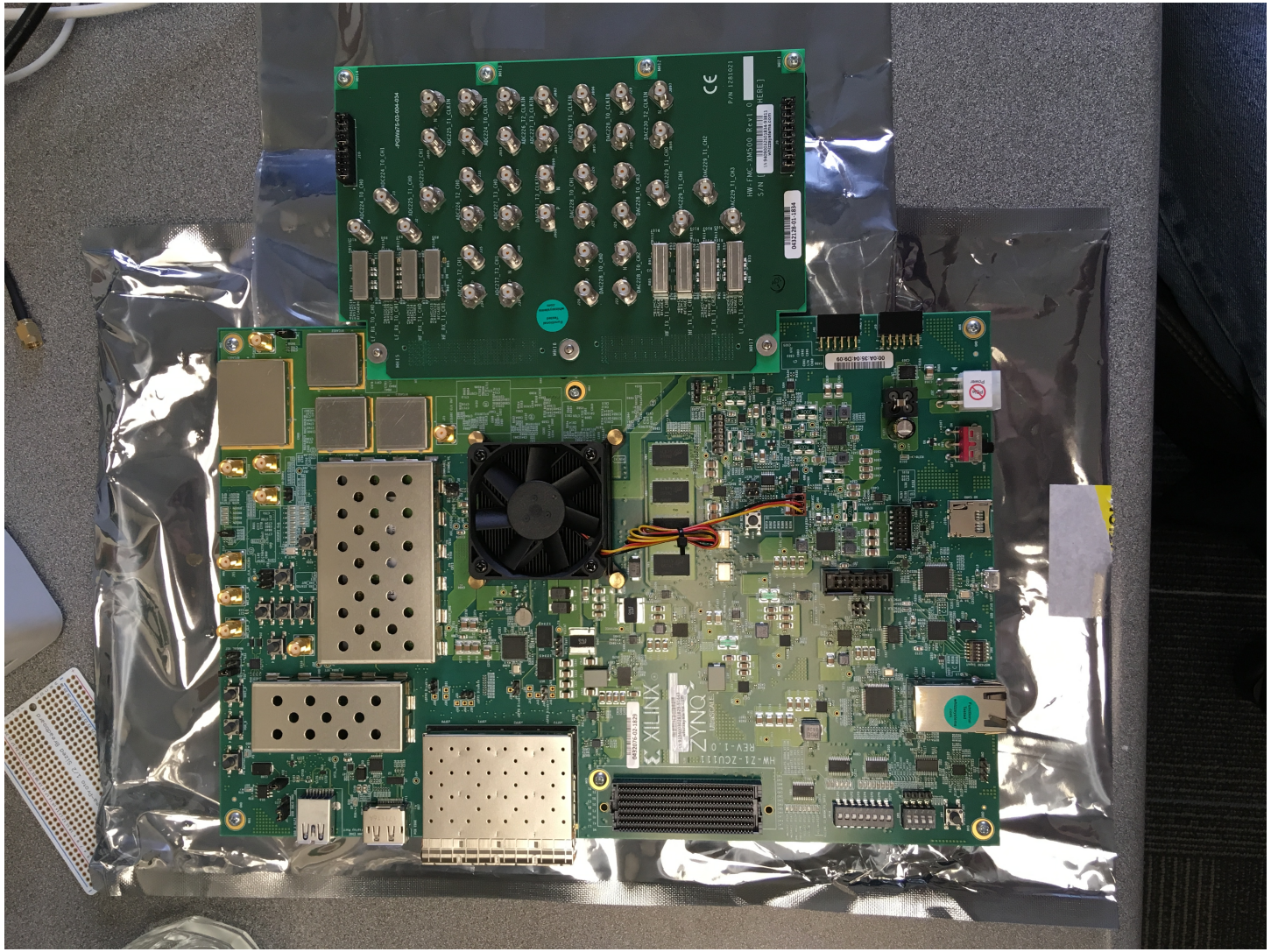
- CORDIC takes a lot of FPGA compute
  - (SMuRF algorithm has some elements in common?)

- Further work needed to study if the algorithm can be made more efficient on the FPGA with an FFT

Xilinx RFSoC Hardware

- RFSoC Chip =
  CPU + FPGA + DAC/ADC
- Board has that chip,
  lots of useful interfaces,
  and SMA connectors for RF
- 8x 4GSPS 12-bit ADCs
- 8x 6.4GSPS 14-bit DACs
- Uses 25 W (!)

- Photo is from my desk,
  WISCA group has experience
  with earlier version of board



Click to Enlarge

Zynq UltraScale+ RFSoC ZCU111 Evaluation Kit

Price: $8,995
Part Number: EK-U1-ZCU111-G
Lead Time: 8 weeks
Device Support: Zynq UltraScale+ RFSoC

XILINX.

Buy Online

Contact Sales

Naive Algorithm Scaling

- A lot of different things go into “resource use” on FPGAs, but here let’s naively consider just the DSP slice count

- NIKA2 has 5x Kintex-7 FPGAs per 400 detectors
  - Algorithm uses 166 DSP slices per FPGA
  - Scaling to the 4,272 DSP slices on the RFSoC yields **2,059 detectors**

- ROACH2 used in BLAST-TNG has a Virtex-6 per 512 detectors
  - Algorithm uses 105 DSP slices on the FPGA
  - Scaling to the 4,272 DSP slides on the RFSoC yields **20,831 detectors**

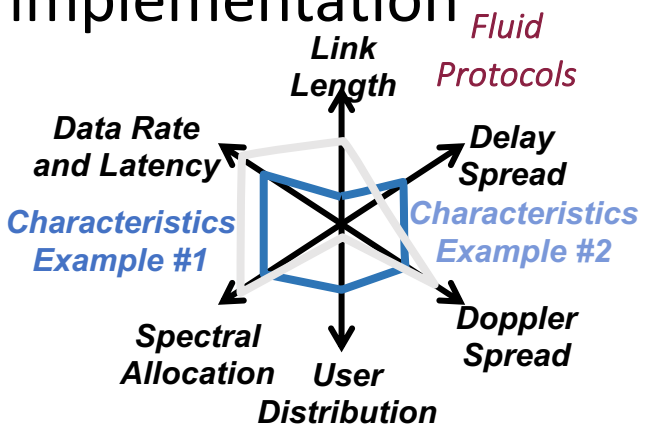
Tone-Tracking Algorithm Development

- Develop interfaces with Vivado to get configuration settings in and data out on a sensible UDP frame over ethernet
- Develop a CORDIC-based non-tracking algorithm
- Develop a FFT-based non-tracking algorithm
- Simulate if a combined FFT/CORDIC method could enable tracking of even more than the naive ~2000 detectors from CORDIC alone
- Develop the optimal tracking algorithm
- Open-source all of the above

ASU's WISCA Center

Wireless Information Systems and Computational Architectures

- Move from new concept, to new theory, to new algorithms, to implementation
  - Advanced communications, radar, sensing, positioning and navigation

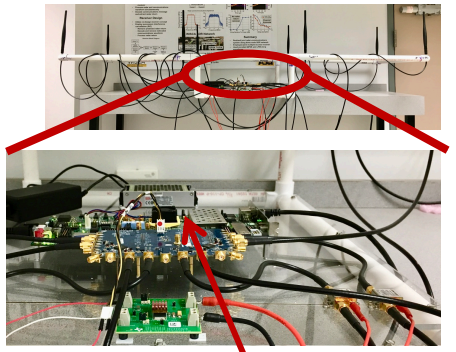


- **Enable next generation advanced RF system research**
  - Fluid radio protocols
  - Interference robustness
  - RF convergence

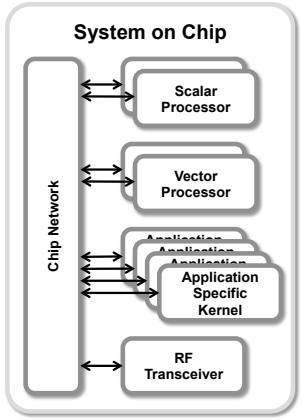
Ettus Software-Defined Radios

- **Perform experimental demonstrations**
  - Quick over-the-air examples
  - Real-time experiments

Semi-Custom SDRs



New Chip Architectures



- **Develop new high-performance flexible computational architectures**
  - Heterogeneous architectures

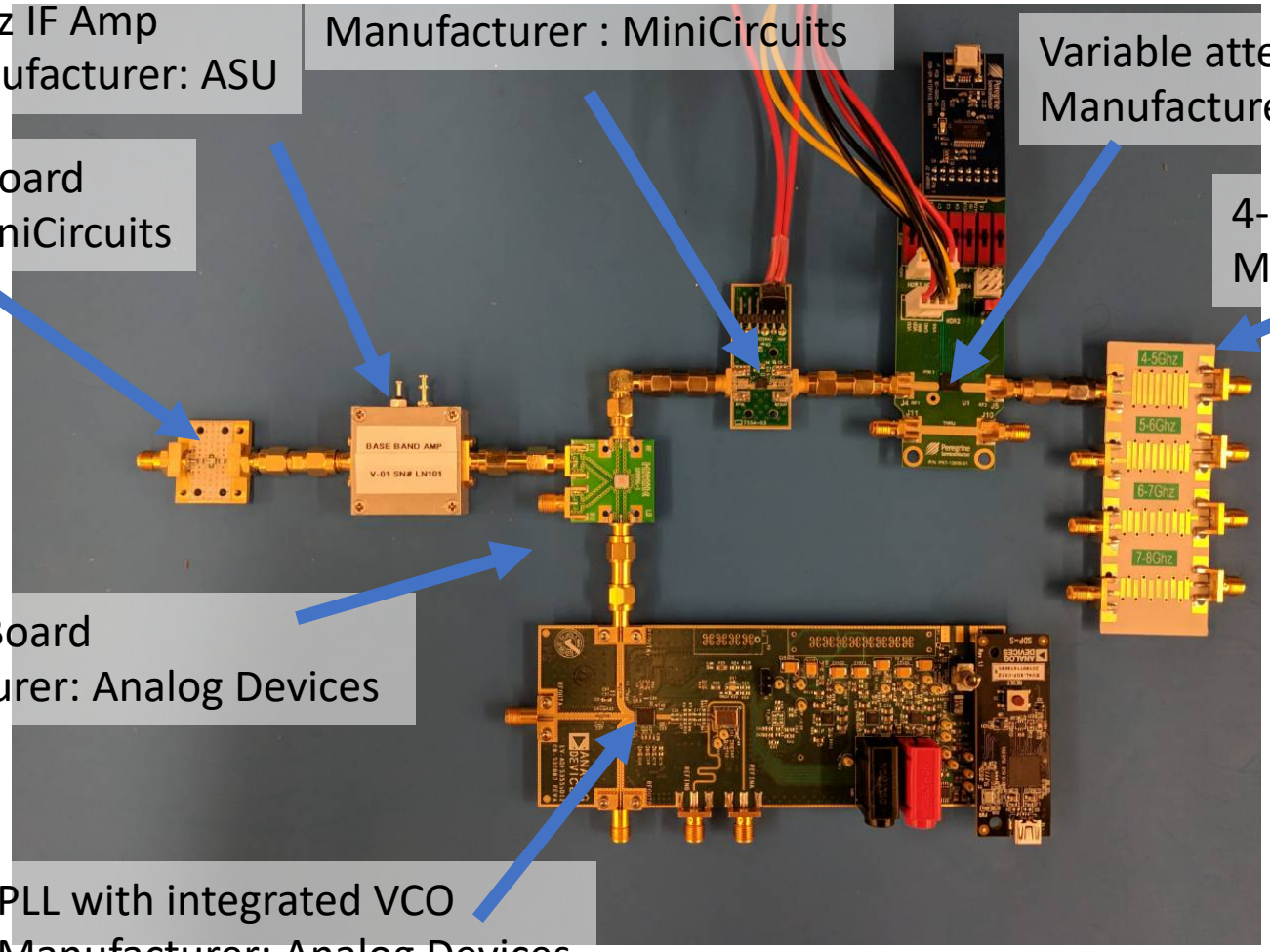
Arizona State University

WISCA Center for Wireless Information Systems and Computational Architectures

Bliss Laboratory of Information, Signals, and Systems

wisca.asu.edu

Integrated Analog IF Board Development



1GHz IF Amp
Manufacturer: ASU

1-8GHz RF Amp Demo Board
Manufacturer : MiniCircuits

Variable attenuator Board
Manufacturer : Peregrine

1GHz LPF Demo Board
Manufacturer: MiniCircuits

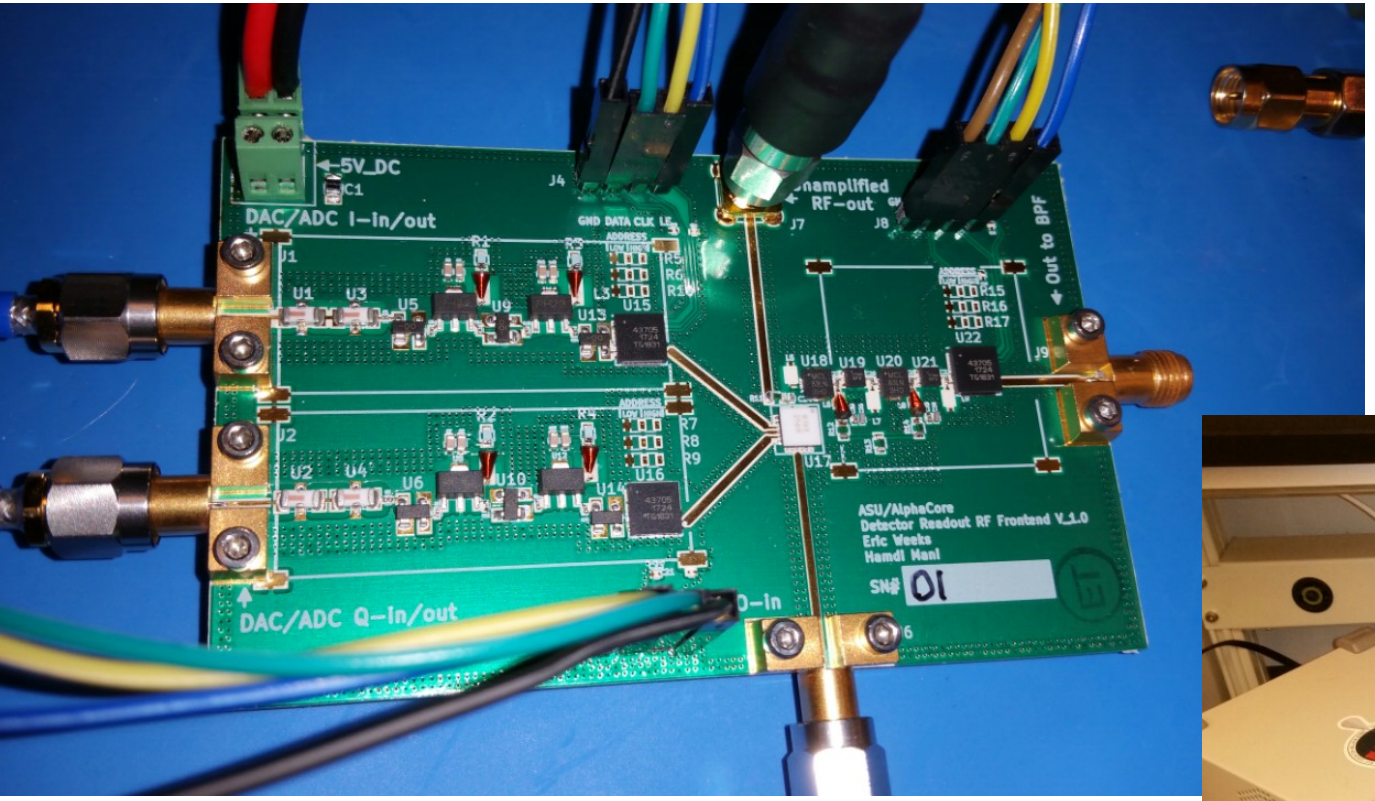
4-8GHz RF Filters
Manufacturer: ASU

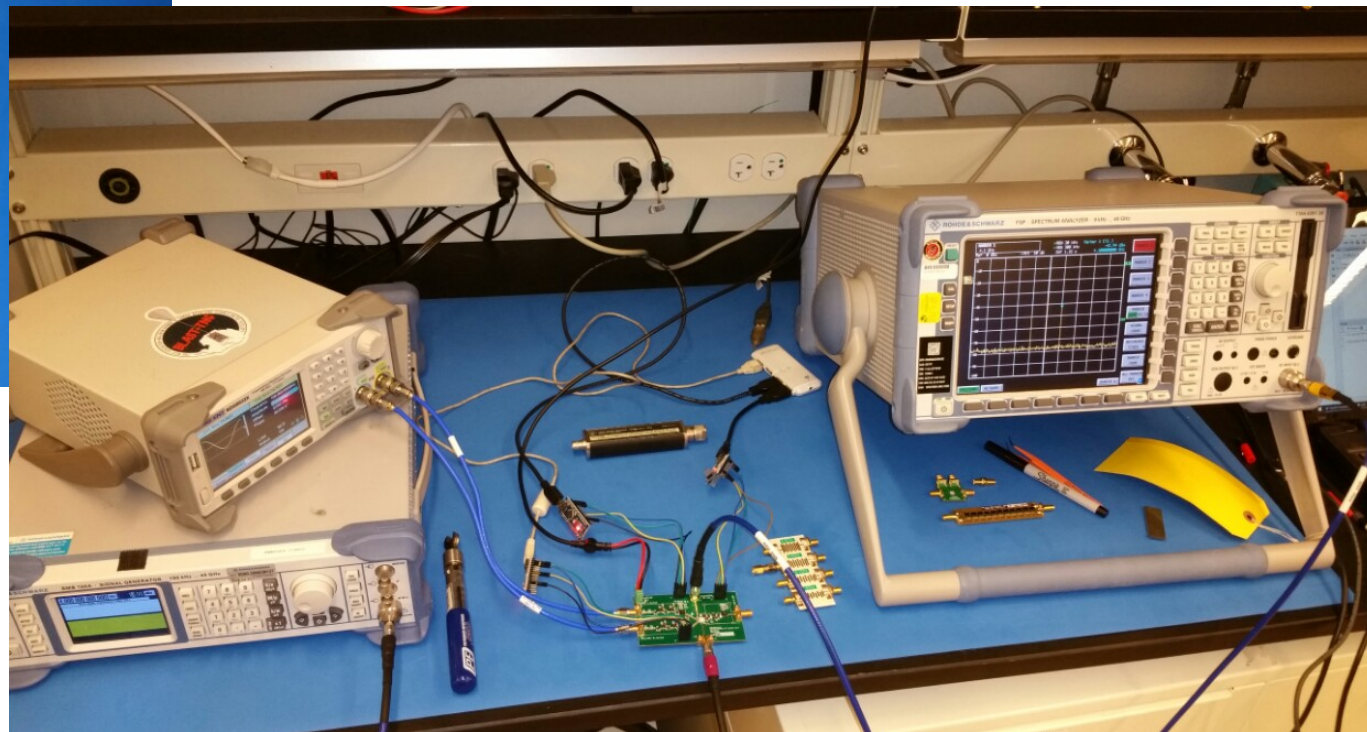
IQ Mixer Board
Manufacturer: Analog Devices

PLL with integrated VCO
Manufacturer: Analog Devices

Eric Weeks
Hamdi Mani
…

Integrated Analog IF Board Development





Eric Weeks
Hamdi Mani
…

Conclusions

- Both the FFT and CORDIC algorithms work well and have heritage
- Combining the advantages of both, especially for tone tracking, is worth further investigation
- Xilinx RFSoC FTW
  - Commercially-available board
  - Low power
  - Lots of compute