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New Developments in Micropower ASICs for 3D Pixelated Charge Readout of Liquid Argon Time-Projection Chambers

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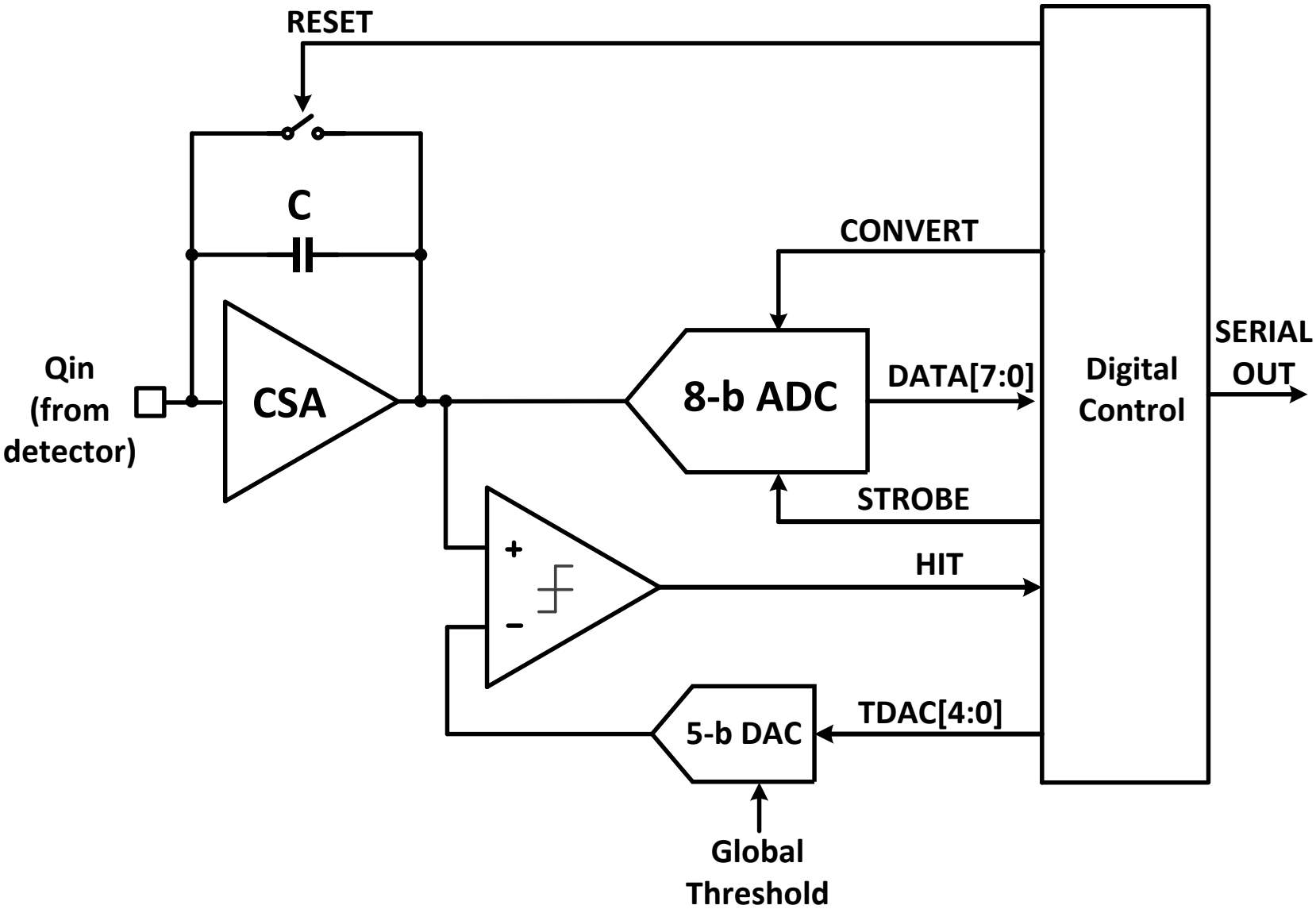
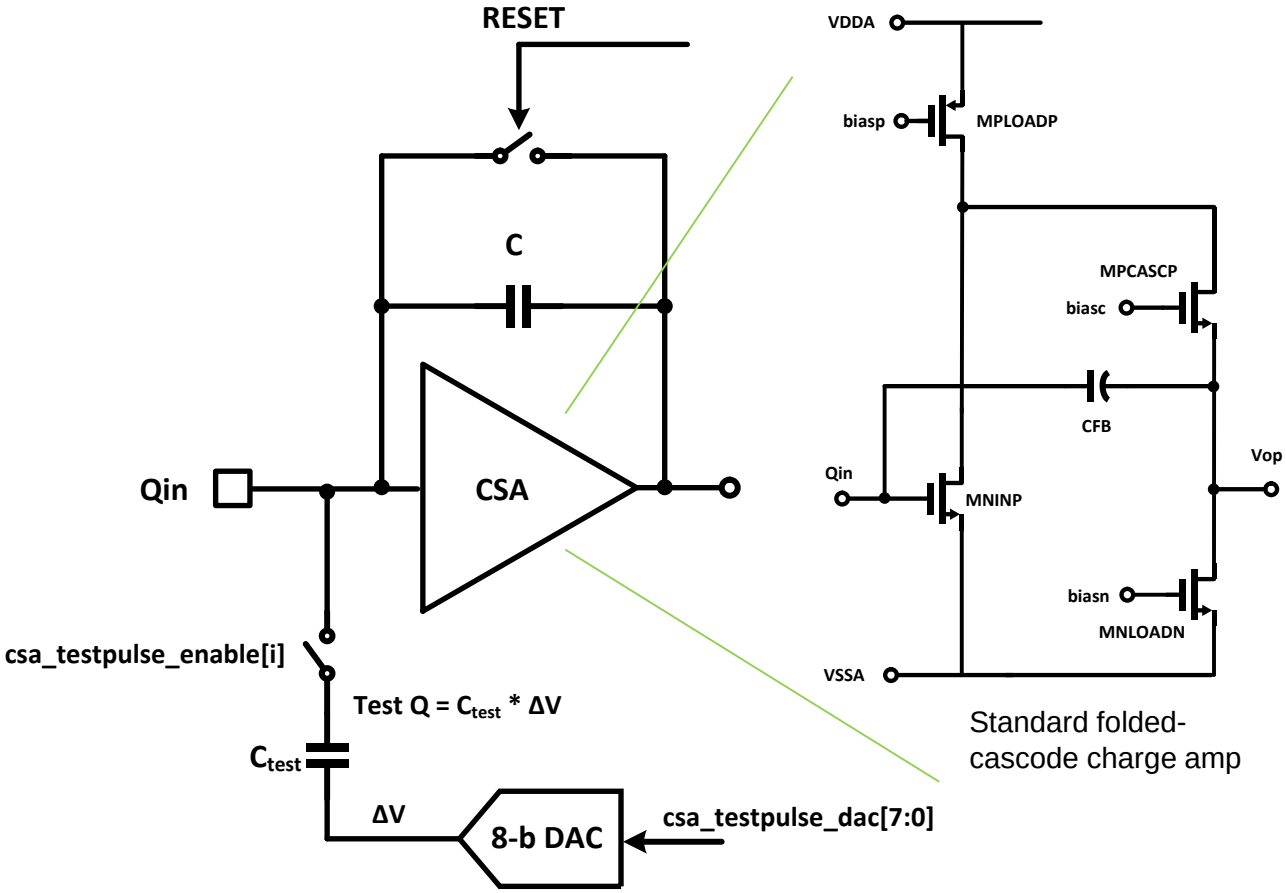
What is LArPix?

- The Liquid Argon Pixel ASIC (LArPix) is a 32-channel ASIC designed to instrument pixelated TPC anodes immersed in liquid argon
- The reduced capacitance and subsequent relaxed noise specifications of pixelated LAr-TPCs allow significant power reductions relative to traditional wire-plane LAr-TPCs
- LArPix must be low power due to large number of potential channels in a large detector
- Initial device successfully imaged cosmic-ray muons in a pixelated LAr-TPC

LArPix Channel



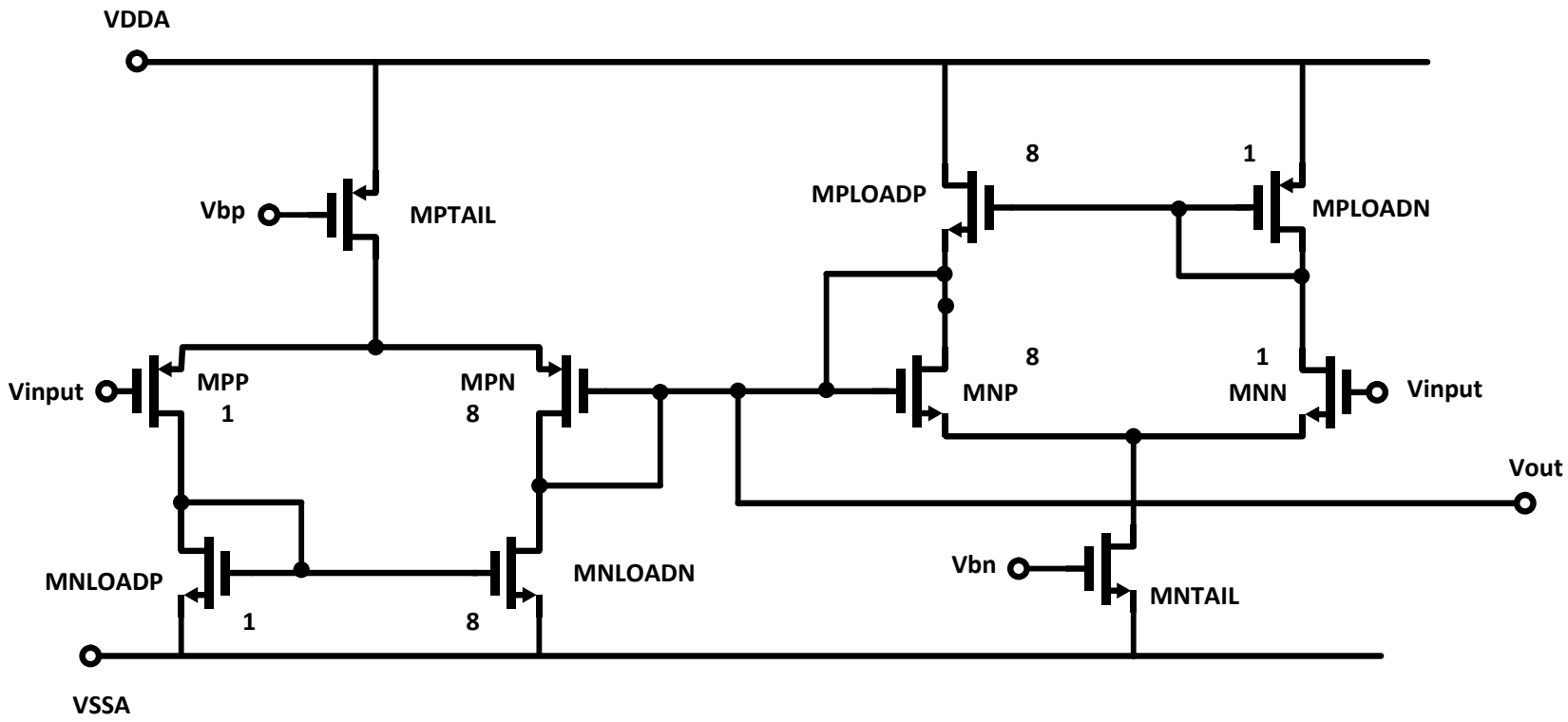
LArPix Front-End



CSA with integrated test pulser

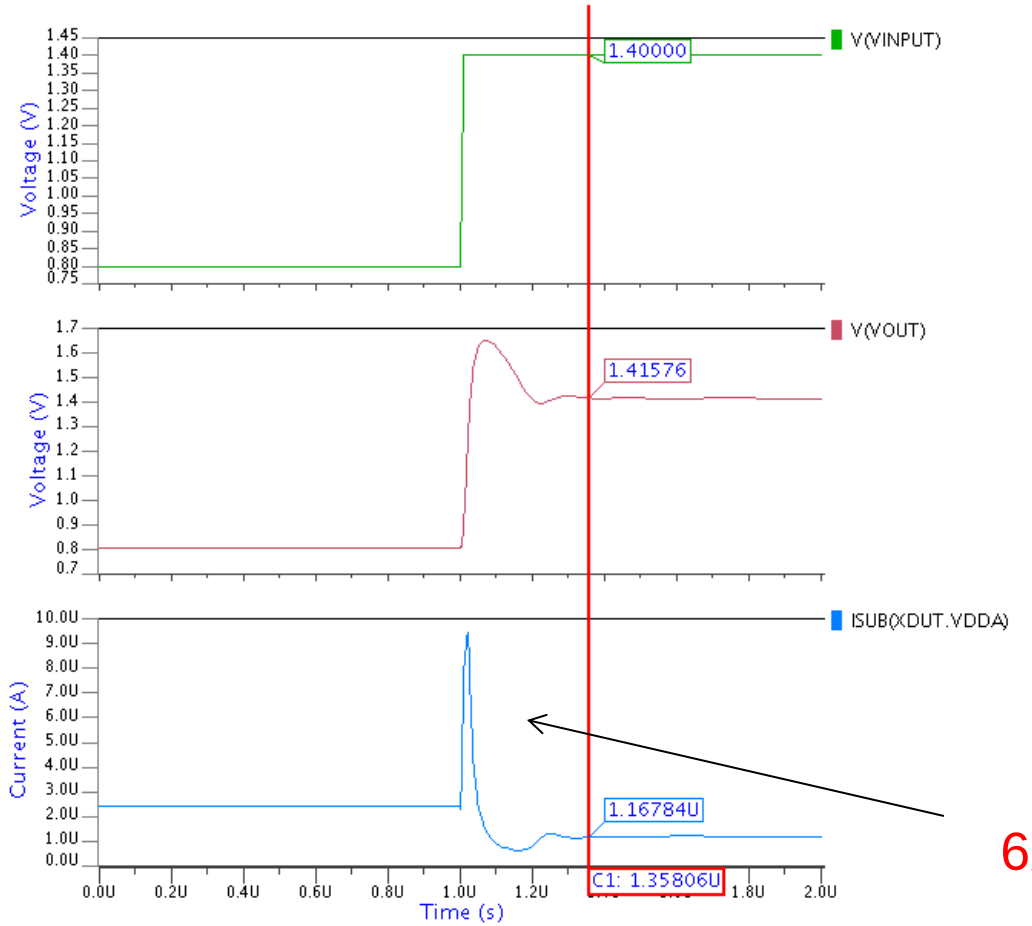
Conservative design to balance noise performance and power dissipation

Class AB Buffer



- In quiescent conditions, DC current is controlled by tail devices
- When driven, all the reference current of one of the pair is switched to the 1X device, so it is multiplied by 8 when copied to the output
- Load also “steals” current from other pair

Class AB Buffer (cont)



CSA output

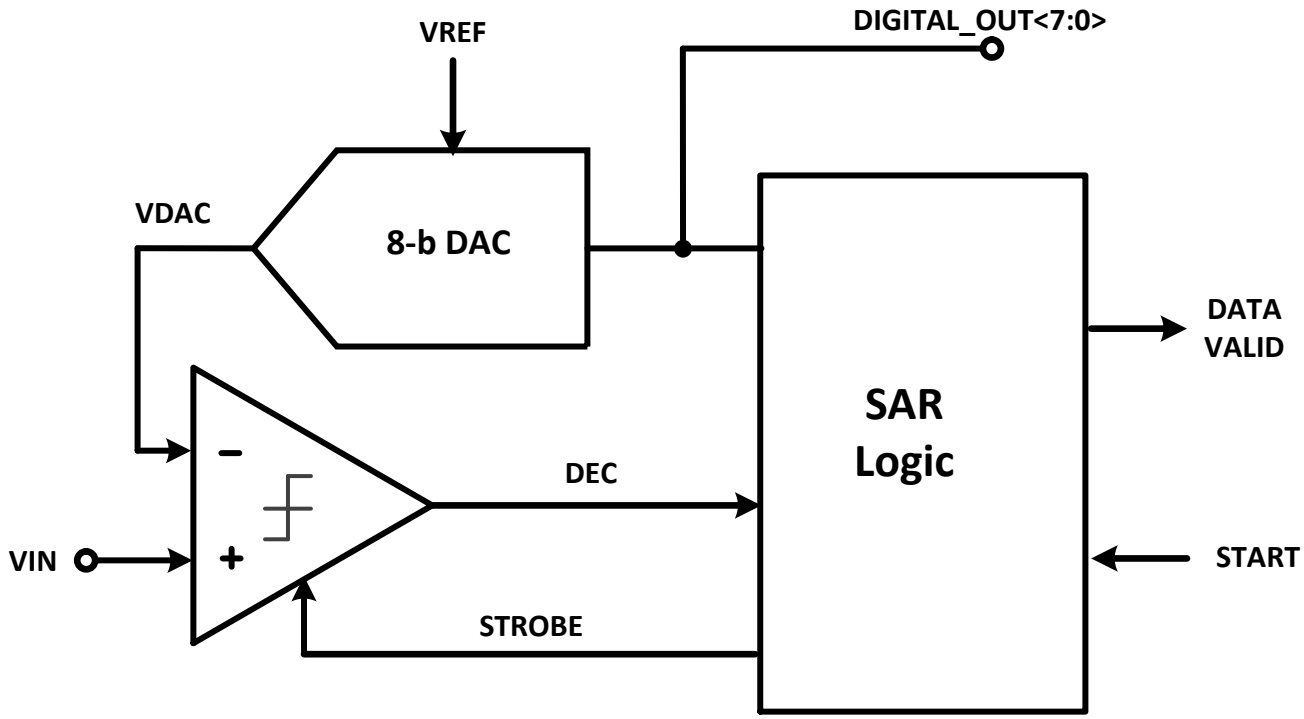
Buffer output

Buffer current draw

6X higher peak load current

Big power savings because we don't need to supply the peak load current all the time

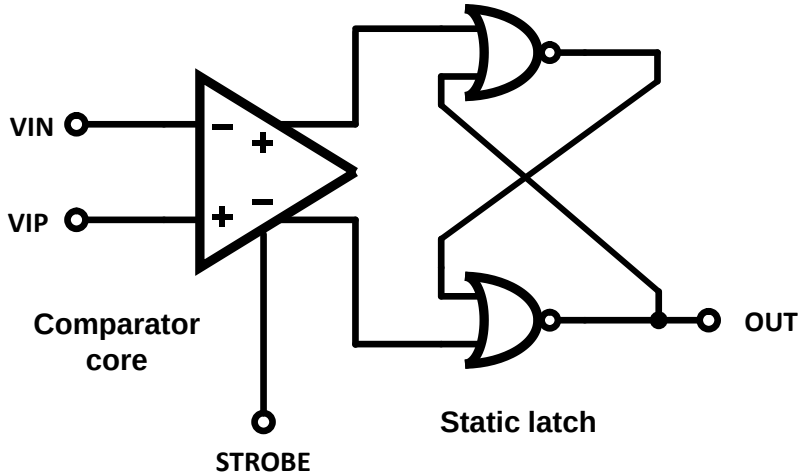
Successive-Approximation ADC

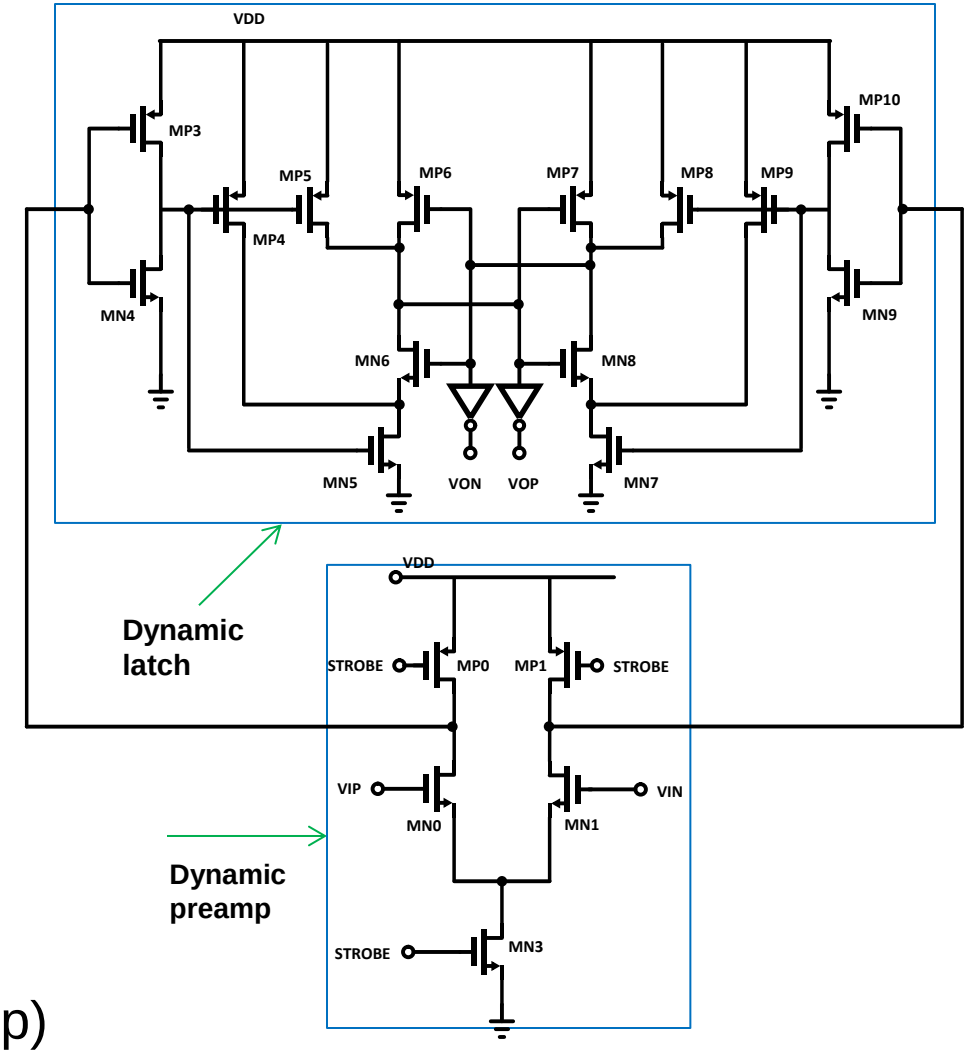


Fully dynamic → dissipates no static power
SAR logic implements binary search algorithm (implemented in Verilog)
Changed at last minute from 6 to 8 bits → bug in updated SAR logic
limited prototype to 6-bit operation

VREF sets quantization noise, DAC capacitance sets thermal noise

Dynamic Comparator (for ADC)



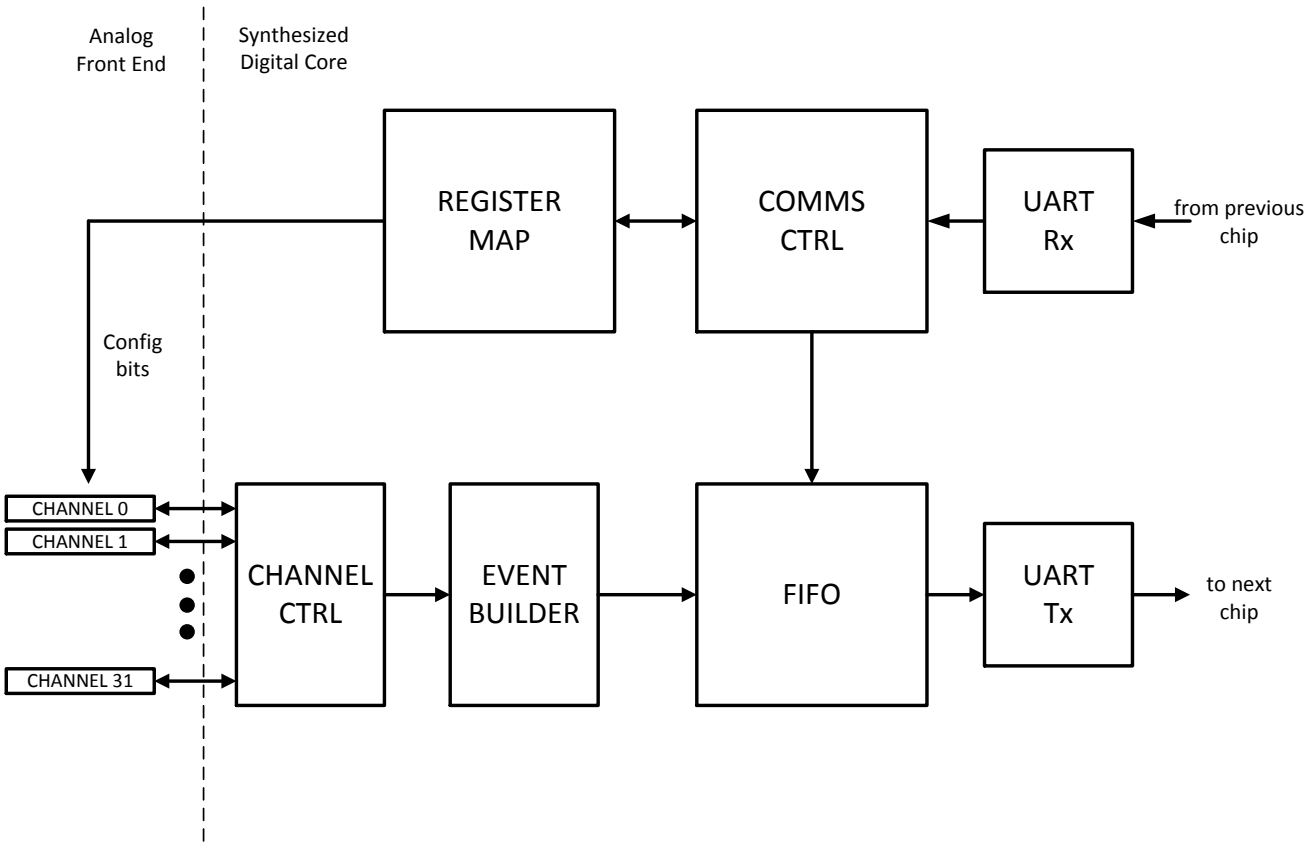


No static power dissipation

Low-ish offset (reduced by preamp)

ADC is highly offset tolerant (can be nulled by adjusting threshold)

LArPix Backend



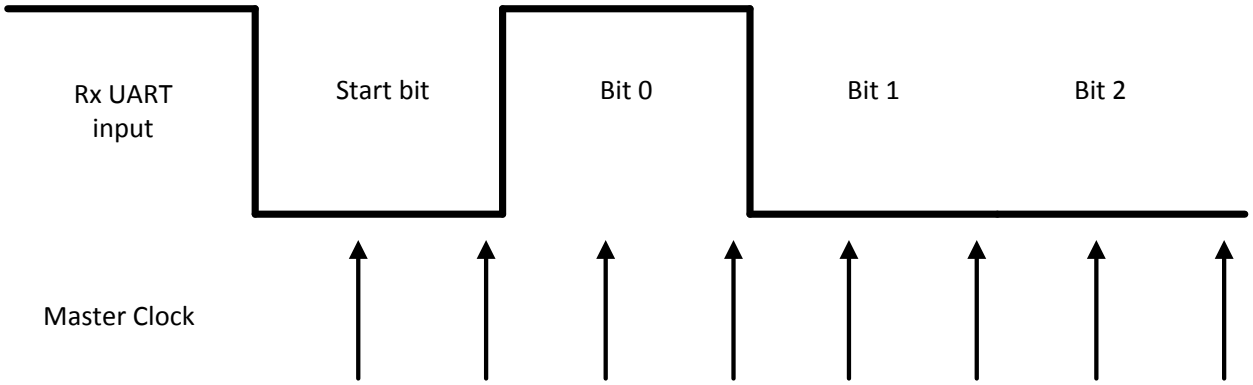
Data from downstream chips and AFE stored in shared FIFO

Simple Universal Asynchronous Receiver/Transmitter (UART) for chip-to-chip communication

When FIFO not empty, it is slowly drained by UART. FIFO depth depends on expected maximum signal burst (e.g. track perpendicular to pixel array) and daisy chain length

LArPix UART

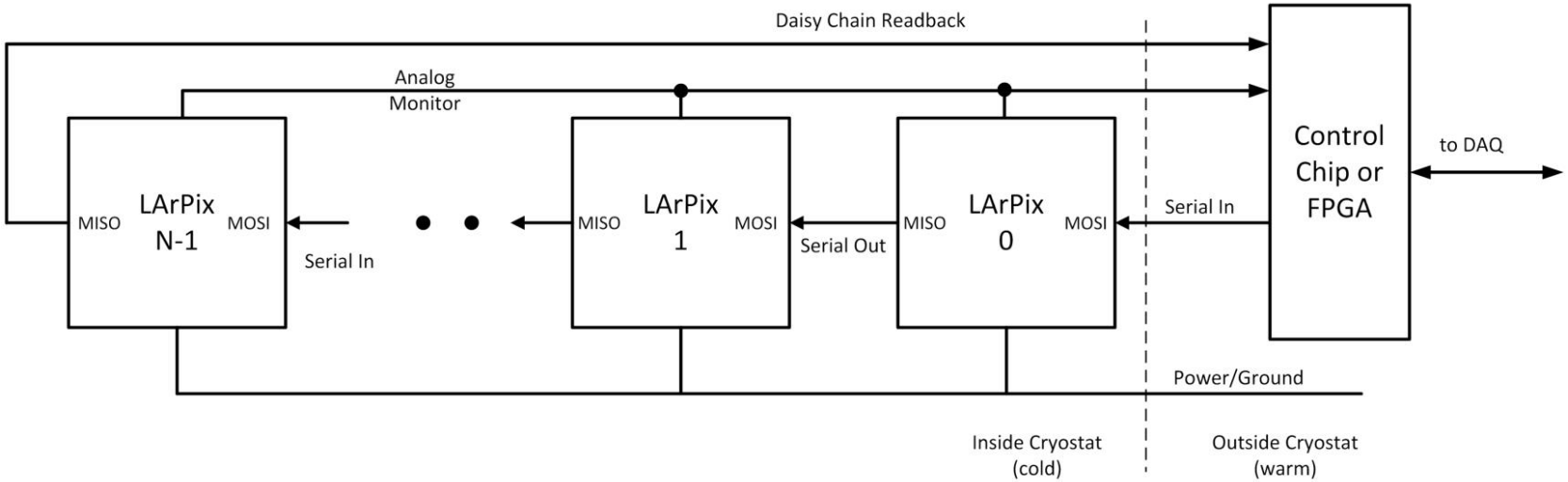
UART oversamples so phase locking between data and clock not required



- Allows bi-directional digital communication over 2 wires:
  - No chip select, dedicated clock, or synchronization pins required

- For simplicity, all I/O words (data, configuration, test) are a common length: 54-bits
- UART includes test patterns to simplify synchronization with master FPGA

LArPix Daisy Chaining



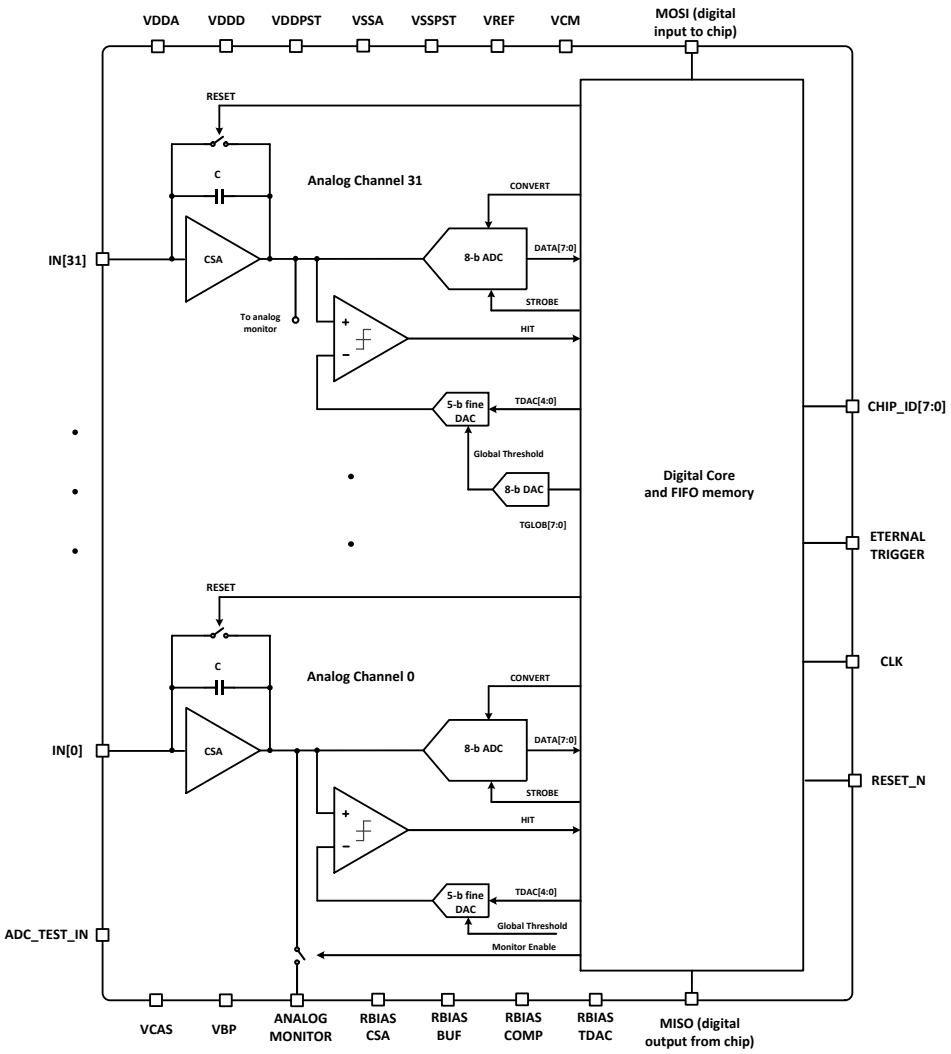
Up to 256 LArPix chips can be daisy chained

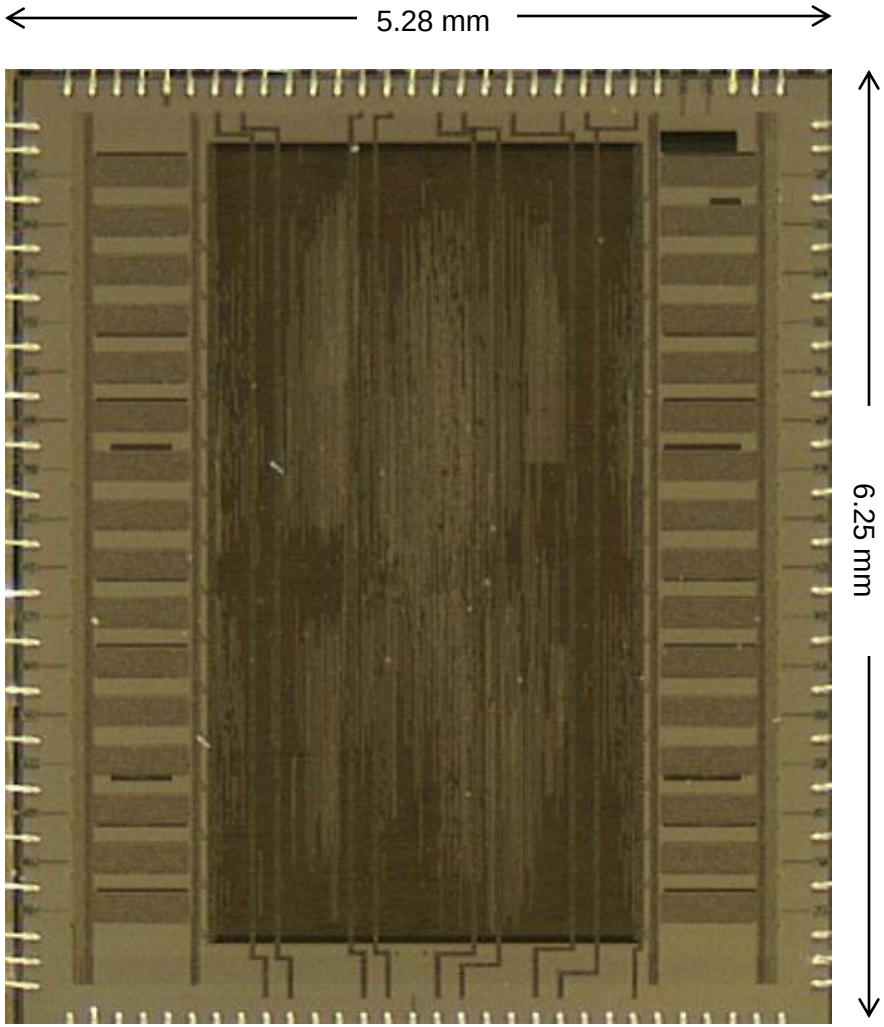
Each chip gets unique address based on bonding option

PRO: Low number of cryostat penetrations (two per daisy chain)

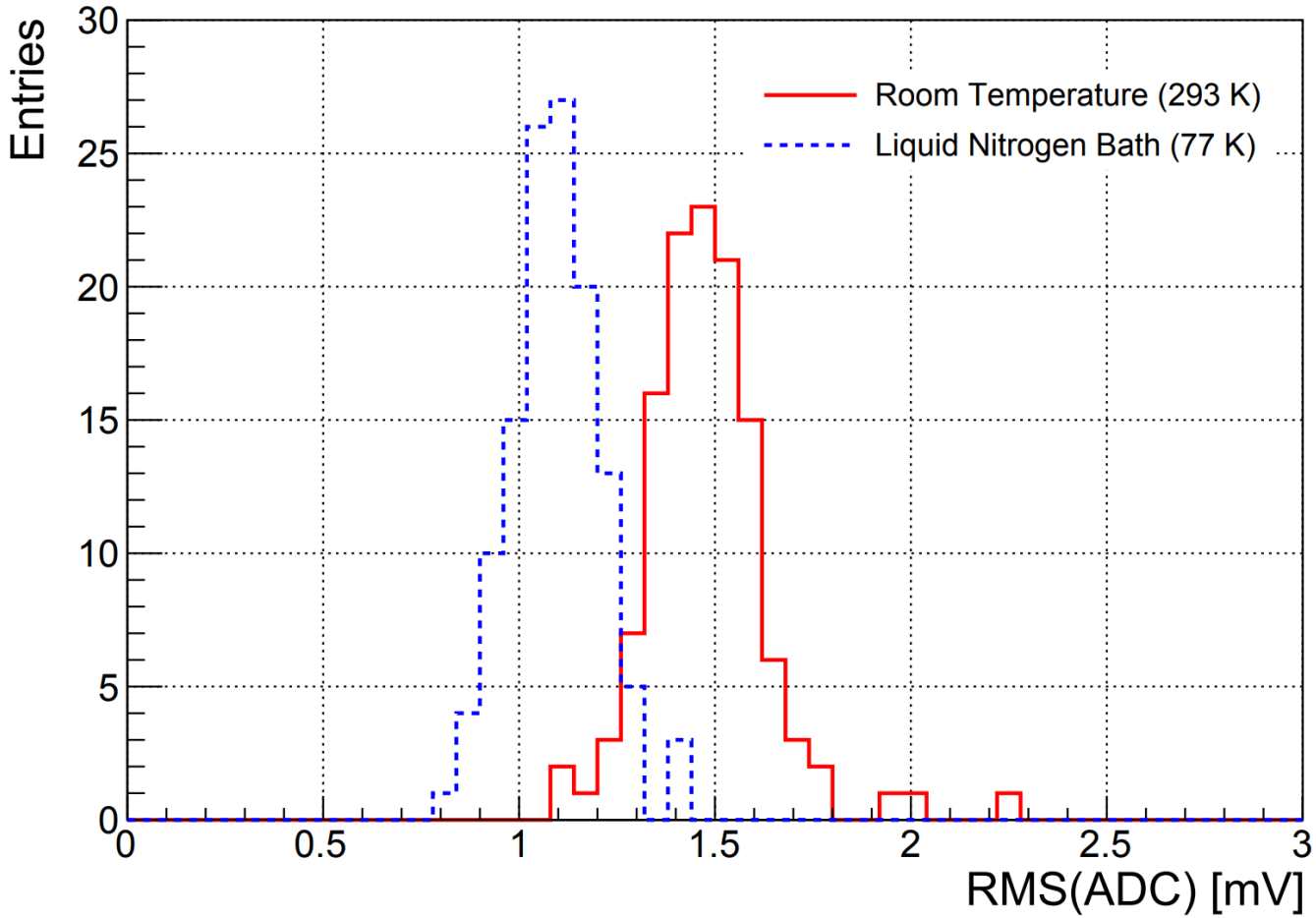
CON: Not robust. Chip failure disables entire daisy chain.

LArPix Prototype





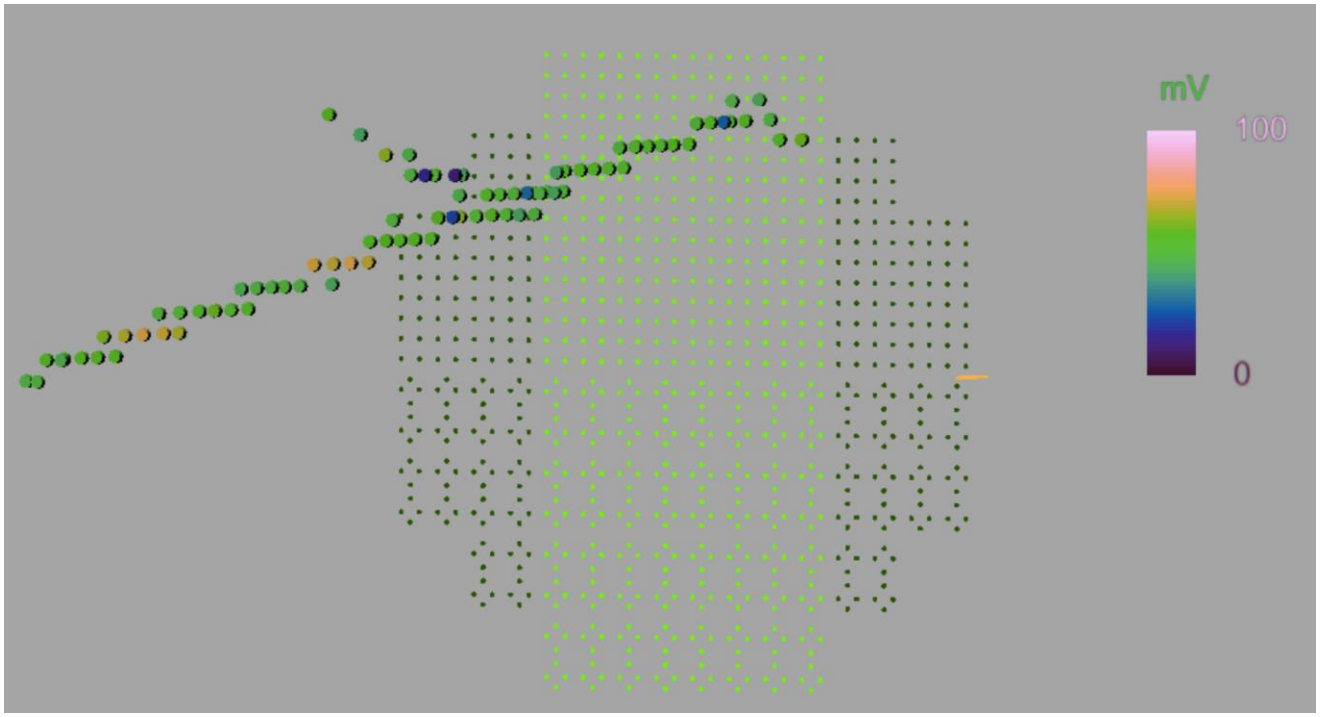
LArPix Noise Performance



Input-referred noise across four LArPix ASICs; no sensor attached

Noise reduced from approx. 1.5 mV-rms (375 e^-) to 1 mV-rms (250 e^-)

LArPix Particle Tracking



A detected cosmic-ray muon track in a Liquid Argon TPC projected onto a PCB-based two pattern anode instrumented with 128 LArPix channels (four LArPix chips). The active channels are in bright green.

Performance Summary

LArPix-v1 Performance: 1.5 V analog and 1.1 V digital		
	Value	Units
CMOS Technology	180	nm
Number of Channels	32	
Equivalent Noise Charge (300 K)	375	electrons
Equivalent Noise Charge (77 K)	250	electrons
Channel Gain	4	mV/e^-
Channel Dead Time	3	clock cycles
FIFO Event Buffer Depth	2048	events
Nominal Clock Rate	2	MHz
Analog Power Dissipation	24	µW/channel
Digital Power Dissipation	37	µW/channel
Die Area	32.8	mm^2

LArPix-v2

Next version of LArPix intended for deployment in ArgonCube

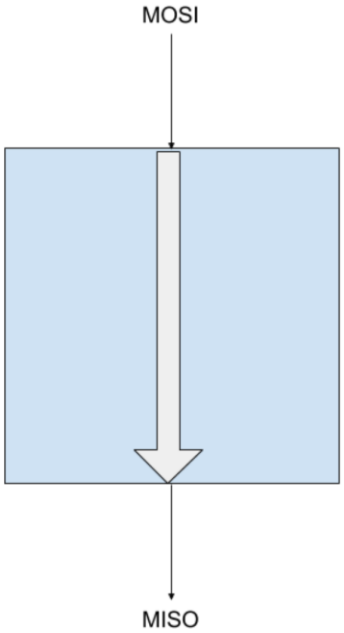
Key improvements:

- New readout scheme address system reliability (Hydra I/O)
- Optimize channels per chip (32 → 64)
- Internal biasing (reduce number of external passive components)
- Reduced dead time (optimized digital core logic)
- Implement digital core with clock-gating to reduce power
- Clocking options allow faster ADC operation if desired
- On-chip voltage regulators for power-supply mitigation
- Migrate FIFO from registers to SRAM to reduce power and area
- Bug fixes

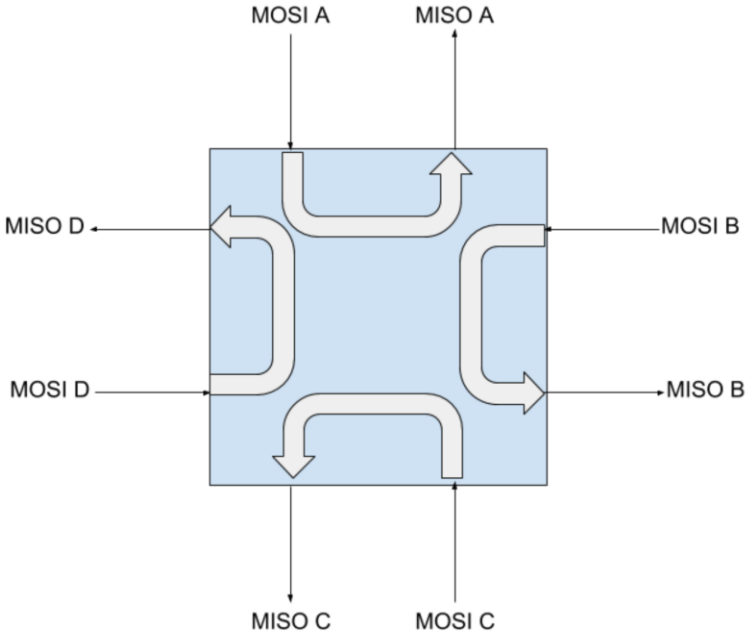
Hydra-I/O

Hydra I/O is a new, robust approach to LArPix data I/O developed by Dan Dwyer. Each ASIC has four independent UARTs that can be freely configured

Hydra I/O combines the simplicity of the UART approach with robustness to chip failure and easier system characterization



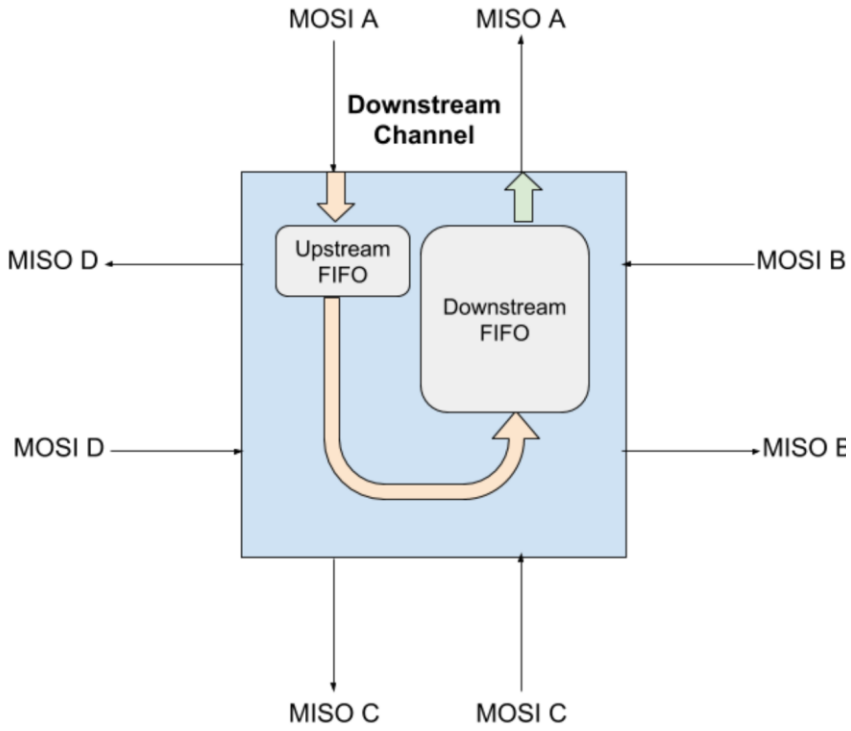
LArPix-v1 single-UART daisy chain



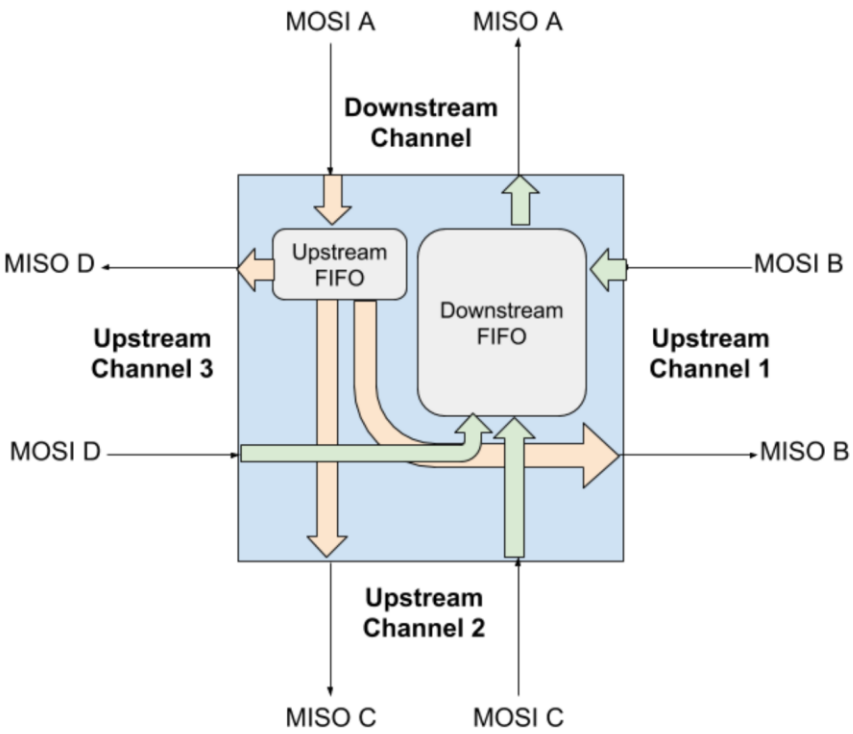
LArPix-v2 4-UART Hydra system

Hydra-I/O (cont)

Upstream FIFO carries configuration data to the network. Downstream carries hit data and configuration responses back to the controller



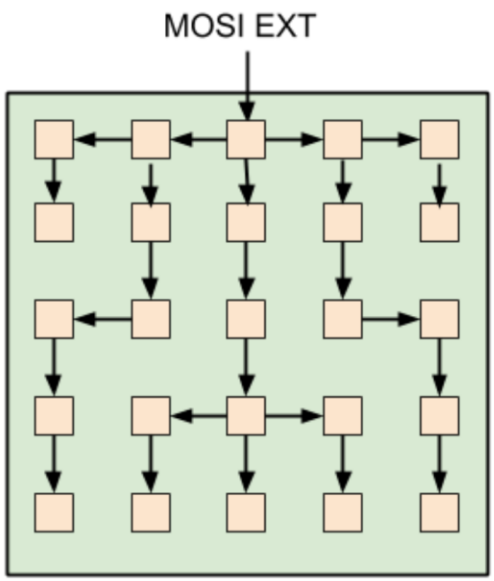
Configured as in LArPix-v1



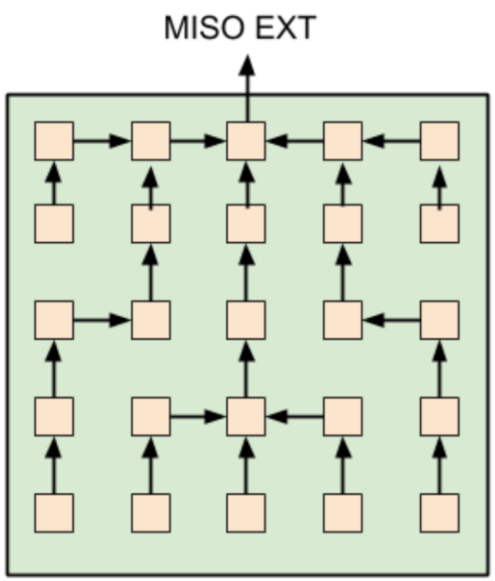
Richer configuration with one-to-many and many-to-one connections

Hydra-I/O (cont)

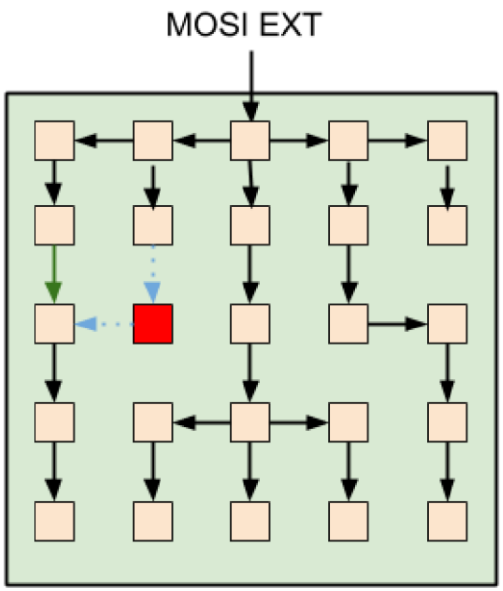
Example ad-hoc network for 5 by 5 ASIC grid. Each ASIC is individually addressable with programmable chip ID



Upstream Network for configuration

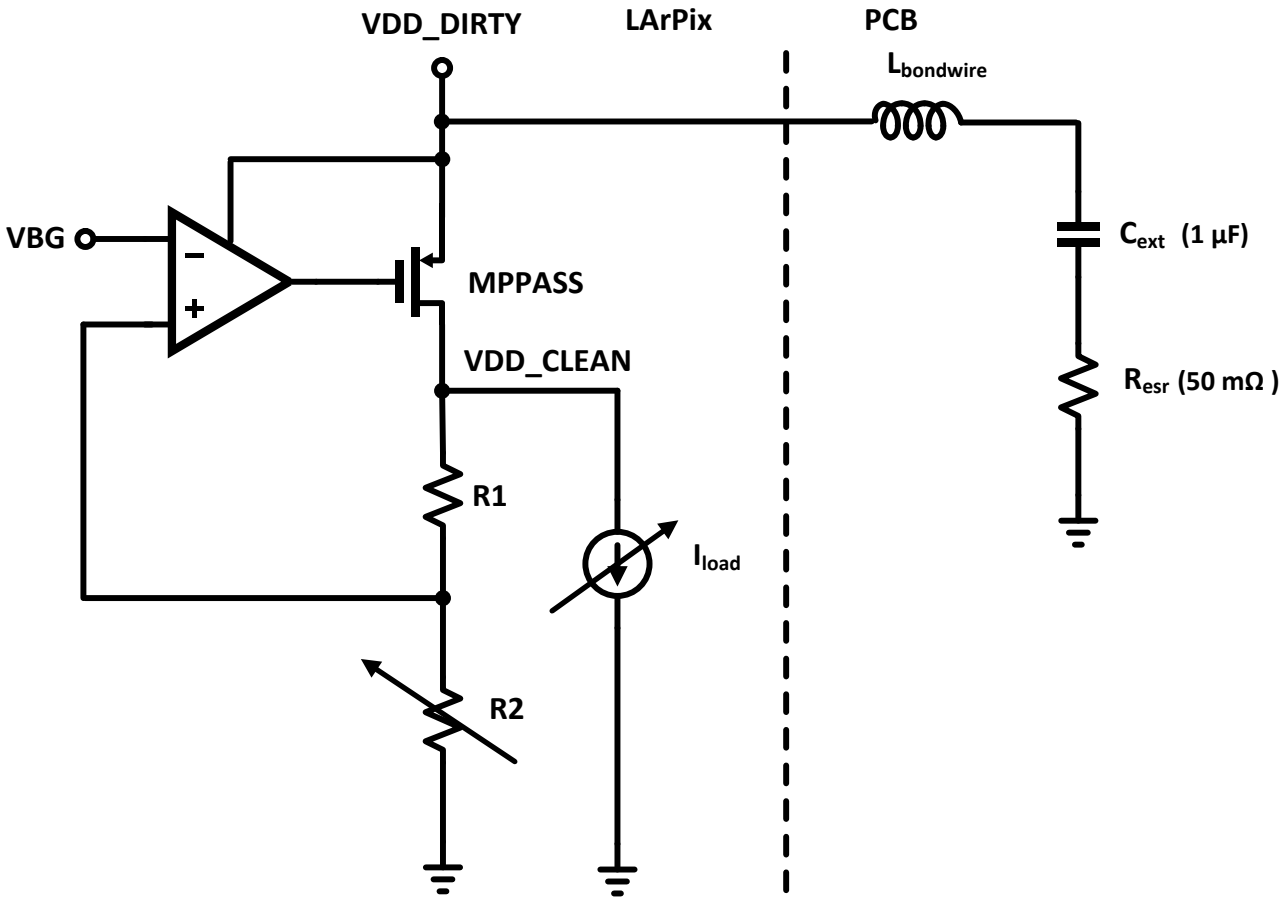


Downstream network for data collection



New upstream network routing around failed node (in red)

LArPix-v2 (LDOs)



- 64 analog channels implemented as four distinct banks of 16
- Each bank has dedicated LDO
- LDO can be powered down to isolate bank in case of fault
- Improves LArPix immunity to supply and PCB noise and interference
- > 50 dB low-frequency rejection expected

Future Developments

LArPix is a data acquisition ASIC platform that allows scalable channel count without unmanageable growth in cost or complexity

Requirement	Possible Implementations
Higher Front End Speed	Faster ADC, waveform sampling, asynchronous techniques
Higher data speed	Replace UARTs with LVDS
Lower Noise	Upgrade front end
Precision Timing	Add TDC hardware
Higher Dynamic Range	More ADC bits, nonlinear ADC
Lower Power	Lower supply, asynchronous ADC, smaller FIFO

All of these would require tradeoffs, e.g. in noise or power

Examples:

Gas detectors: Faster front end and ADC, relaxed power requirements

Photodetection: Faster front and back end, lower gain, dedicated timing

Conclusion

- LArPix is an ASIC platform for scalable, low-cost pixelated readout
- LArPix-v1 successfully imaged cosmic-ray muons in a pixelated LAr-TPC
- Improved LArPix-v2 currently in development
- A flexible base architecture means future LArPix-based readout ASICs could address a wide range of use cases beyond LAr-TPCs

LArPix CONTRIBUTORS

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