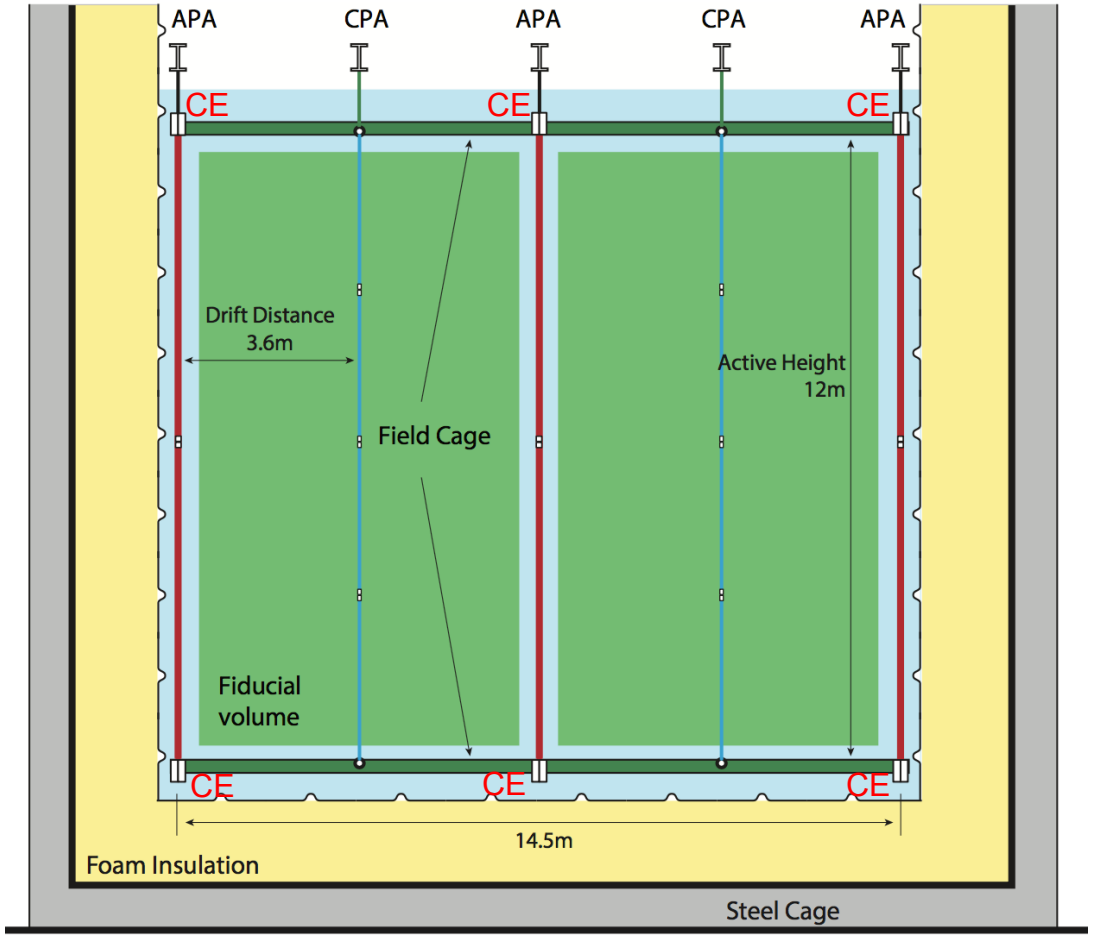
Cold Electronics for Noble Liquid Detectors

Mark Convery

December 11, 2018

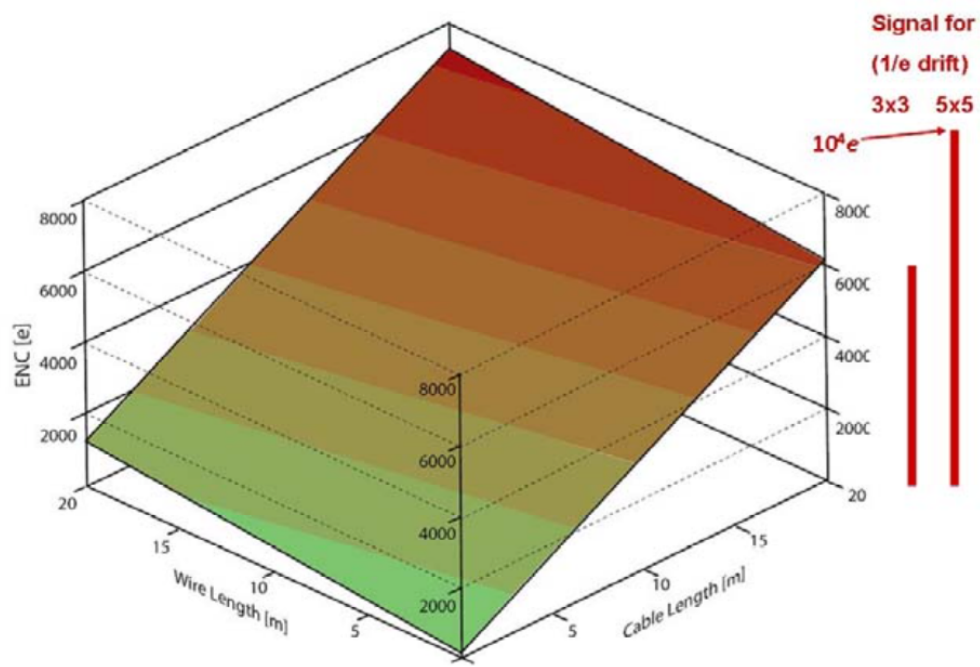
“Giant” Liquid Argon TPC Detectors

- DUNE’s long-baseline physics goals require >10kT LAr fiducial volume: ~25 m diameter sphere
- Rectangular cryostat depth limited to ~15 m by hydrostatic pressure
- How to instrument 15m high volume?



Cold Analog Motivation

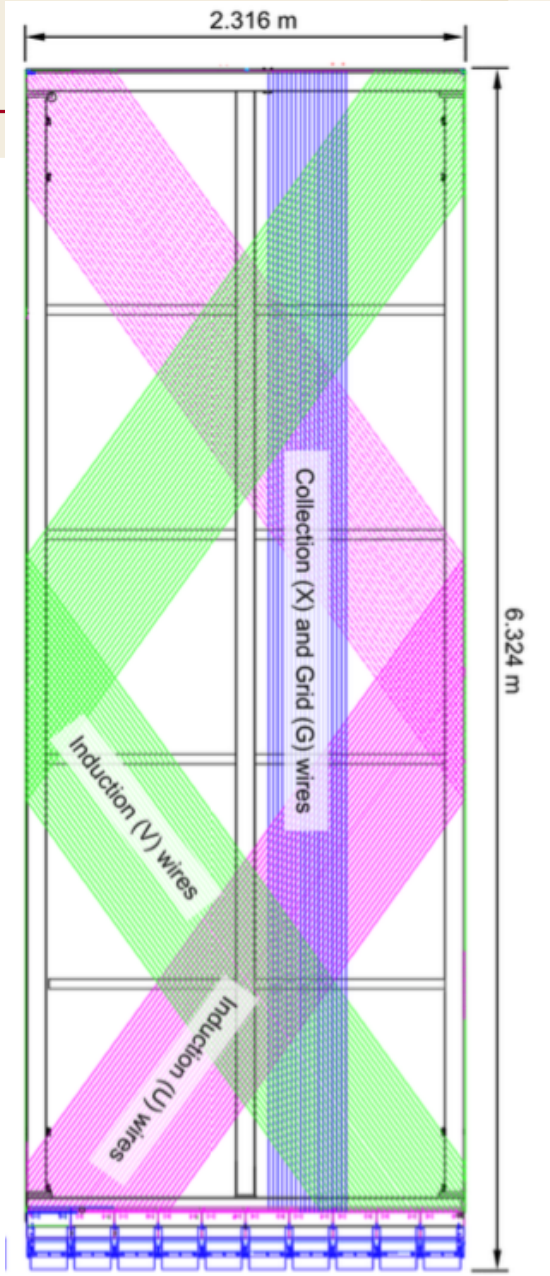
- Largest source of irreducible noise linearly increases with detector and cable capacitance, and decreases with transconductance: $e_{ENC}{}^2 \alpha (C_{det} + C_{cab})^2/g_m$
- For wire or cable lengths ~ 10m, e_{ENC} ~500 e^-
- Compared to expected signal of ~10,000 e^-, sets practical limit on wire+cable length of about 10 m – not enough to build DUNE-scale detector
- Solution: add active electronics (amplifiers) in the cold
- Building LArTPC > 10m does not seem possible without cold analog electronics



Cold electronics for "Giant" Liquid Argon Time Projection Chambers, Radeka et al. , Journal of Physics: Conference Series 308 (2011) 012021

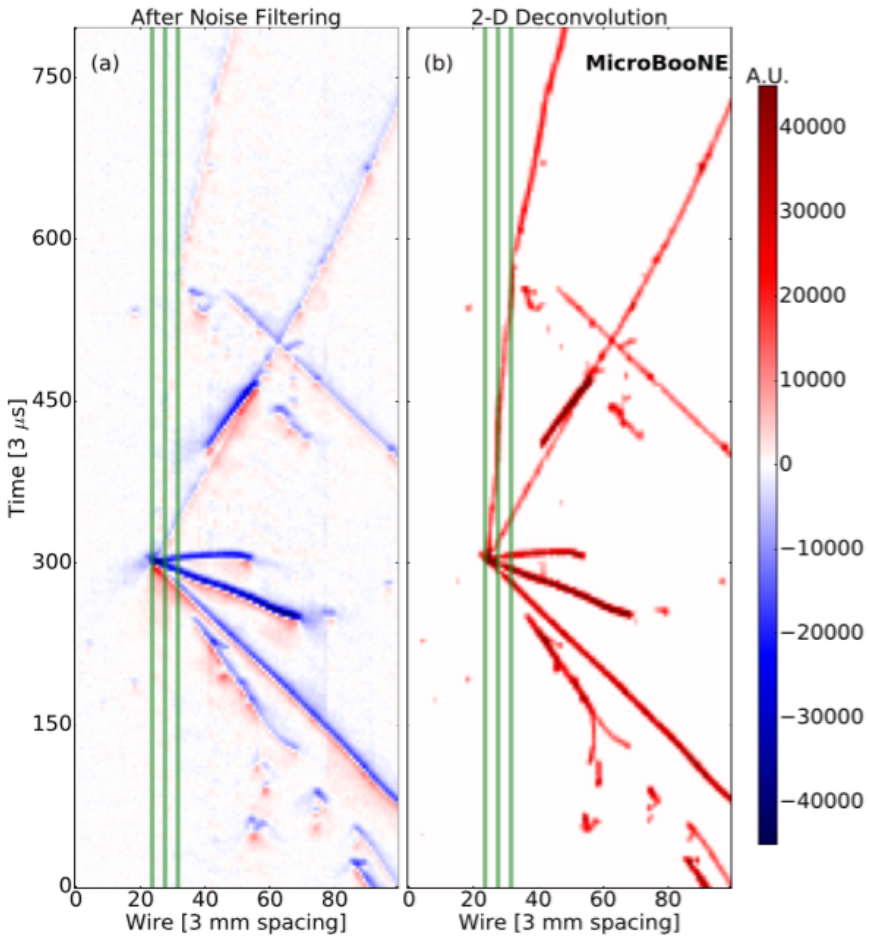
Cold Digital Motivation

- With ~50K wires/kTon, cable management becomes a challenge
  - How to bring signal up from bottom modules?
- Solution: TPC signals are slow (~2 MS/s)!
  - Can multiplex many (~32) channels on to a single digital line (1Gb/s)
- Cold digitization and digital multiplexing great reduce cable plant – e.g. signals can be run through frame of wire plane



Need to Read All the Data

- Initial plans for fully cold electronics assumed that data could be “zero-suppressed” before transmission
- Detailed studies indicate that all data must be saved to correctly reconstruct induction plane signals
- Also, at rates >1 Gb/s, signal cables don’t dominate cable plant (power does).



MicroBooNE, JINST 13 P07006 (2018)

DUNE Cold Electronics Requirements (from TDR)

SLAC

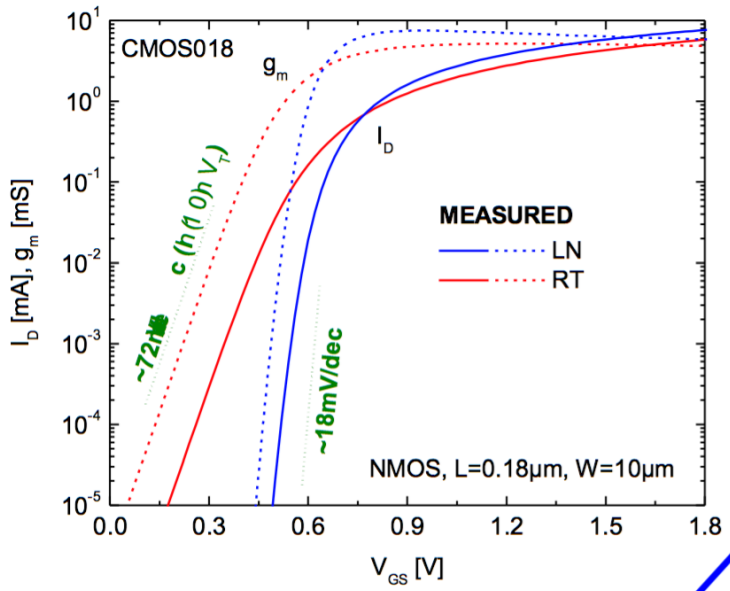
- Noise < 1000 e^-
- FE peaking time between and 1 and 3 μS
- ADC 2 MS/s
- Linear response to 500,000 e^- (stopping p's, etc.)
- Dynamic range 3000:1
- ADC not to add to noise
- Power/channel < 50 mW
- Highly reliable (>20 years in the cold without access)

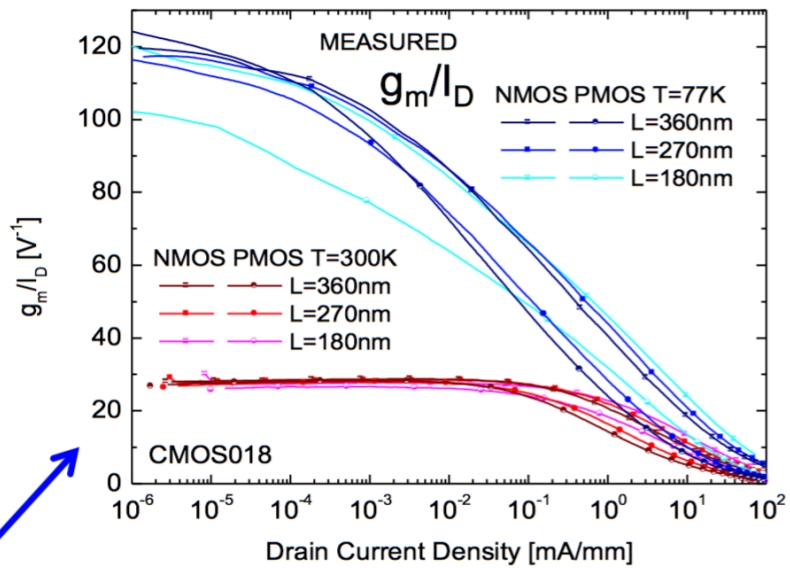
Progression: ICARUS->…->DUNE

	ICARUS	MicroBooNE	ProtoDUNE	SBND	DUNE (Baseline)	DUNE (Alternative)
Analog Front End	Warm	Cold (BNL LArASIC)	Cold (BNL LArASIC)	Cold (BNL LArASIC)	Cold (BNL LArASIC)	Cold (SLAC CRYO All-in-one)
ADC	Warm	Warm	Cold (BNL Domino)	Cold (COTS)	Cold (BNL/ FNAL/ LBNL SAR)	
Digital Multiplexer	N/A	N/A	FPGA	FPGA	ASIC (ColData)	

CMOS Noise Characteristics

- For large (>10 pF C_{det}), $e_{ENC}{}^2 = 4k_B T R_{in} (C_{det} + C_{cab})^2/t_P$
  - R_{in} = transistor input series resistance (=1/g_M transistor transconductance)
  - t_P = shaping time

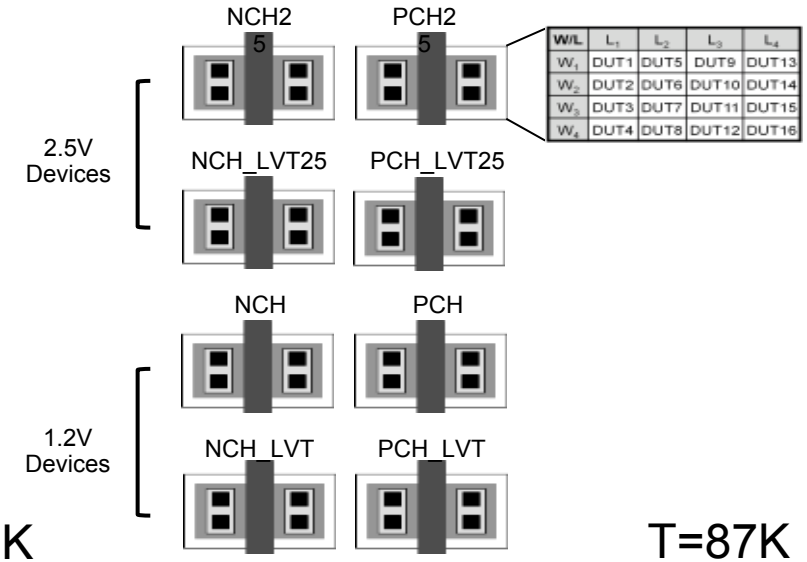




Transconductance/ drain current → $\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$

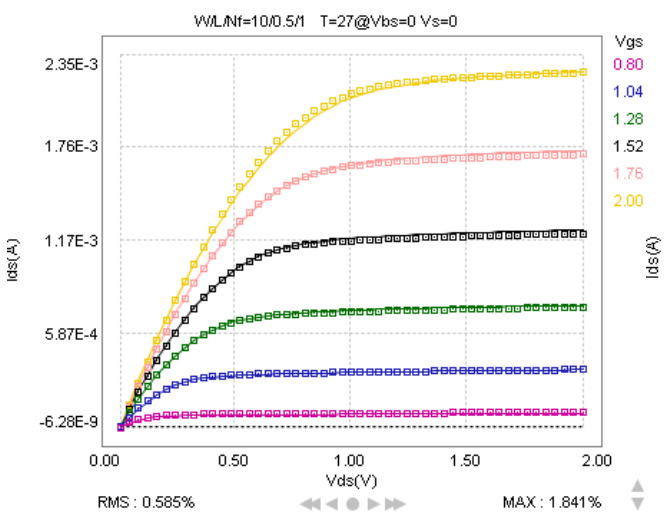
CMOS temperature dependent modeling

- Accurate models of transistor performance needed for ASIC designs
- Foundry models not reliable at LXe or LAr temperatures
- SLAC performed measurements to characterize and create model for all transistors needed. 8 different types and many combinations of W and L

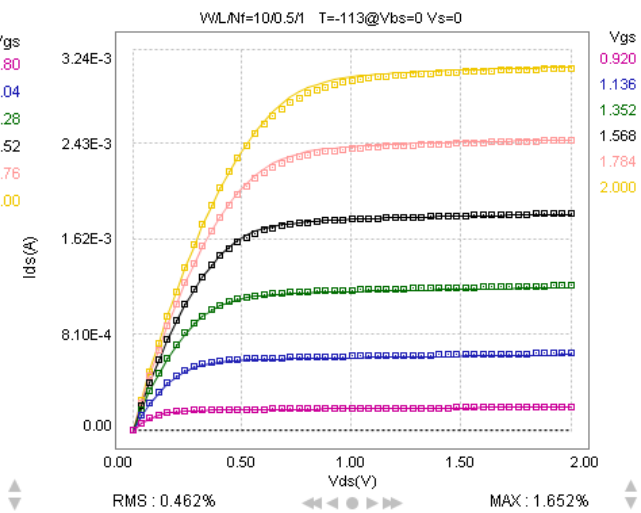


W/L	L_1	L_2	L_3	L_4
W_1	DUT1	DUT5	DUT9	DUT13
W_2	DUT2	DUT6	DUT10	DUT14
W_3	DUT3	DUT7	DUT11	DUT15
W_4	DUT4	DUT8	DUT12	DUT16

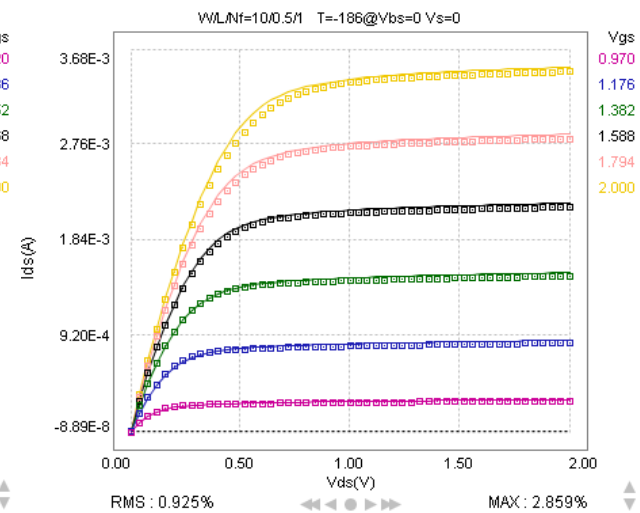
T=293K



T=165K



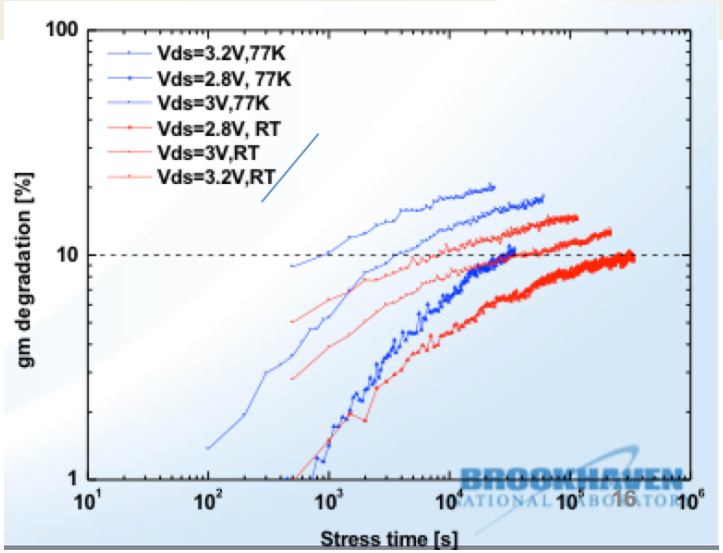
T=87K

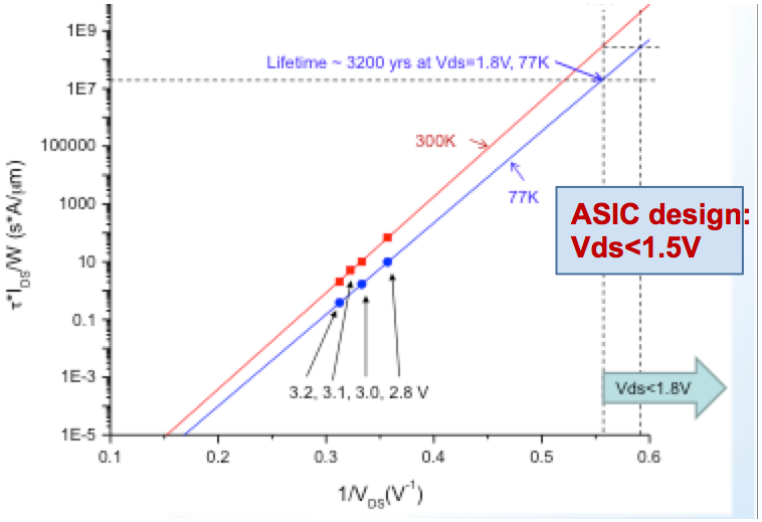


CMOS Lifetime

- While most CMOS aging processes slow down at low T, one exception is the “hot carrier effect”
- Causes damage that builds up over time and changes transistor parameters (e.g. g_m)
- Parameter change of 10% defines “lifetime” of the ASIC
- Accelerated lifetime “stress” testing by running at high V_{ds}
- Implies long lifetime may be achieved by
  - lowering V_{ds} 10% below normal
  - Increasing device length by 50%

$$\ln\left(\frac{\tau I_{ds}}{W}\right) \propto \frac{\varphi_{it}}{q\lambda E_m} \propto \frac{1}{V_{ds} - V_{dsat}}$$

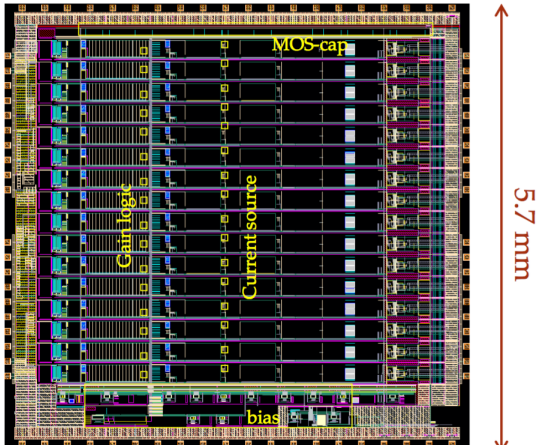




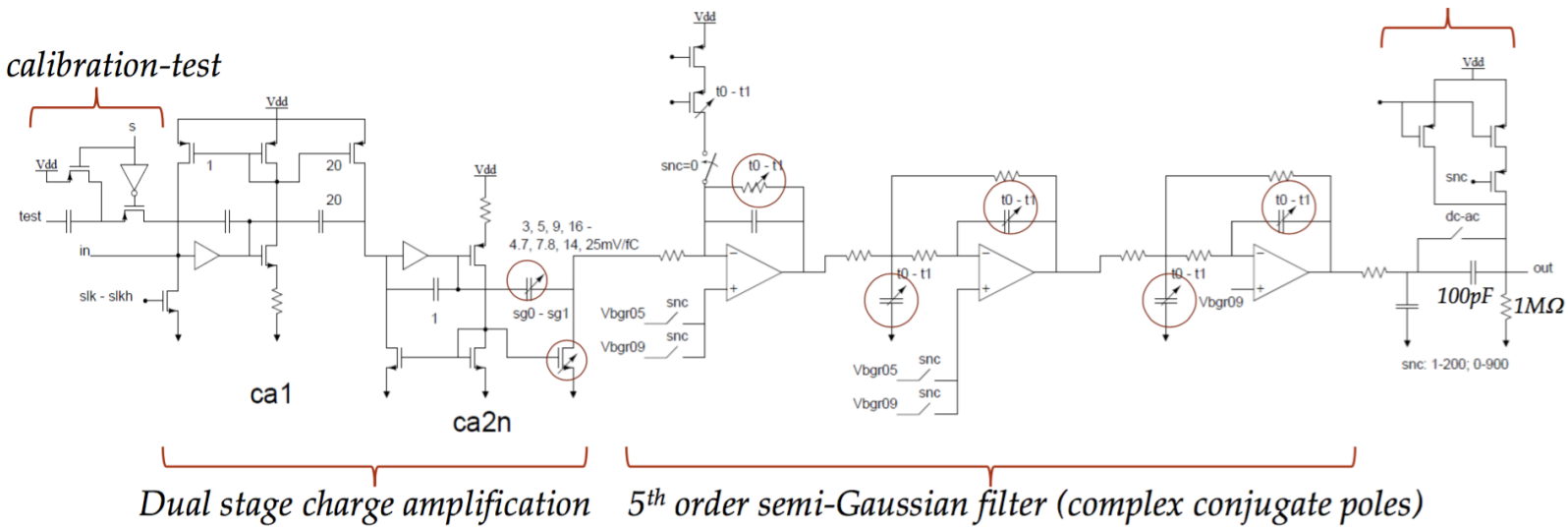
Hucheng Chen

BNL Front End ASIC (LArASIC)

- 16 channels
- 144 configuration registers, SPI interface
- CMOS 0.18 µm, 1.8 V
- Several Iterations

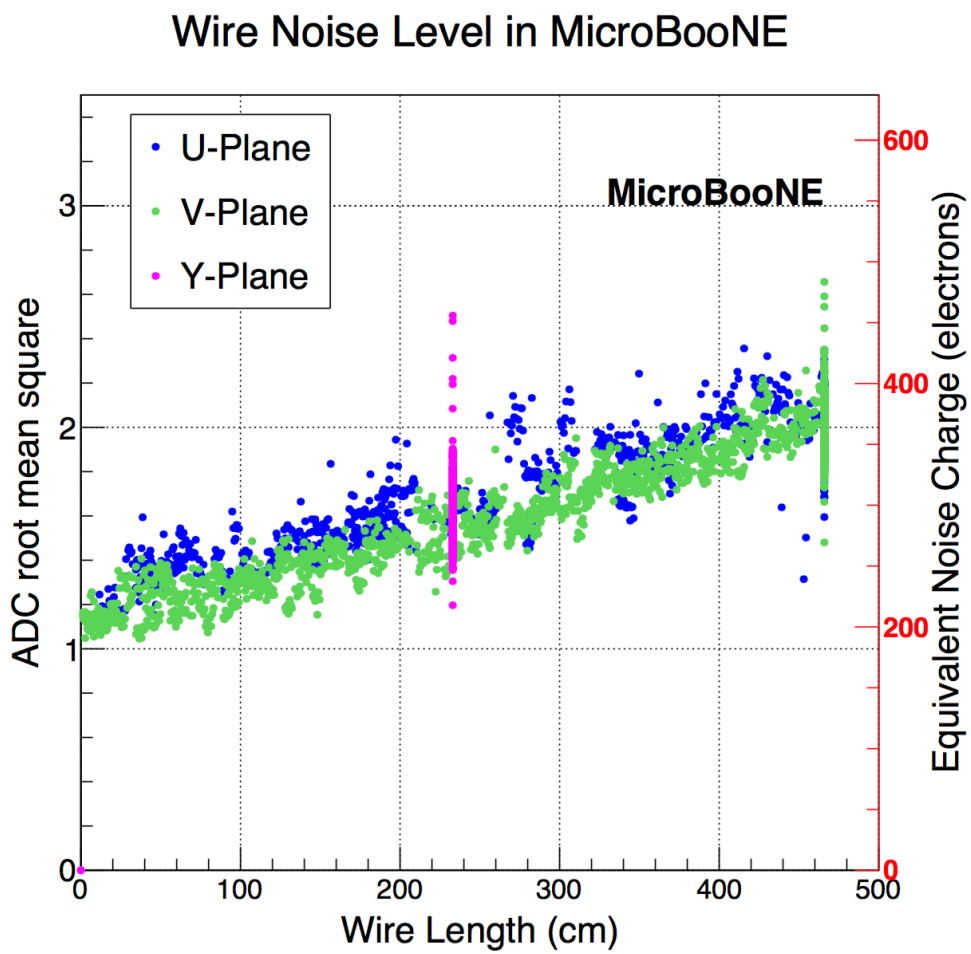


Channel schematic



MicroBooNE Noise Results

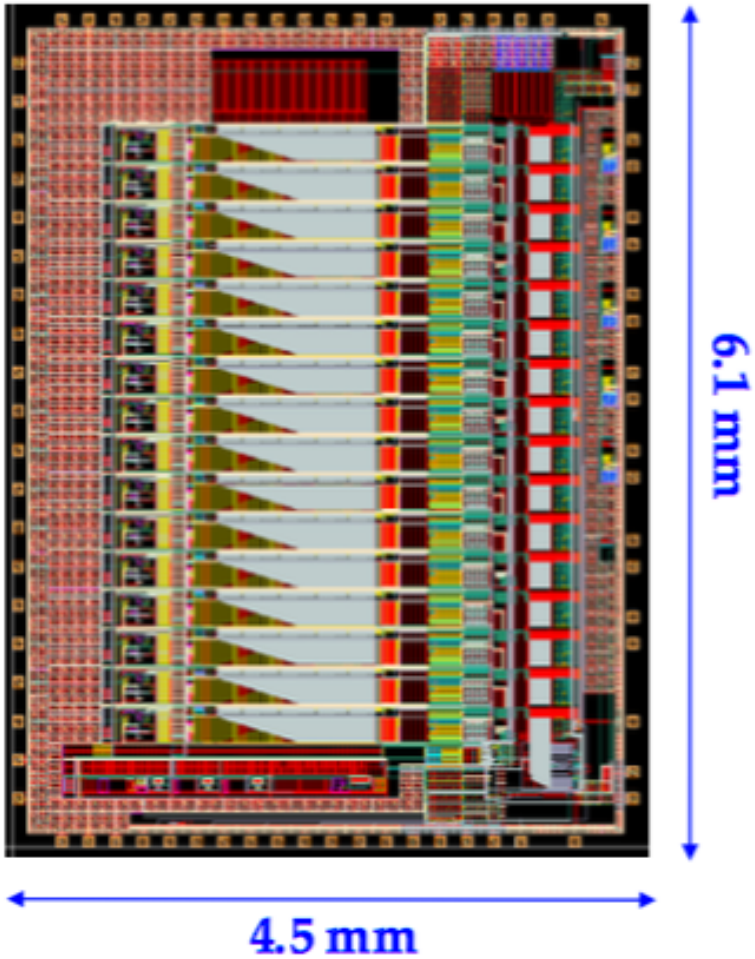
- MicroBooNE first large-scale use of BNL LArASIC
- After removal of coherent noise, excellent noise performance observed
- Wires of varying length confirm C_{det} dependence



MicroBooNE, JINST 12 P08003 (2017)

Existing Cold ADC

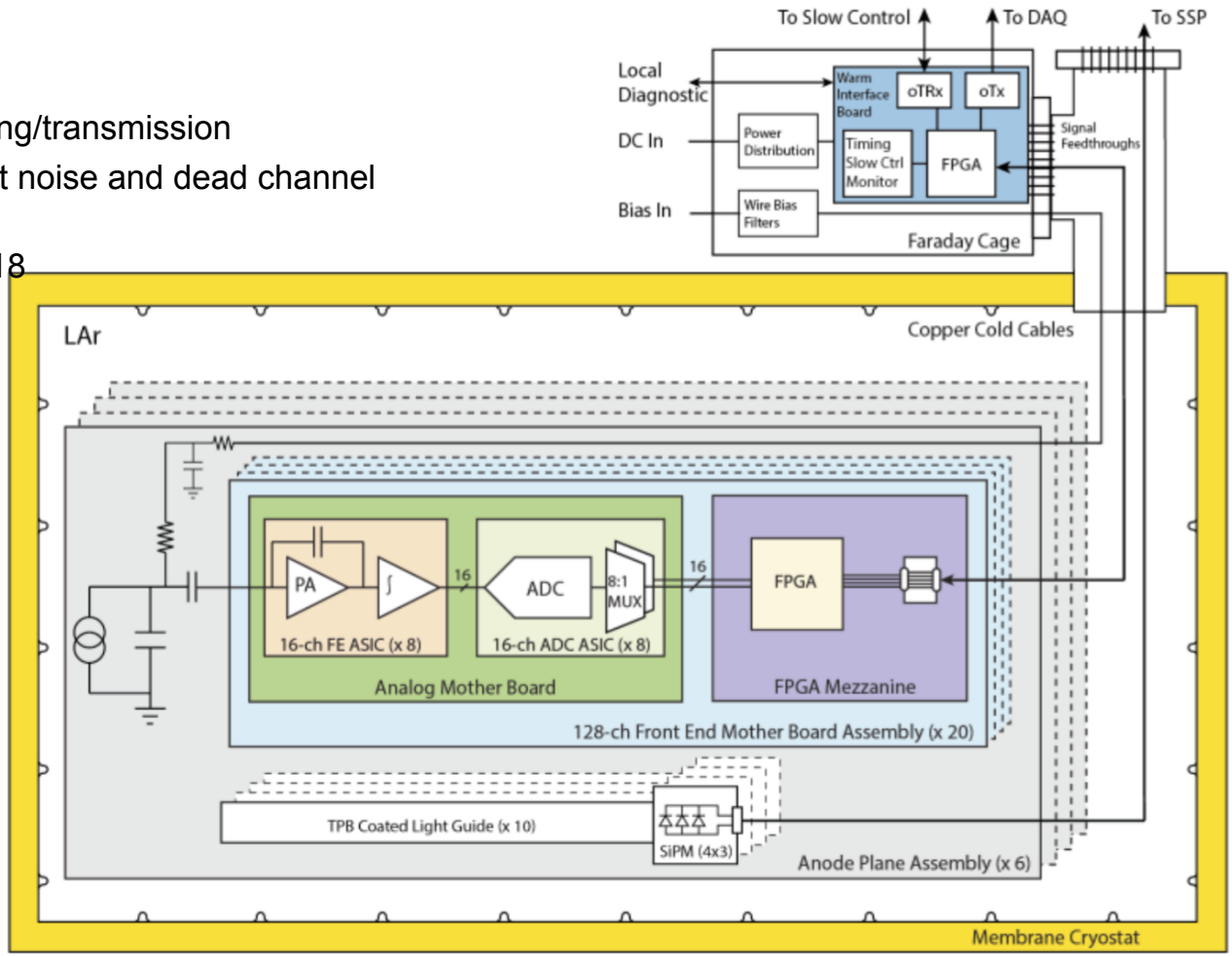
- DUNE requirements:
  - 12-bit
  - 2MS/s
  - Function at 293K and 87K
- BNL has developed a “domino” ADC that was used in ProtoDUNE-SP
- Active component matching proved problematic
  - Inadequate simulation model accuracy
- Development stopped in favor of:
  - Pipeline (LBNL/FNAL/BNL)
  - SAR (SLAC)
- Nonetheless, performed well in ProtoDUNE (with some known issues)



ProtoDUNE-SP Electronics

- Implementation of full cold electronics chain
  - BNL LArASIC
  - BNL Domino ADC
  - FPGA for multiplexing/transmission
- 15,360 channels: excellent noise and dead channel fraction
- Data taken Sep->Nov, 2018
- Results available soon

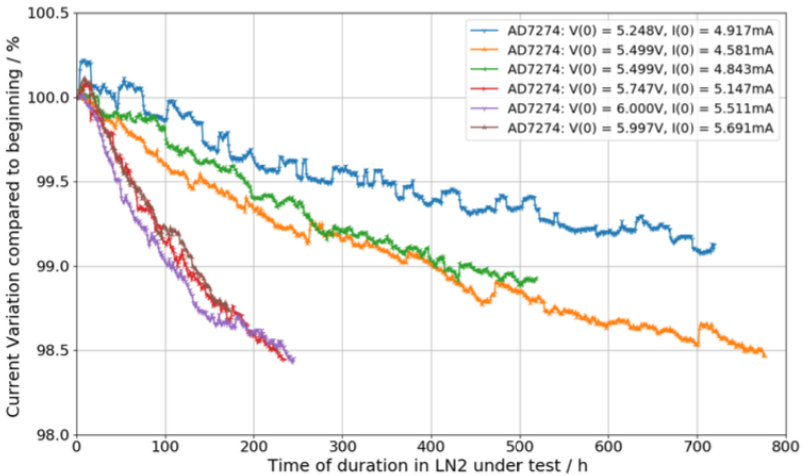
128 channel
Mother Board

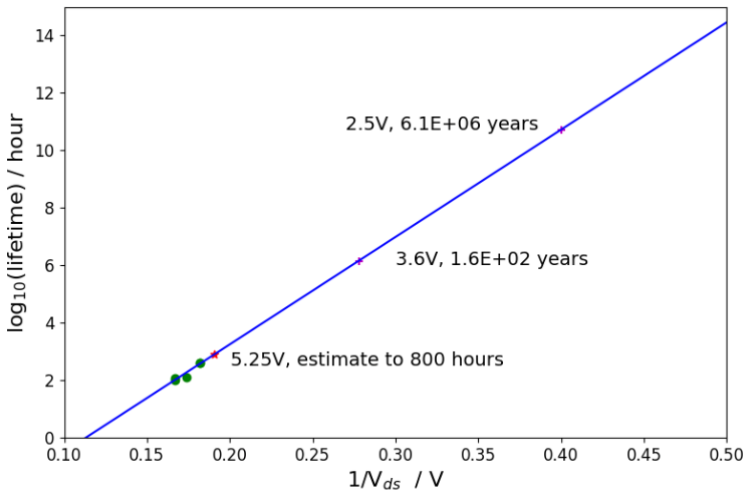


ProtoDUNE-SP TDR

SBND Approach

- New cold ADC not likely to be ready in time for SBND running
- COTS ADC (ADM7151) found to have adequate lifetime for SBND run





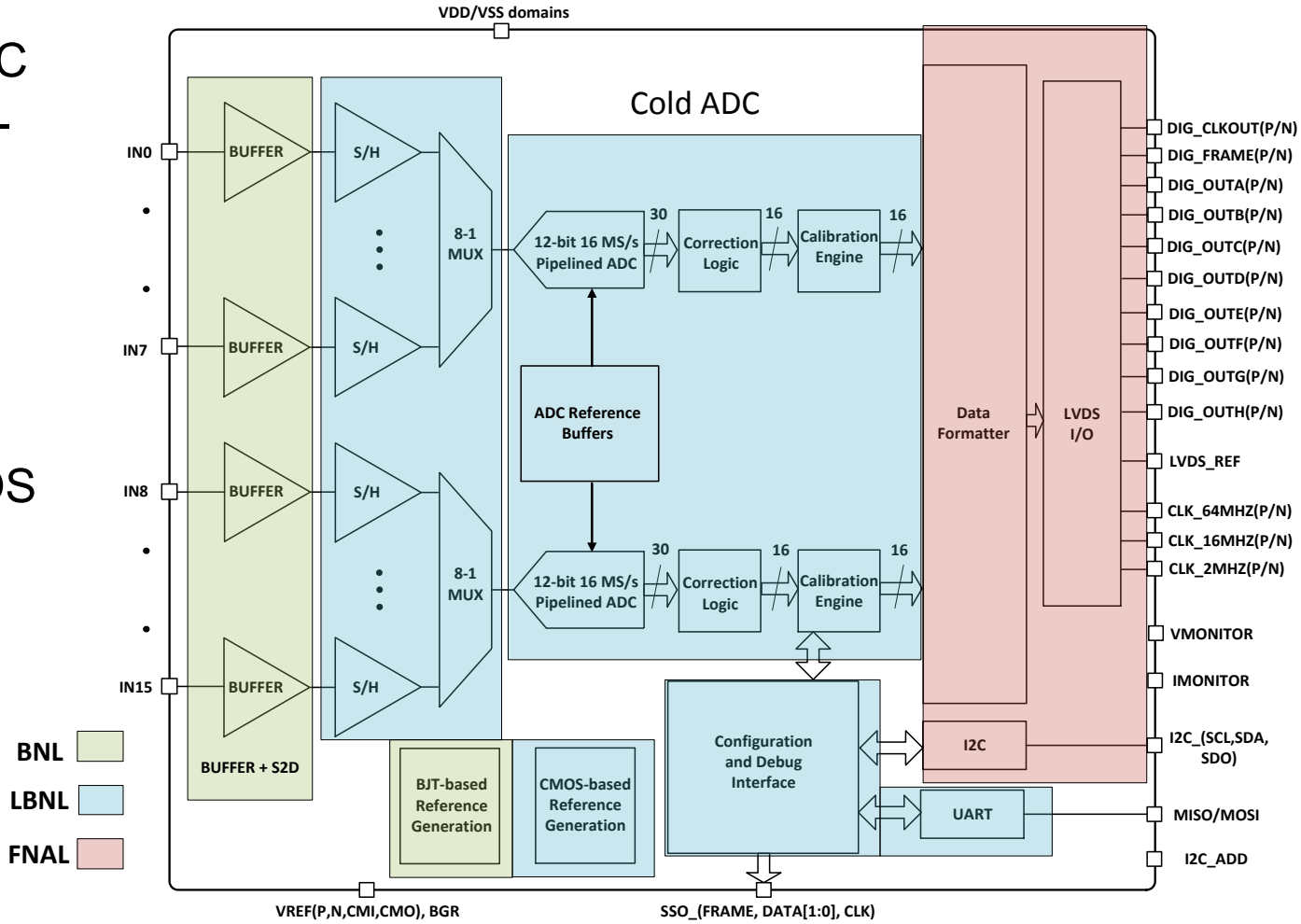
DUNE Development Plan

SLAC

- Continue “3-chip” solution development
  - Develop new ADC for “3-chip” solution:
    - LBNL/FNAL/BNL Collaboration. Pipeline-based ADC
    - First iteration submitted to foundry November 2018
  - Develop digital multiplexer/transmitter ASIC (COLDATA)
    - To be submitted early 2019
- Pursue alternative “all-in-one” solution: SLAC CRYO
  - Contains analog FE, ADC, multiplexer/transmitter
  - First iteration submitted November 2018
- Test both solutions in Spring/Summer 2019 (use cold FPGA for 3-chip) on:
  - ProtoDUNE Cold Box APA
  - Small TPC at FNAL (ICEBERG)
- Down-select in 2020

New Cold ADC (LBNL/FNAL/BNL)

- 16 channel ADC
- Linearity: +/- 0.5 LSB
- ENOB: 10.5 bits
- Input Range: 0-1.6V
- 0.065 μm CMOS
- Submitted November ’18



CRYO ASIC

- In 2017, SLAC began to design an "all-in-one" ASIC for nEXO
  - 64-channels
  - Analog front-end
  - ADC
  - Digital multiplexing and transmission
  - 0.13 μm TSMC
- Requirements almost identical to DUNE
- SLAC proposed a DUNE-specific version and joint development
  - Submitted to foundry November 2018
- Testing to begin in January 2019

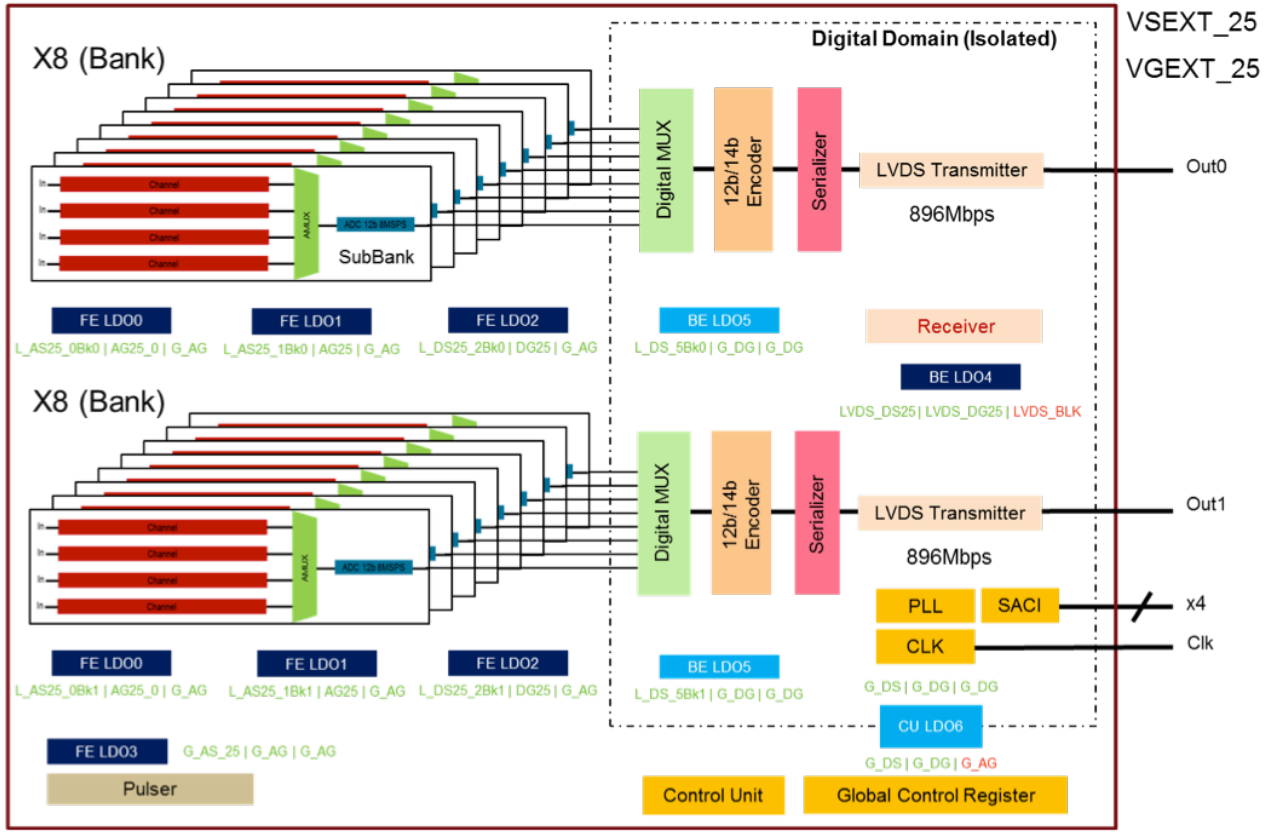
Requirements

	nEXO	DUNE
Analog BW	~500 kHz	~500 kHz
Sampling Freq.	2 MSPS	2 MSPS
Dynamic Range	12 bit	12 bit
Input Capacitance	15 pF	~220 pF
Temperature	165 K	87 K

DUNE CRYO Features

Anti-Alias Filter	Bessel 5th Order (P.T. 0.6us, 1.2us, 2.4us, 3.6us)
Multiple gains (max signal)	6X, 3X, 1.5X, 1X (50fC, 100fC, 200fC, 300fC)
Noise	ALARA (~500e- @ 3X, 1.2us)

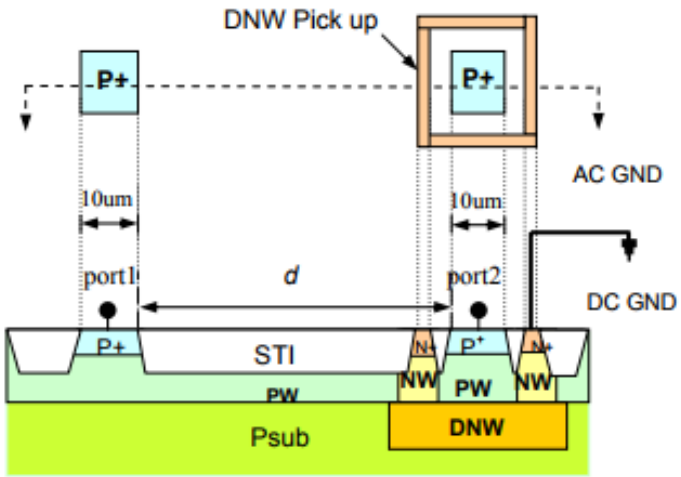
CRYO ASIC Architecture

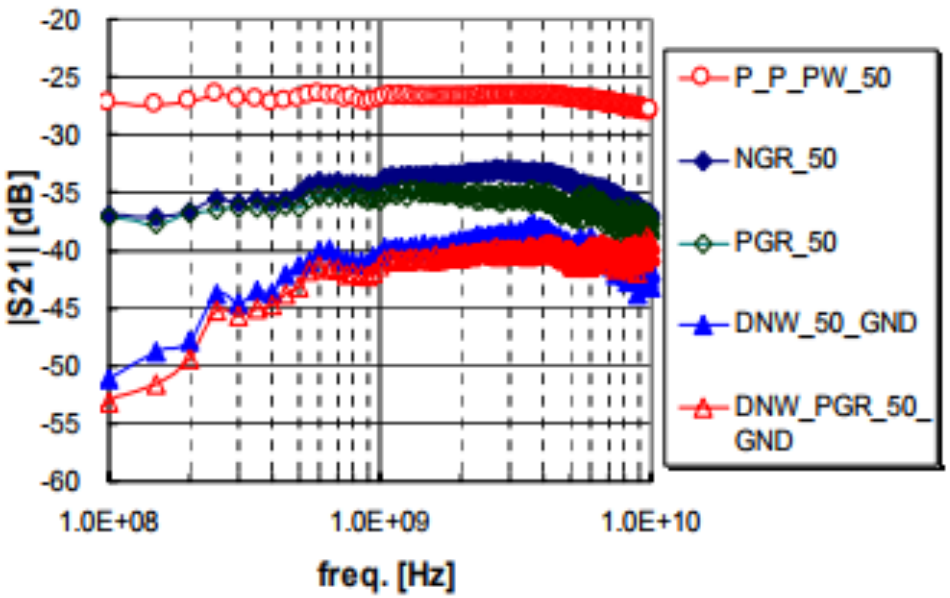


- Distributed supply regulation on-chip
- 4x1 multiplexing of channels into a single ADC with a dedicated LDO
- 8MSPS 12b SAR ADC (2 MSPS/ch)
- 12b/14b custom data encoding
- Serialization and LVDS data transmission at 896Mbps
- Digital domain isolated in DNW
- Dedicated slow control unit (SACI) an global registers to control functions and operative points (digitally assisted operation of analog sections)

Substrate Isolation: Key to combining digital and analog functionality

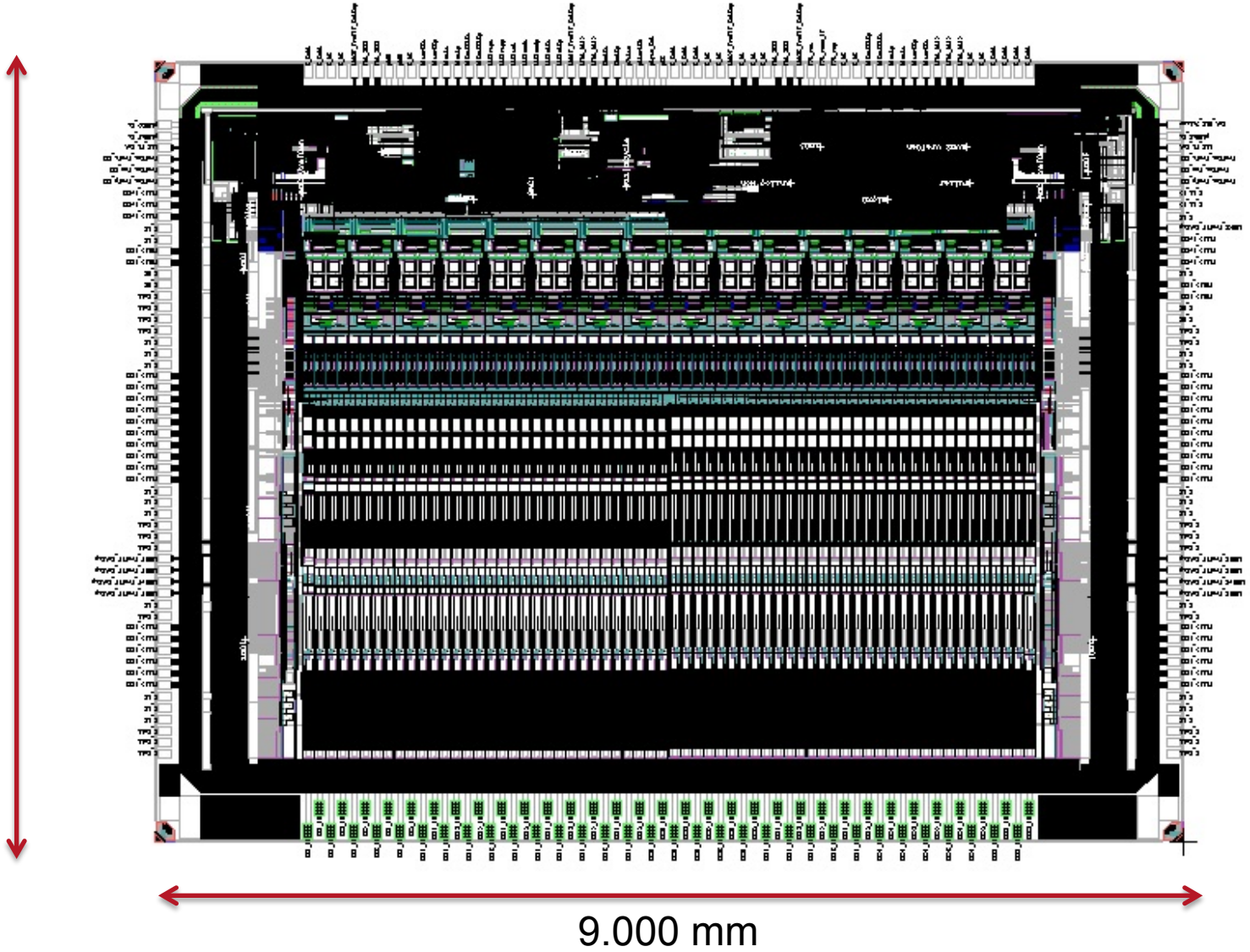
Approach tested in several designs





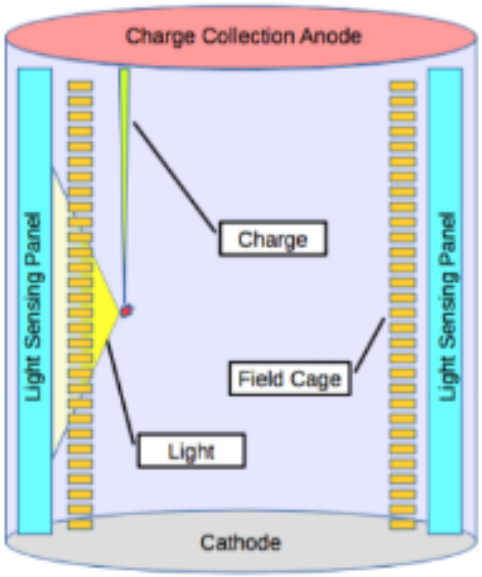
Wen-Kuan Yeh et al. Solid State Devices and Materials, Tokyo, 2003, - 408 - P1-5 pp. 408-409

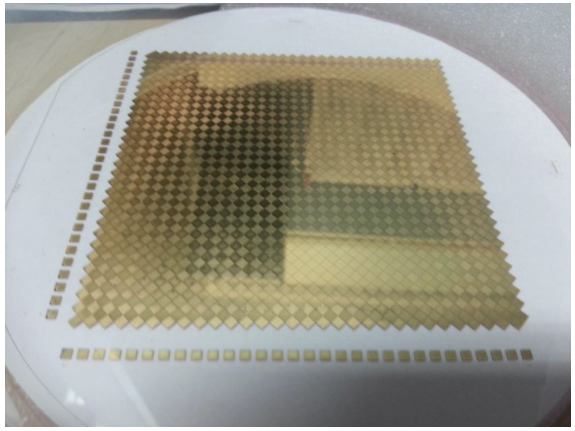
CRYO Layout



CRYO as Applied to nEXO

- Quartz Tile Size: 10 x 10 cm x 500 um with square pads
- Number of strips: 30 X strips and 30 Y strings
- Size of the strips: length ~ 10 cm diagonals of the square, 3 mm
- Capacitance of each strip to a group plane on the other side of the quartz tile, ~ 8 pF
- Capacitance of each strip to a single neighbor wire: ~ 0.2 pF
- Capacitance of each strip to all neighboring channels: ~ 6 pF
- Very similar requirements to LArTPC execpt:
  - Higher operation temperature (165 K)
  - Lower input capacitance (~14 pF)
  - Higher capacitance to neighbors (~6pF) – prone to crosstalk
  - Very strict radiopurity – no packaging
- Second version of CRYO with front end optimized for lower capacitance to be submitted in late 2019
- DUNE version of CRYO will be tested on nEXO teststand





CRYO Design/Simulations

CRYO design is well advanced

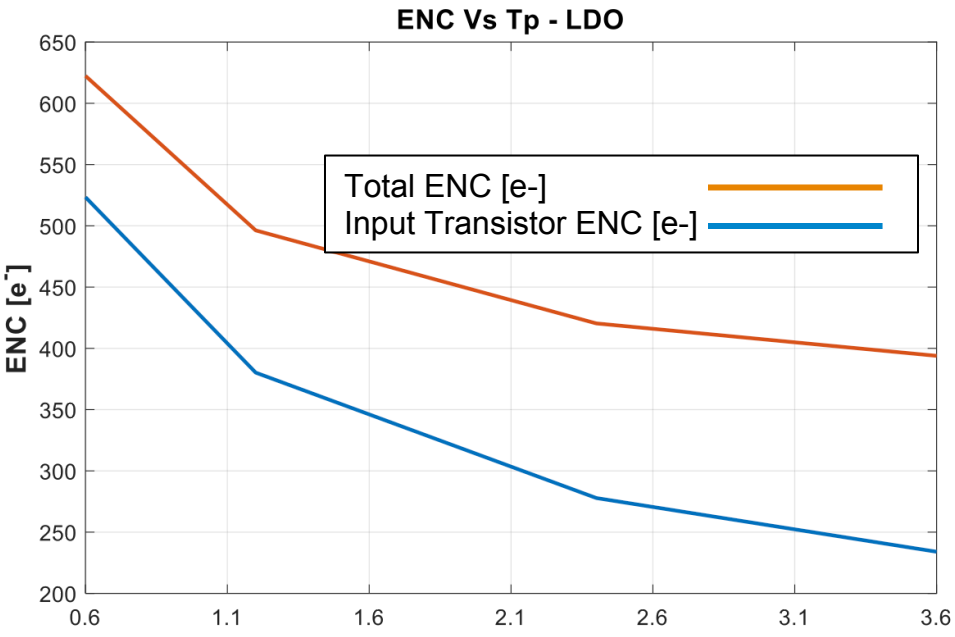
Simulations predict:

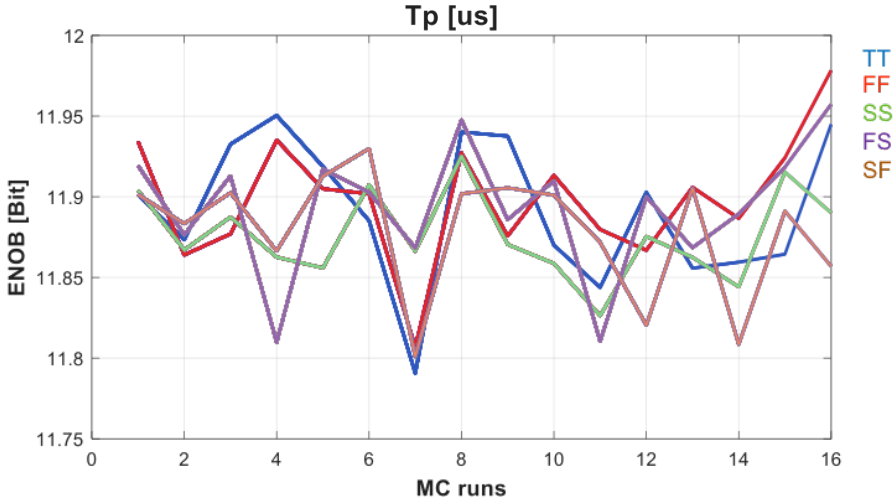
- Excellent front-end noise performance
- Excellent ADC ENOB performance even at the "corners" of transistor speed variation and component mismatch

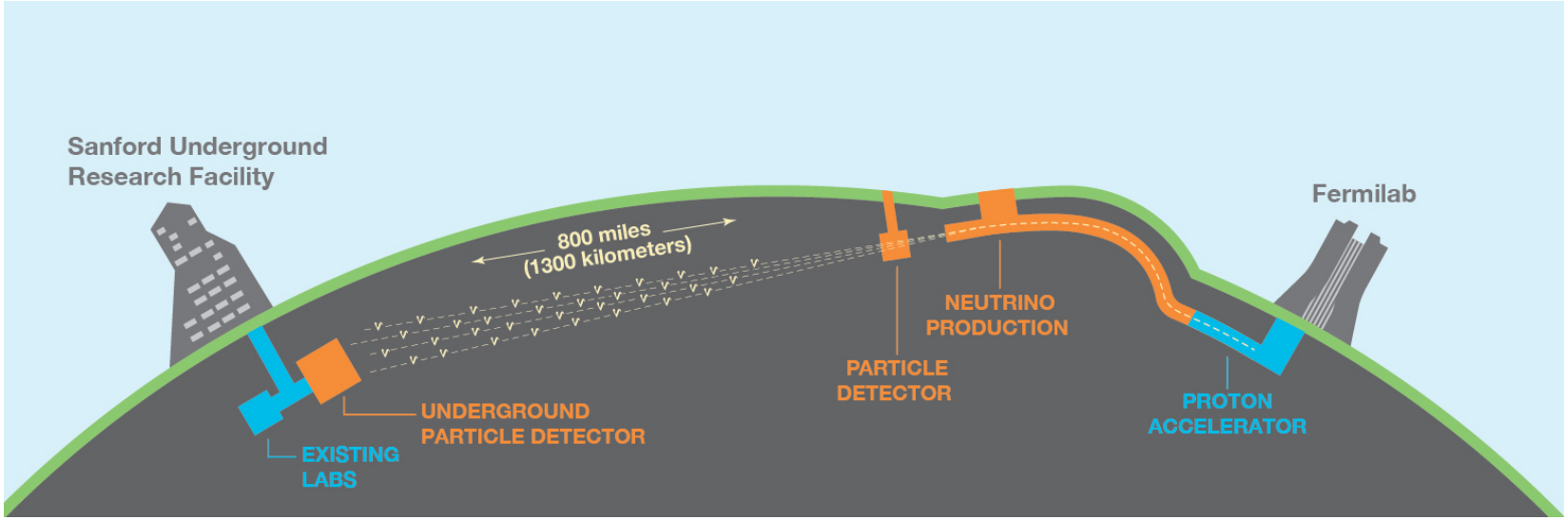
Expect first chips by January '19

CRYO Advantages

- Lower ASIC count (2 vs. 18)
- Simpler testing
- Likely higher reliability





Conclusions/Outlook

- Cold electronics is a key enabling technology of “giant” LArTPCs – 10kT scale likely not possible without it
- Analog front end has demonstrated excellent low noise performance in MicroBooNE
- Cold ADC has proven problematic. But,
  - Good performance of existing ASIC in ProtoDUNE-SP
  - New ADC under design
  - COTS option also a possibility
- CRYO “all-in-one” option has a number of nice features that make it a good option for DUNE
- The next two years will be an exciting time for finalizing the DUNE Cold Electronics