Trigger & clock distribution

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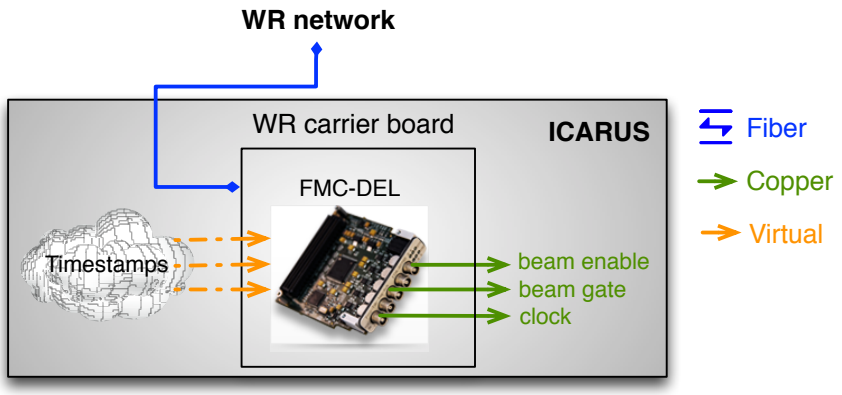
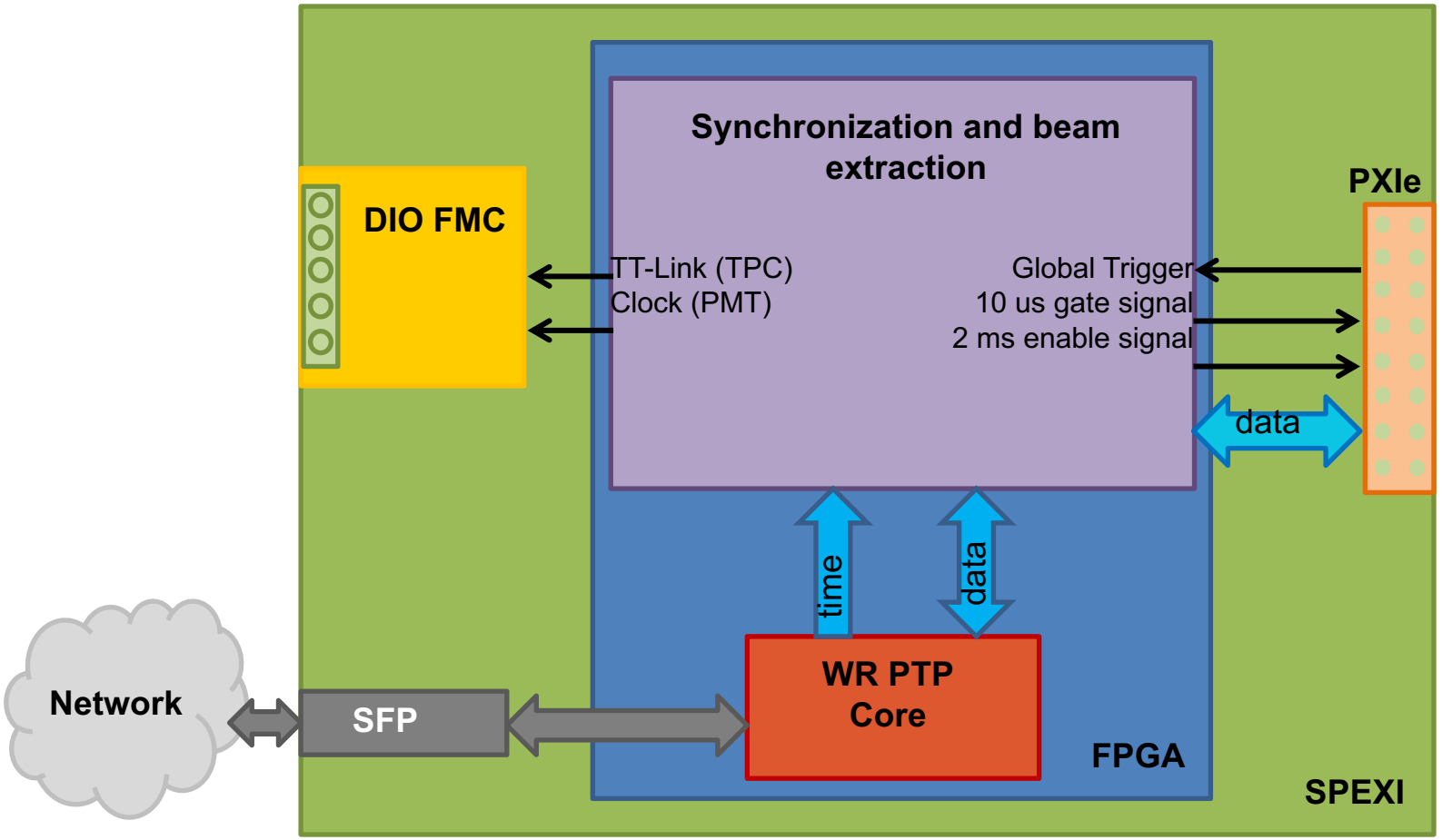
Distribution of clock and beam signals in ICARUS

- One functionality in the ICARUS DAQ will be devoted to decode timing and beam information received through White Rabbit network and generate clocks for the front-end electronics and beam gates for triggering:



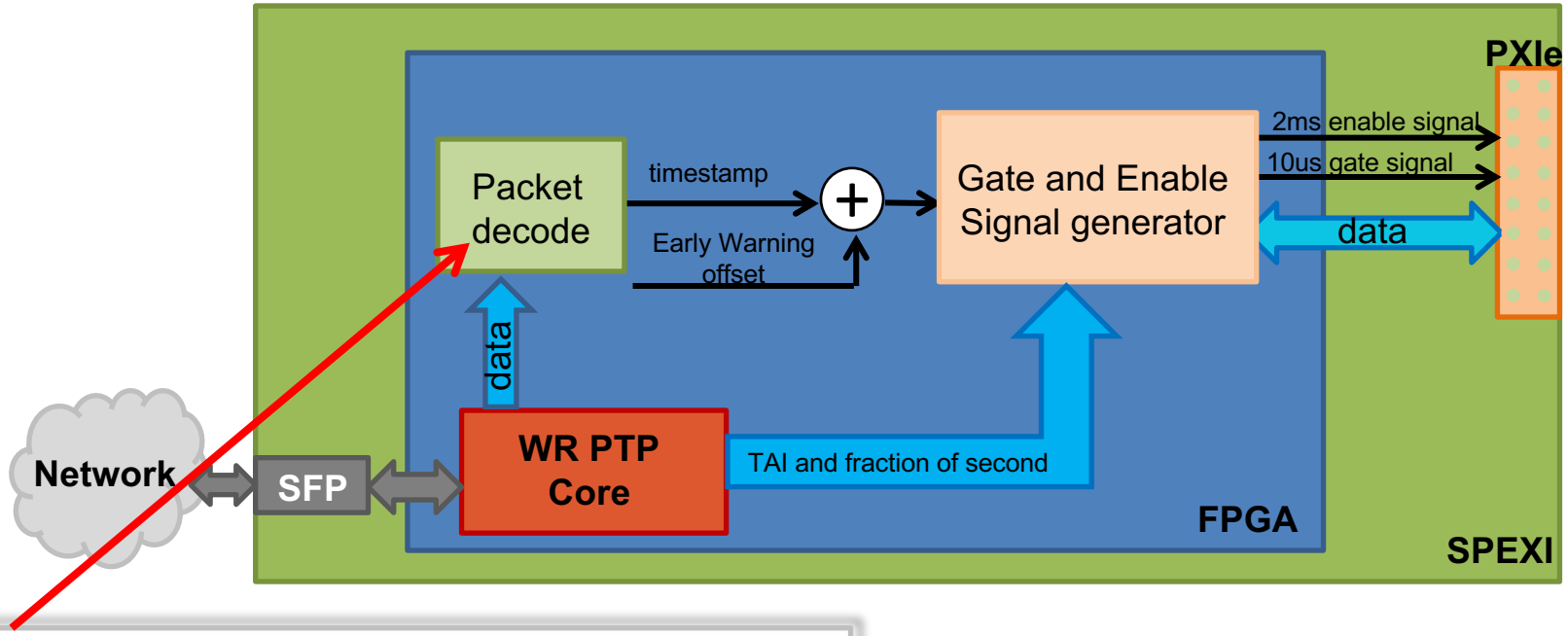
  - ✓ 50 MHz clock for the PMT digitizers;
  - ✓ signal to reset the internal counter of the PMT digitizers used for the local time-stamping of the trigger;
  - ✓ TT-Link signal required by the wires digitizers, i.e. the single wire serial bus 10 MHz communication encoding clock, trigger and run commands;
  - ✓ 2 ms wide beam enable signals (1 ms before the 10 μs gate signal), both for BNB and NuMI, for activating the PMT readout;
  - ✓ 10 μs wide beam gate signals, both for BNB and NuMI, in which to look for a PMT-Trigger in order to generate the Global Trigger for the wires readout.
- This is being implemented in a FPGA (Field Programmable Gate Array) in one PXIe board (SPEXI) in the National Instrument crate used for trigger.

ICARUS SPEXI Board Block Diagram



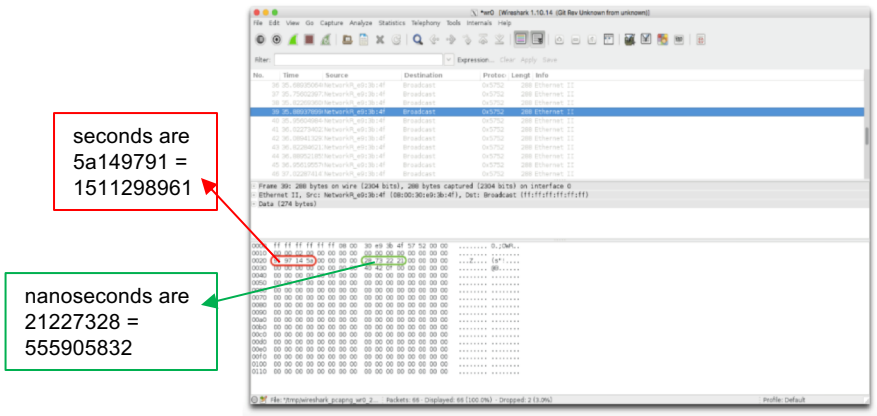
Acronyms
SPEXI : Simple PXI express FMC Carrier Board
DIO FMC : Digital Input/Output FPGA Mezzanine Card
WR PTP : White Rabbit Precision Time Protocol
PXIe : PCI extension for instrumentation
SFP : Small Form-factor Pluggable

Beam Extraction



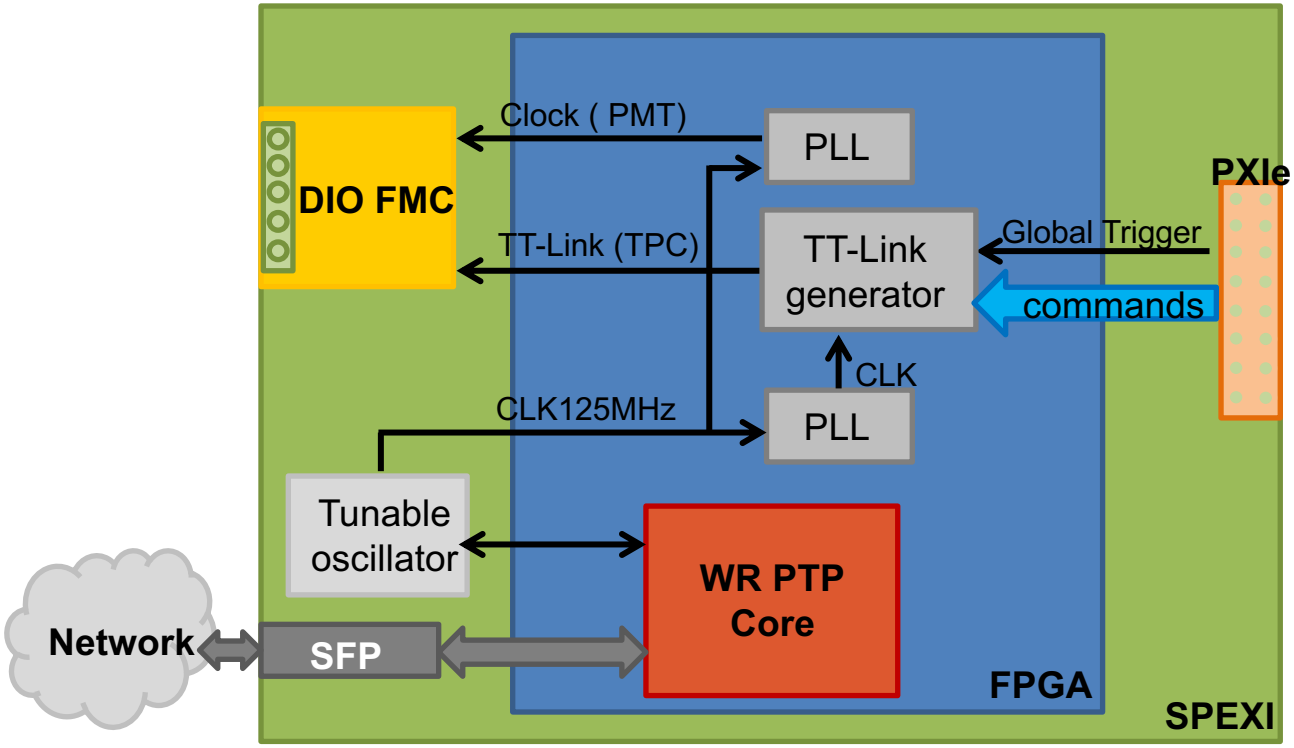
Structure of the time-stamp packet sent with WR-NIC

36 words, 8 bytes each, (64-bit arch):
-- the 4 less significative bytes of word number 5 are the seconds;
-- the 4 less significative bytes of word number 6 are the nanoseconds;
Bits ordering is swapped.

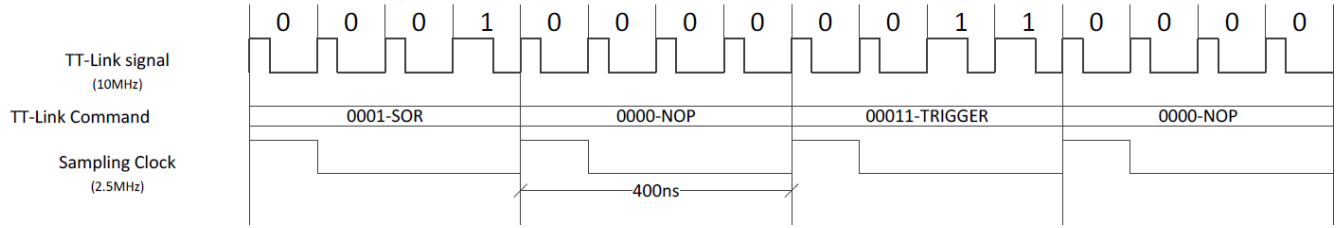


- The packet information is obtained from the screenshot provided by FNAL.
- The timestamp is 40 bit TAI and 28 bit fraction of each second (resolution of 8 ns) .
- SPEXI FPGA decodes received packet, adds Early Warning offset, generates the gate and enable signals when the beam arrives.

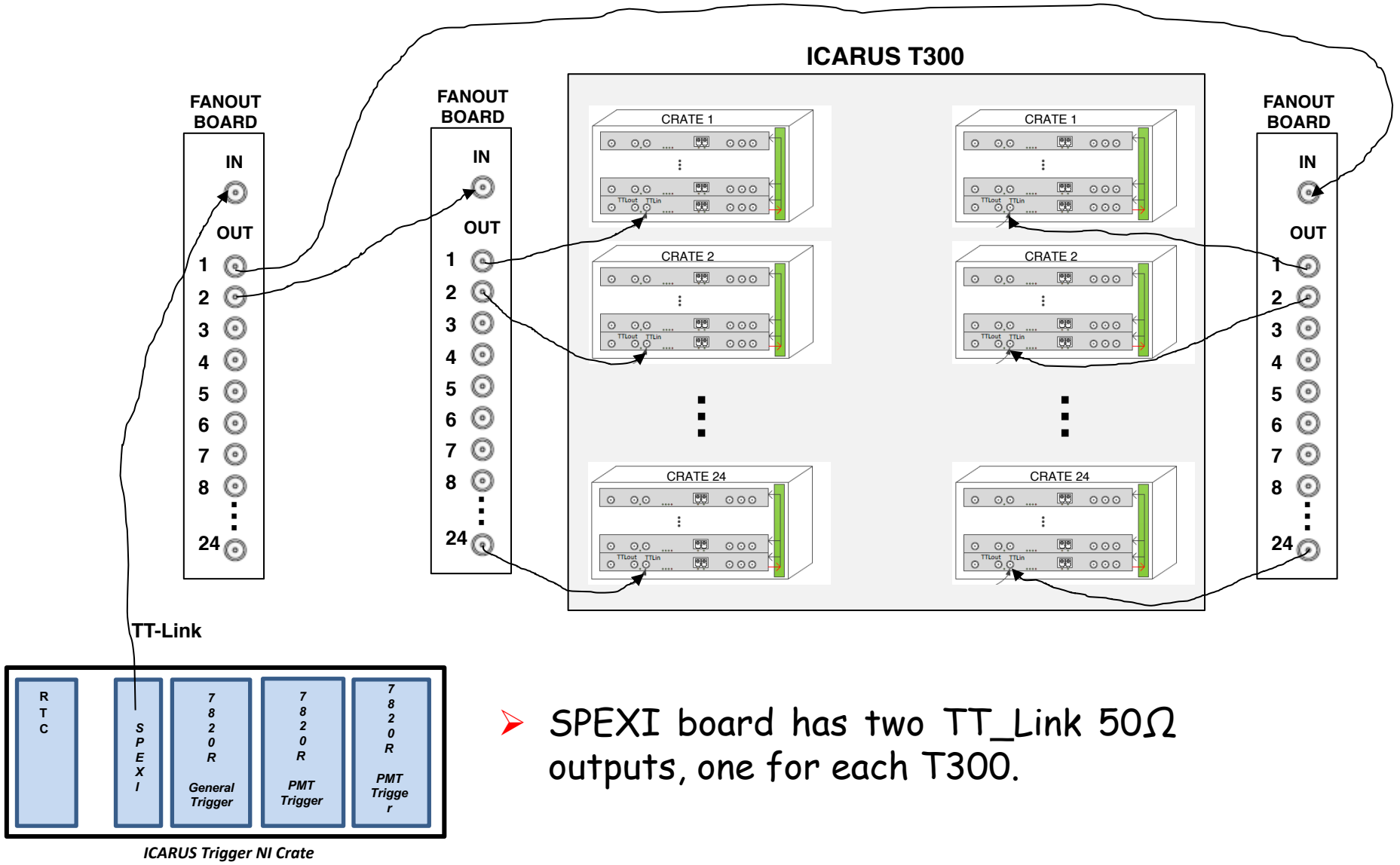
TT-Link and clock generation



- The TT-Link (Timing and Trigger Link) is used to distribute the sampling clock and a set of real time commands to all the TPC readout electronics boards (A2795).
- TT-Link input on the board: LEMO connector, TTL standard, Zin=50Ω.



TT-Link Connections



- SPEXI board has two TT_Link 50Ω outputs, one for each T300.

Development status & perspectives

- One operative SPEXI board and one DIO FMC are available in Pavia.
- One NI crate, complete with CPU, is available in Pavia.
  A second one can be temporarily loaned at Fermilab.
- The firmware of the SPEXI board has been prepared by Padova group.
- The Labview software is being developed by Pavia group.
- Tests to be done.
  1) Verification of the functionalities of both firmware and LabVIEW program _ at CERN.
  2) Synchronization of the SPEXI board, as slave node, with the White Rabbit network and verification of clock generation _ at Fermilab.
  3) Reception of early warning information and verification of proper decoding and gate opening _ at Fermilab.