DUNE Cold Electronics For Single Phase TPC Far Detector

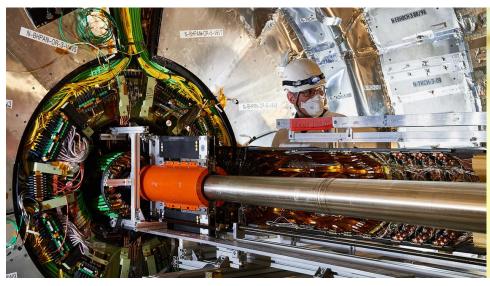
Marco Verzocchi - Fermilab Pixel LArTPC Workshop 29 September 2018

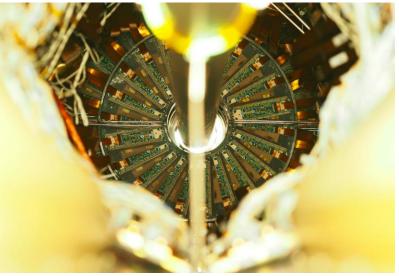




Some Background

- I am the technical lead for the DUNE CE consortium / L2 manager for this part of the US project
- I am talking at this workshop in a personal capacity
- I have joined DUNE / started working on the Cold Electronics one year ago
- I am presenting work done by others (mostly protoDUNE)
- I have worked from 2013 until 2017 on the CMS Phase 1 Pixel Upgrade







09.29.18

What is my charge for this talk?

- "I think it would be very valuable to have the perspective from the DUNE Cold Electronics Consortium presented. In particular, an overview of the DUNE FD Cold Electronics schedule and overall plan could be enlightening. "
- I will take this as
 - Remind people that the development of a complete electronic readout chain takes time
 - Remind people of the kind of tests you need to do to ensure that the detector you put inside a LAr cryostat can live for 20 (?) years
 - Provide some background on how long it takes to actually build a detector once you get out of the R&D phase
 - I will provide some minimal cost information





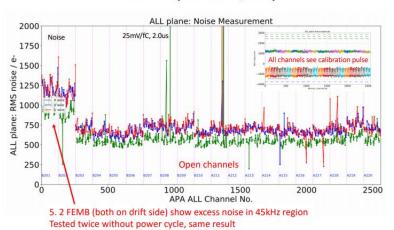
Developing a custom readout chain (i)

- R&D of CMOS cold electronics started in 2008 at BNL
 - The cold electronics development for LAr TPCs was launched, before the final decision for LAr TPC for LBNF/DUNE had been made in Jan 2012
 - microBooNE started with plans for JFET's, then adopted the cryogenic CMOS analog front end ASIC developed for LBNF/DUNE LAr TPC program
- Multiple generations of Front-End ASICs developed (and used) for microBooNE, other LAr prototypes, protoDUNE, DUNE

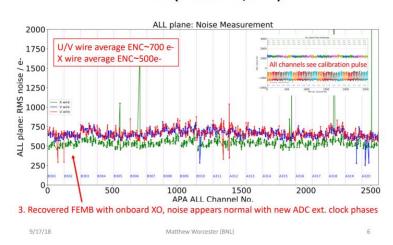


It Works

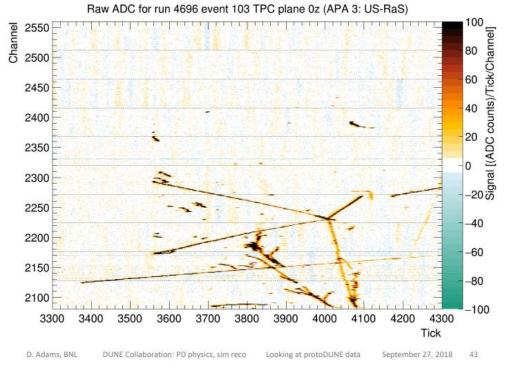
APA2 (from 9/13)



APA3 (from 9/13)



All the people who have worked on the LAr concept(s) for years and on protoDUNE deserve a lot of credit for these plots







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Developing a custom readout chain (ii)

- First cold ADC developed at BNL (used in protoDUNE) has multiple issues
 - Chosen architecture too sensitive to variations in properties of components
 - Inaccurate simulation model for cold temperature
- Second generation of ASICs (new Cold ADC pipeline architecture by BNL+FNAL+LBNL, new SAR ADC developed at BNL, 3-in-1 CRYO developed at BNL)
 - Use libraries of CMOS components (65 and 130 nm) that have been measured at cryogenic temperatures
 - Roughly 1 year to go from concept to tape-out



Will it work? When will you know?

- ~1 year to go from concept to tape out
 - Some developments limited by availability of ASIC engineers
 - Following iterations will be faster
- 3 months to get ASICs back
- Initial testing by ASIC engineers that have designed the chips
- Package ASICs, calibrate, mount on FEMBs, test FEMBs
- Proceed to system tests
 - Mount FEMBs on APAs (40% APA prototype at BNL, protoDUNE APA in CERN cold box, new small TPC at Fermilab)
- Almost 2 years from beginning to end of 1st iteration
- Proceed in parallel with design of 2nd iteration
- Second submission only when full set of results from system tests available





Will it (continue to) work in 2045?

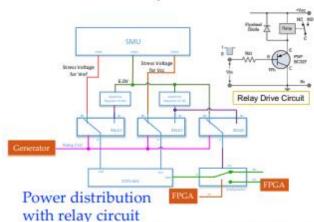
- The detector parts inside the cryostat need to survive for 20-30 years with a minimal loss of channels (few %)
- Experience (NA48, ATLAS) shows that once the detector components are immersed in the cryogenic liquid things are very stable
- Mechanism for performance degradation for CMOS components well understood (measurements performed) and addressed in design of ASICs
- Need to demonstrate that final ASICs have a lifetime >> 30 years (even if this has already been done at the individual transistor level)
 - Already done for COTS ADC used for SBND
 - Plan to repeat these studies for all new ASICs and other components to be installed in the liquid





Lifetime tests of COTS ADC (SBND)

Development of Test Stand





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- The test stand shown in previous slide has been used in exploratory phase to study COTS ADC lifetime from September to December 2017
 - It took some effort to develop and optimize the test stand for COTS ADC lifetime study
- A new COTS ADC test board has been designed for ADC lifetime study in validation phase
 - Analog switch: NLASB3157 (used on FM)
 - Clock fan-out: CDCV304 (used on AM)
 - Add series termination resistors for ADC SPI signals
 - Support stress voltages up to 6V with level translator qualified for cold operation
 - Fully automatic data taking with only manual intervention of LN2 filling
- New COTS ADC test boards are used to study ADC lifetime in validation phase at both BNL and Manchester

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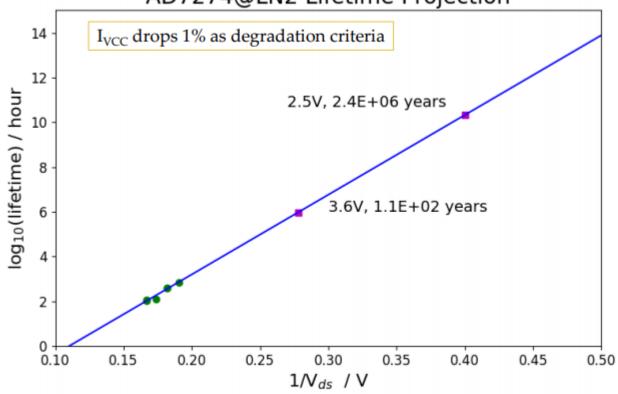


2018/07/16

Lifetime tests of COTS ADC (SBND)

ADC Lifetime Projection





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It's not just the ASICs

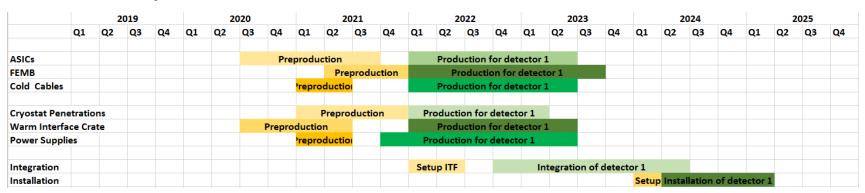
- System design is a crucial part of keeping the noise in the detector at a low level (pixel detectors have a clear advantage here)
- Other components of the detector represent a significant fraction of the cost (example for DUNE-SP ASICs are just 10% of the overall M&S cost)
 - Power supplies: could one go with cheaper (i.e. less stable) power supplies for pixel based detector?
 - Cold cables: for SP transmitting data at 1.28-2.56 Gbit/s on cold cables, lower speed requirement for pixel based detector could lead to significant savings
 - Interface to DAQ: warm interface electronics crate could also be simpler
 - Cryostat penetrations: could be significantly more complicated (serialize the data in the chimney ?)
- Need to design the whole system to carefully estimate costs





Construction Schedule

This is a possible DUNE-SP construction schedule



- It is NOT the official DUNE-SP construction schedule (availability of funding, approvals)
- It gives a reasonable timeline for the time it takes to build the components, test them, integrate them on the APAs, install everything in the cryostat
 - Filling with LAr and commissioning not included
- Several years of R&D plus 4-5 years of construction, integration and installation





Conclusions

- "In just seven days I can make you a man"
 - (Frank-n-Furter, Rocky Horror Picture Show)
- The development of LArPix so far has been impressive, but expanding this to the size of the near detector or a full far detector cryostat will take time, personnel and resources
- Building a 4th detector with the LArPix detector seems feasible

