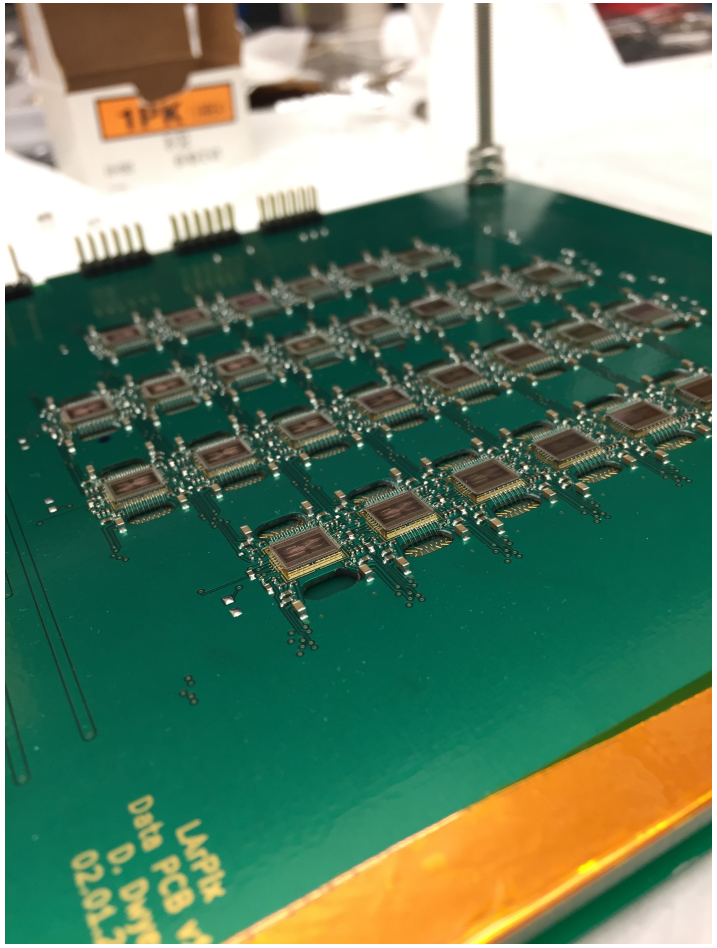
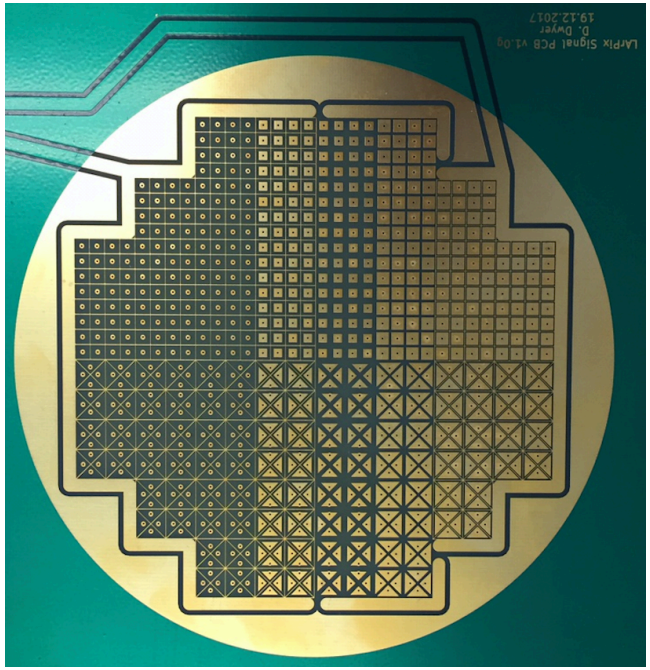
# LArPix:
# Status and Plan

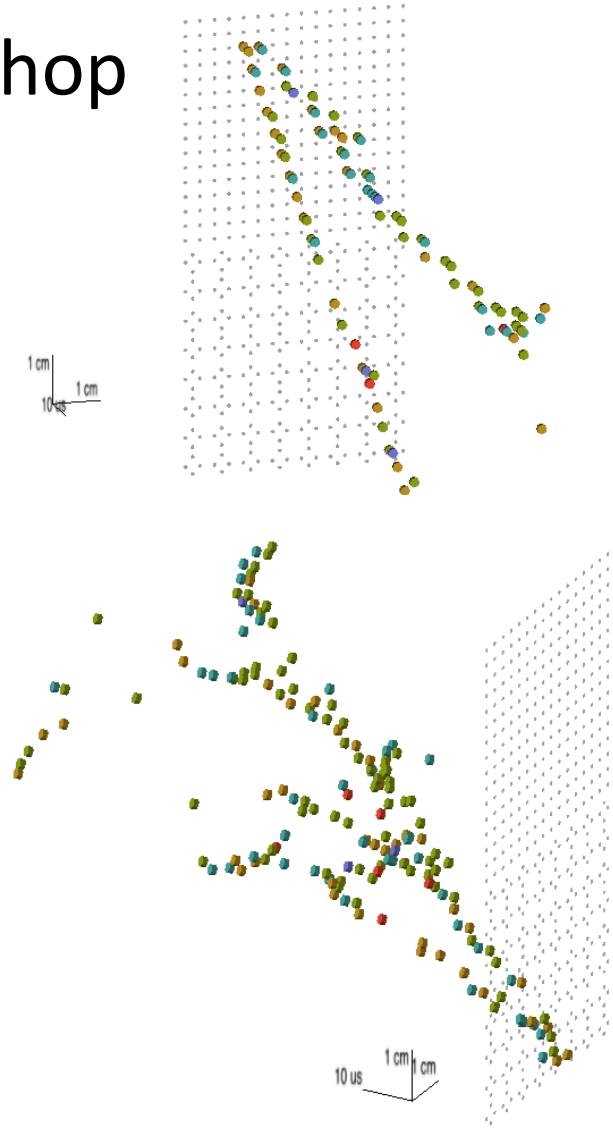
Dan Dwyer (LBNL)

Pixel LArTPC Autumn Workshop

Sep. 29, 2018

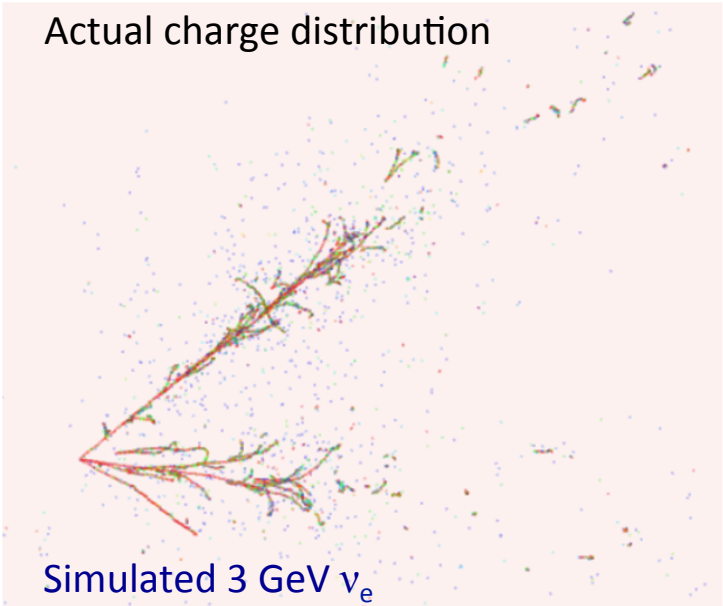


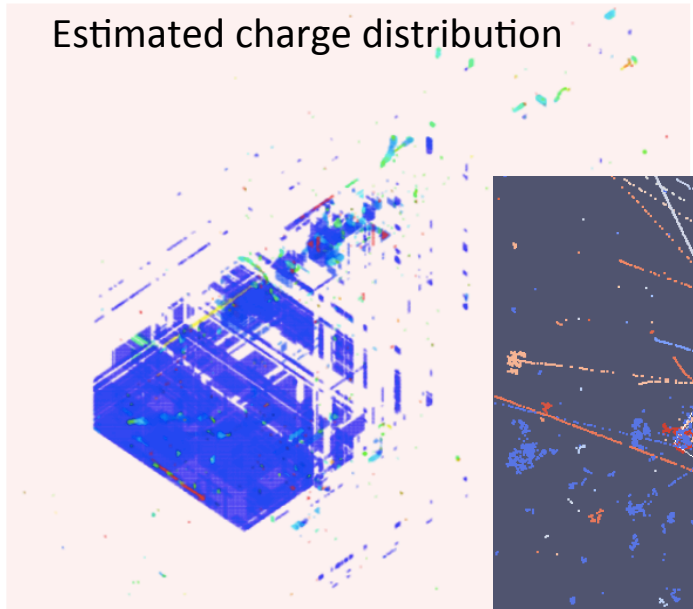




# 3D LArTPC

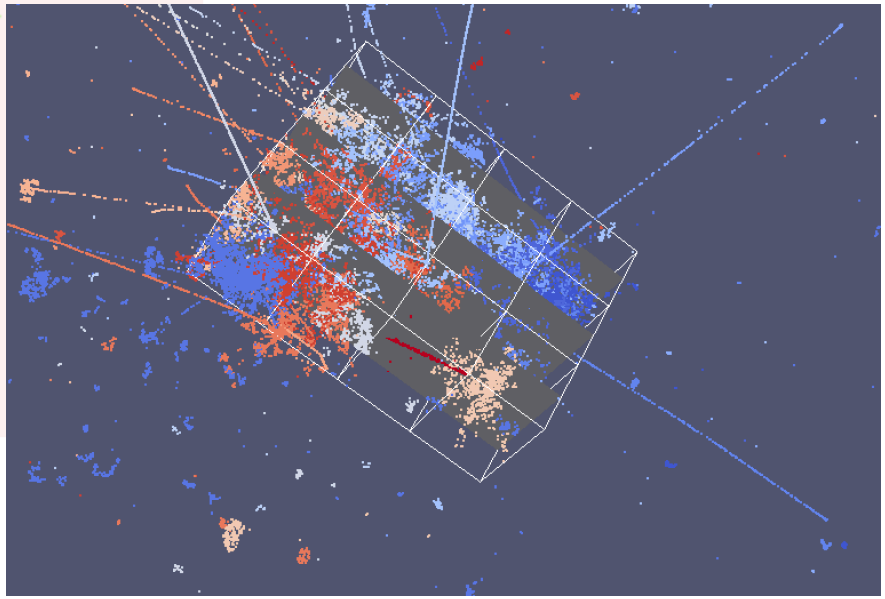
## Ambiguities in projective wire readout:




## DUNE Near LArTPC:

High neutrino rate exacerbates ambiguities.



*Example neutrino signals from one LBNF spill*

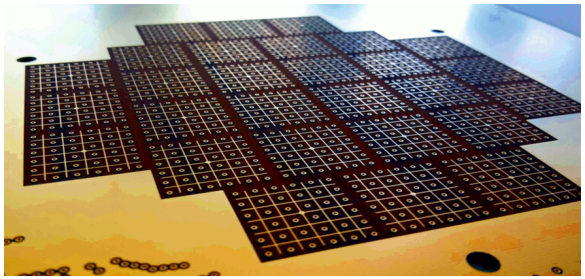
## Pixel Readout Development

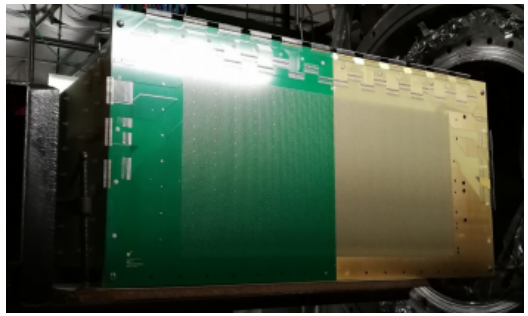
Demonstration of pixel sensor feasibility (Bern/ArgonCube)

Progress with in-beam tests (PixLAr)

→ Low-power pixel electronics (LBNL)

ArgonCube





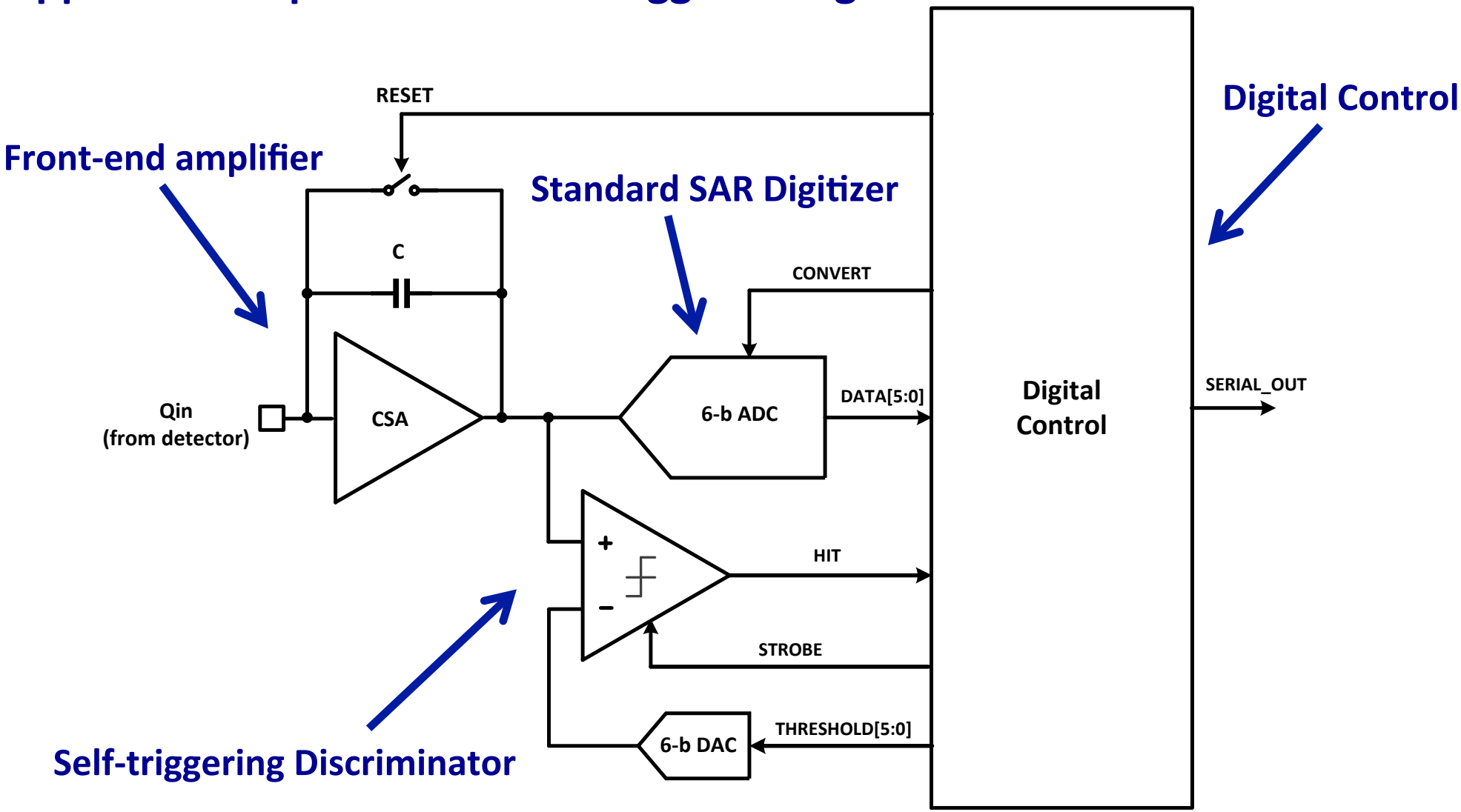
PIXLAR

A LArIAT production

# LArPix-v1 Design

**True 3D readout: A dedicated front-end channel for every pixel**

**Approach: Amplifier with Self-triggered Digitization and Readout**




*Achieve low power: avoid digitization and readout of mostly quiescent data.*

# LArPix v1: Design for Testability

## Incomplete list of testing features

**Front end:**

- contains programmable test pulse generator
- output of any channel can be routed to analog monitor bus
- can be bypassed so ADC performance can be evaluated independently
- has multiple reset modes: self-reset (post-digitization), periodic reset (adjustable, 200 ns to 3 s)

**ADC:**

- can execute programmable number of ADC conversions before reset issued
- has programmable ability to allow more time for front end to settle

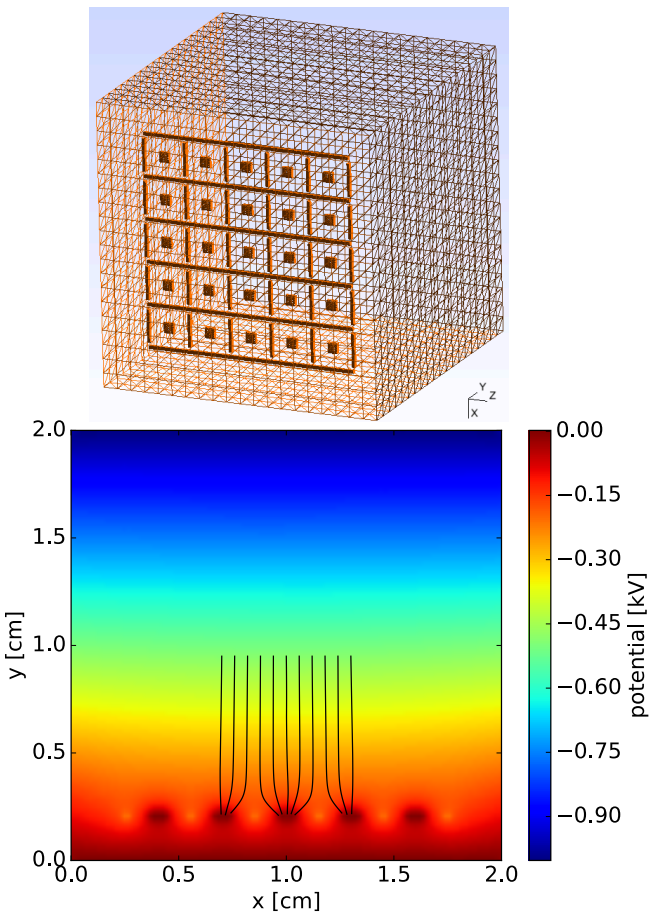
**Digital core:**

- allows any number of channels to be disabled
- allows any number of channels to be externally triggered
- operates on different power supply from analog front end
    - power reduction can be explored using low-voltage digital
- has multiple reset methods: soft reset (through configuration interface), hard reset (pin toggle)
- has multiple FIFO test modes:
    - configuration interface sends out known patterns, exercises FIFO memory
    - FIFO is put into overflow condition to check impact on system performance
- has FIFO monitoring: half-full and overflow flags, explicit mode for tracking FIFO depth

# Close Dialog with Physics

## Developed a set of tools to assess TPC readout design

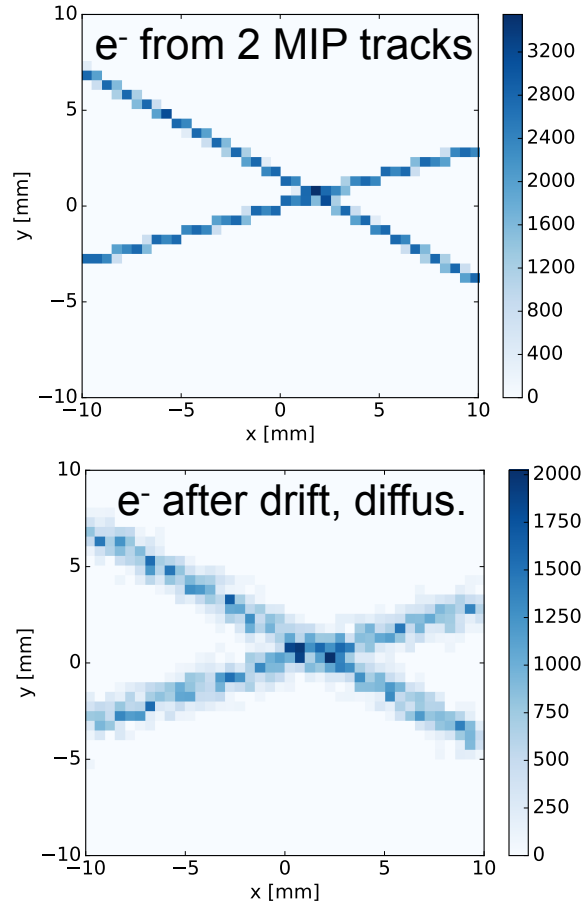
### Sensor model in 3D



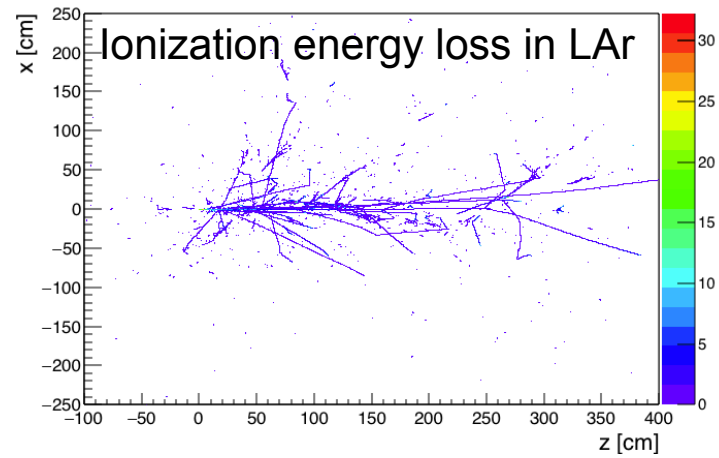

### 3D drift field, pix response

→ *Thanks to B. Viren for intro to BEM tools*

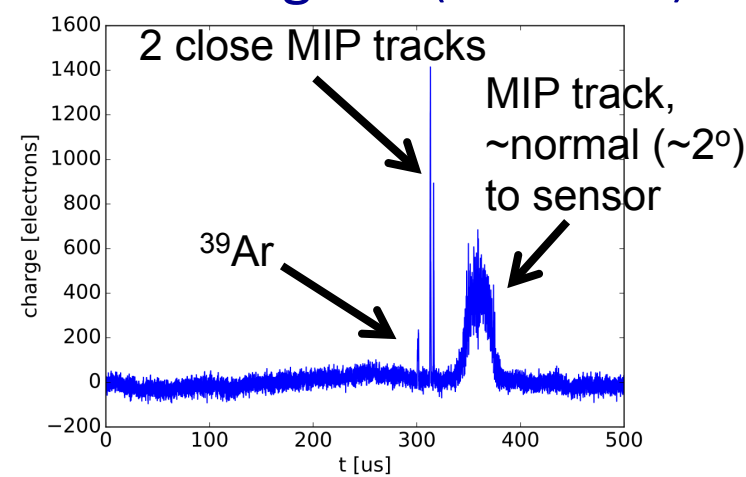
### Ionization, recomb., drift loss, diffusion




### Fast primitive Geant4 sim.




### Realistic signals (with noise)




**Signals have been input to IC modeling program (Spice, Cadence) to assess IC design, performance.**

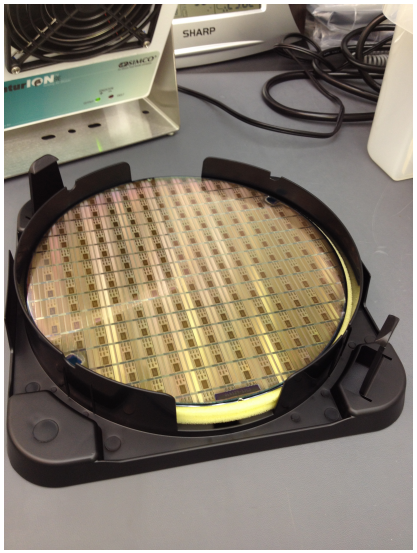
# LArPix-v1 Progress

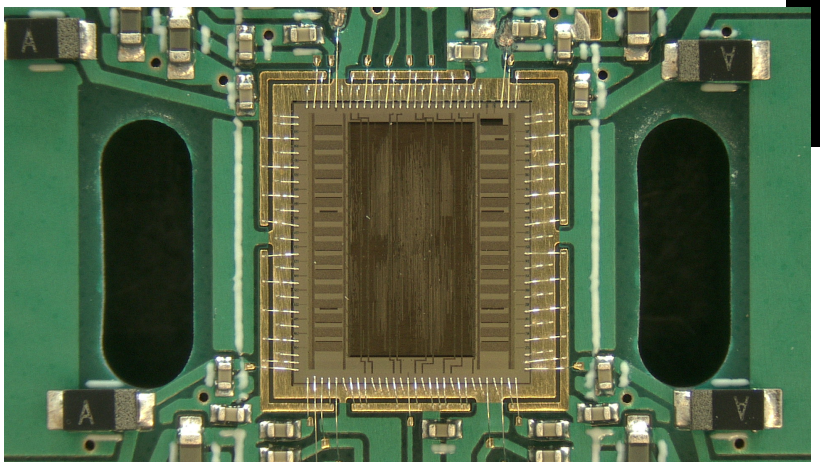
## LArPix-v1 ASIC:

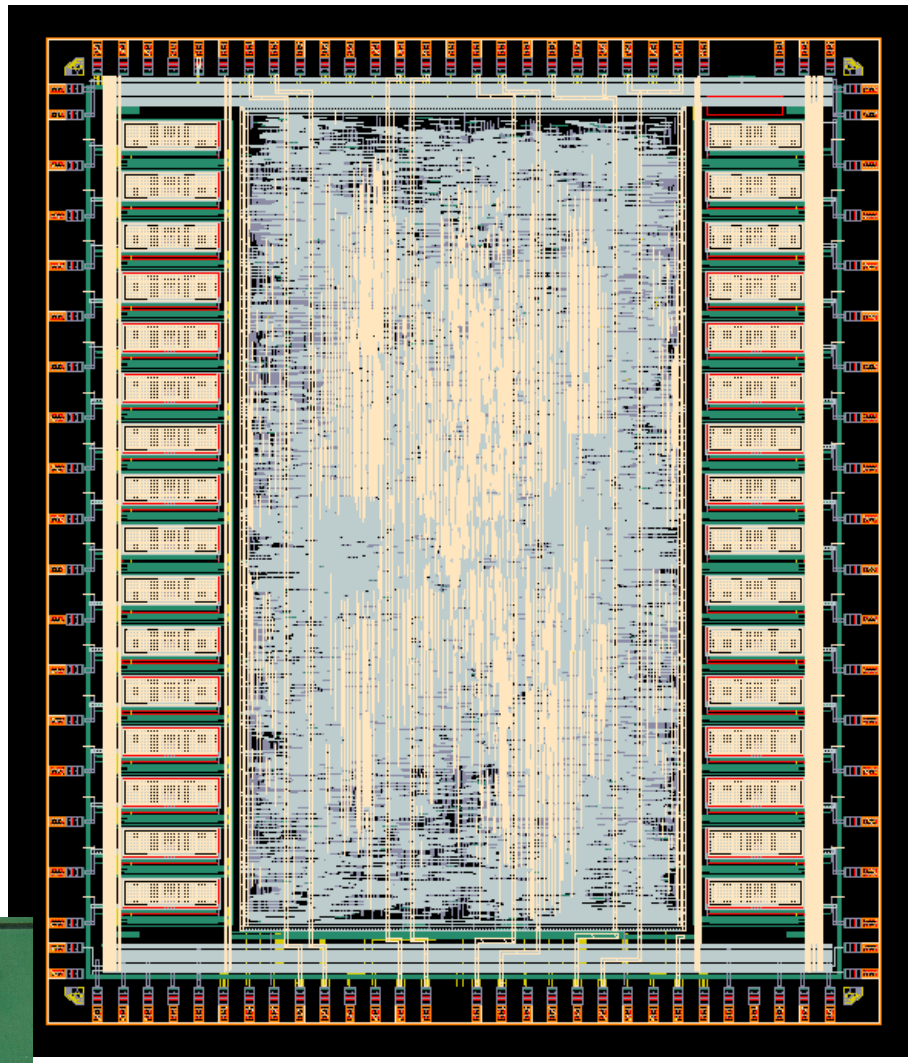
- Dec. 2016: Design began
- June 2017: Submitted for fabrication
- Oct. 2017: First chips, test boards @ LBNL
- Dec. 2017: Bench tests successfully completed
- Jan. 2018: Assembled sensor, integrated LArTPC

## Progress since last collaboration meeting:

- Feb. 2018: First tracks from true 3D LArTPC @ LBNL
- Mar. 2018: Developed integrated control system
- Apr. 2018: Assembled scalable 512-channel system, operated in 60-cm-drift TPC @ Bern
- May 2018: Operated 832-channel system @ LBNL







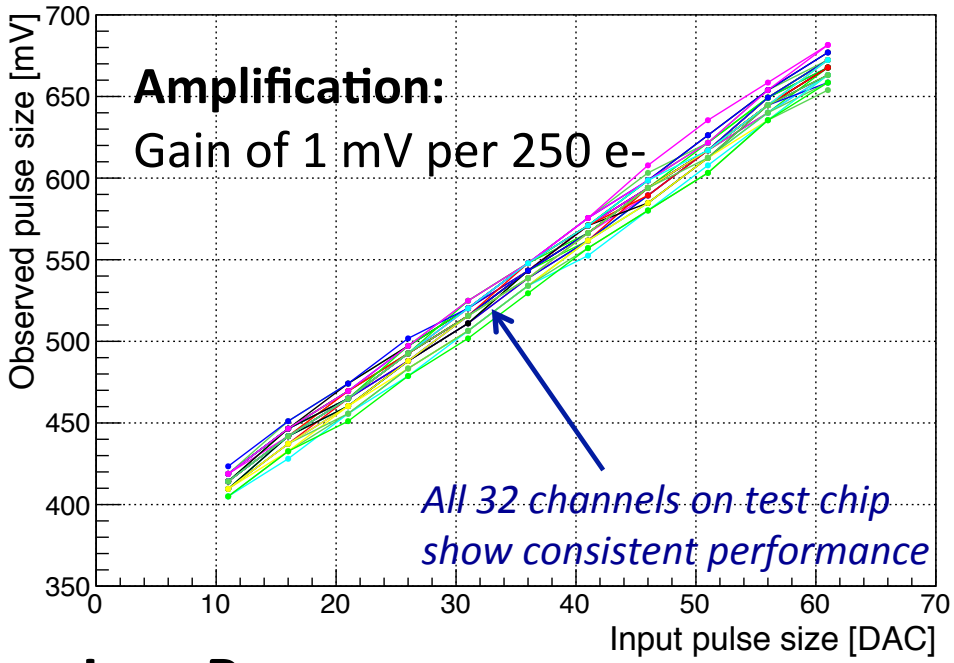
Process: 180nm bulk CMOS

**Design and testing team @ LBNL:**

D. Dwyer, C. Grace, M. Garcia-Sciveres, A. Krieger, D. Gnani, T. Stezelberger, S. Kohn, P. Madigan, H. Steiner

# Initial Bench-testing Results

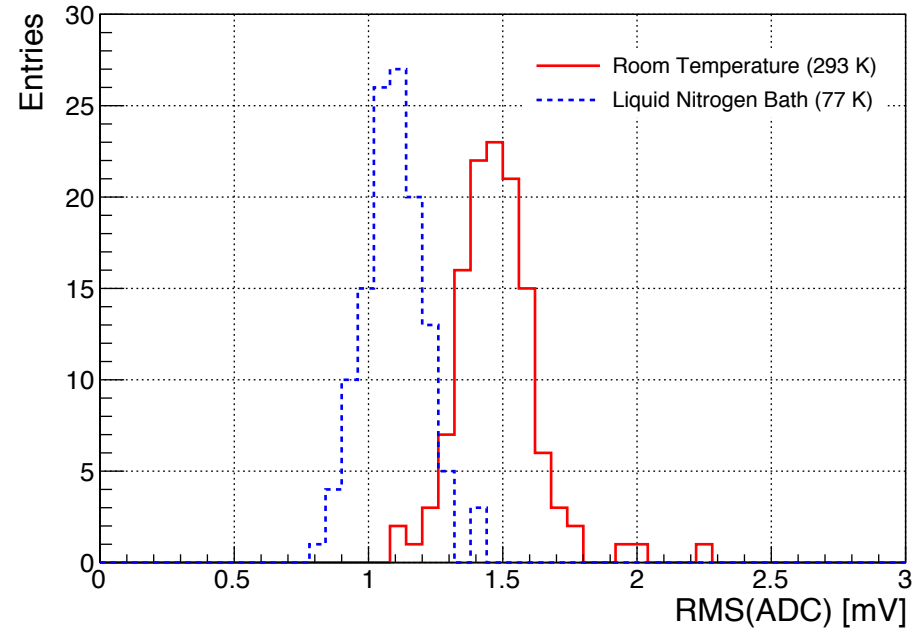
**Demonstrated low-noise low-power cryogenic amplification, digitization, and readout:**




**Low Noise:**

~1.5 mV (~375 e-) at room temp

~1.1 mV (~275 e-) in $LN^2$ bath




## Low Power:

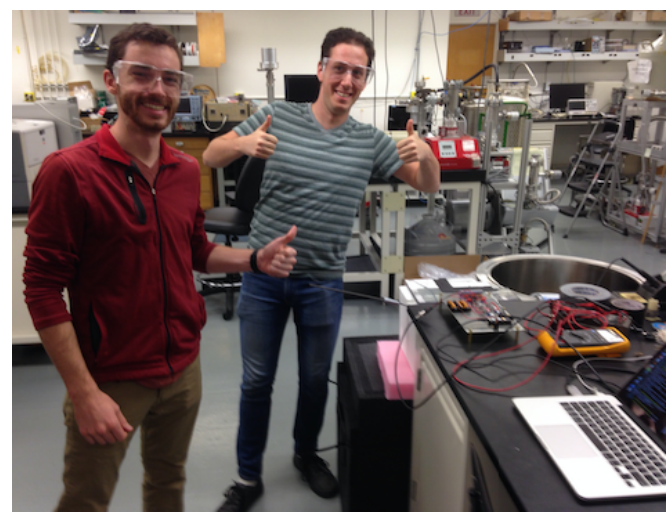
Average power for 128-channel readout:

- Analog: 24 µW/channel
- Digital: 38 µW/channel
- **Total: 62 µW/channel**

**Performance exceeds design targets:**

< 500 e- ENC

< 100 µW/channel

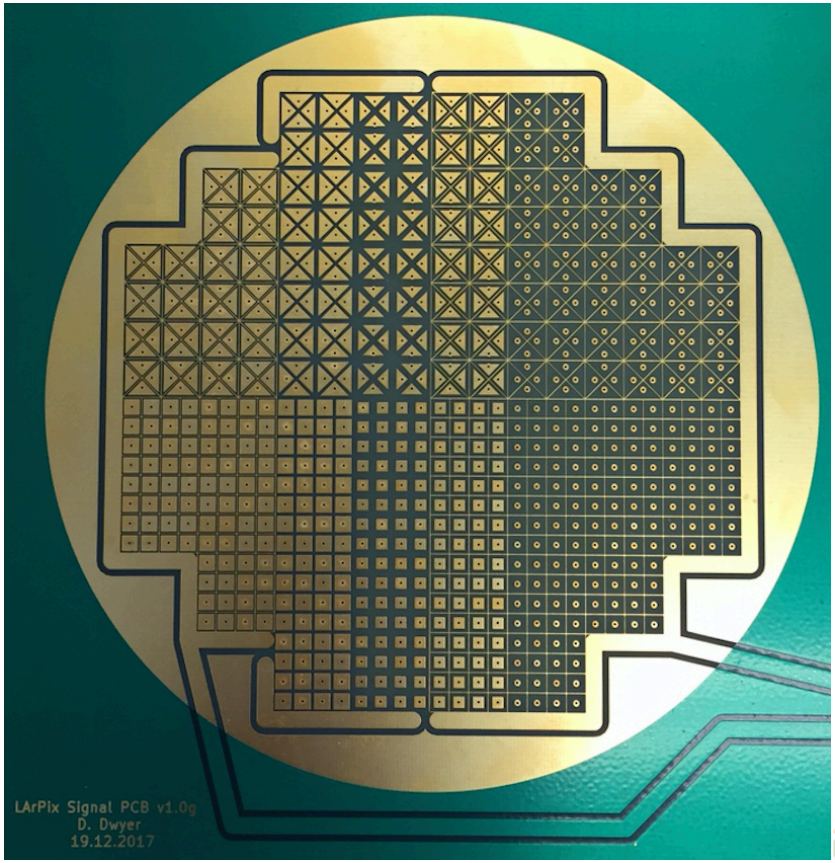


*P. Madigan, S. Kohn: drove testing effort*

# LArPix-v1: Readout Assembly

## Pixel Board:

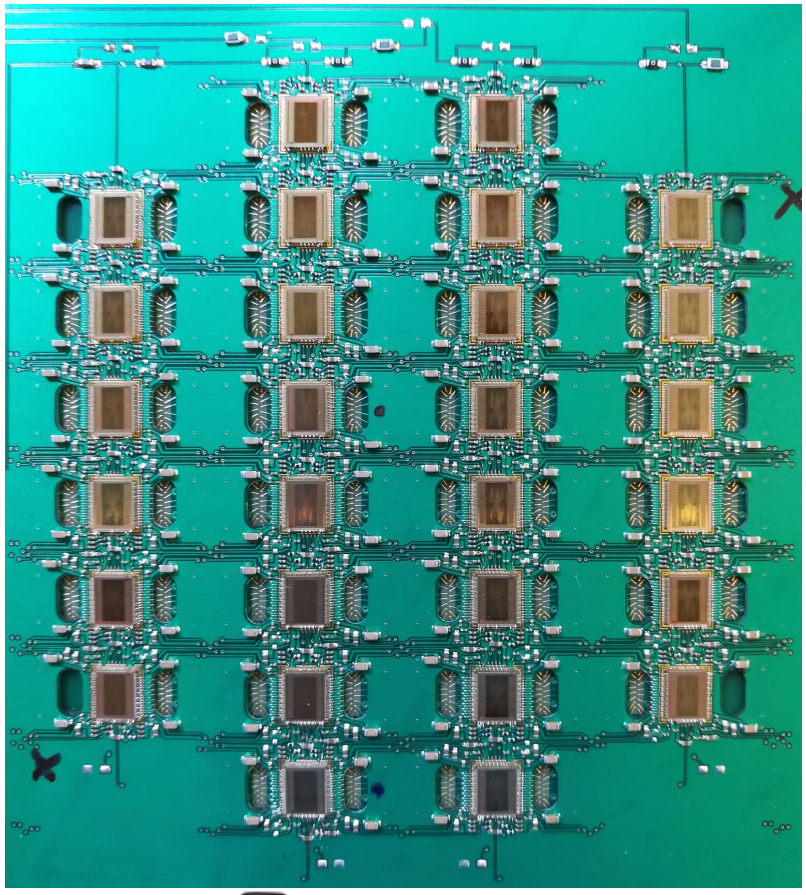
Standard printed circuit board
Fits Bern Pixel Demonstrator TPC
10 different pixel geometries

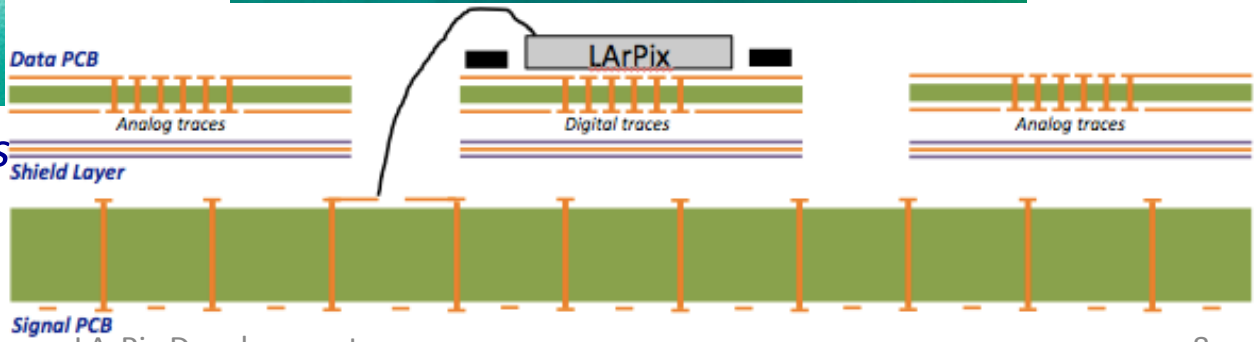



*10 cm diameter, 3mm pitch, 832 pixels*

## Complete readout assembly

28-chip LArPix data board sandwiched to pixel board

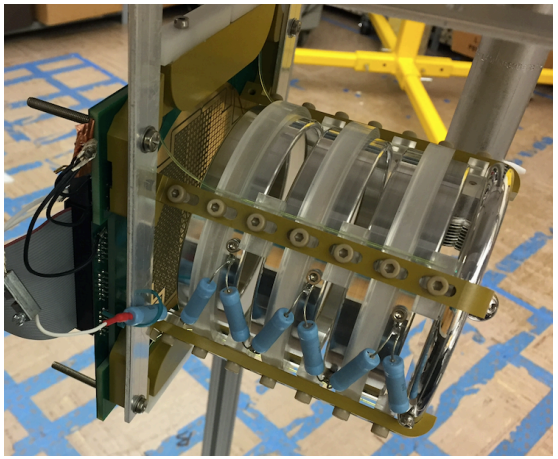


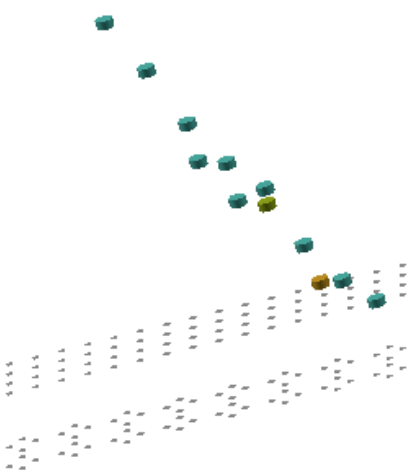


# LArTPC Operation

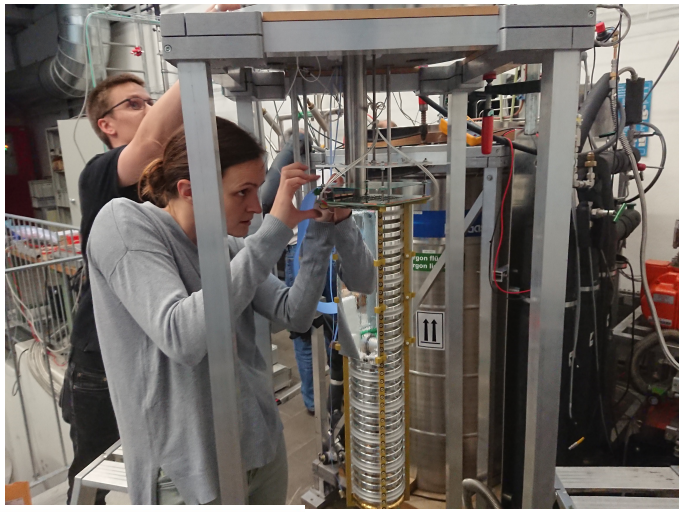
## Demonstration of cosmic ray detection at increasing scales

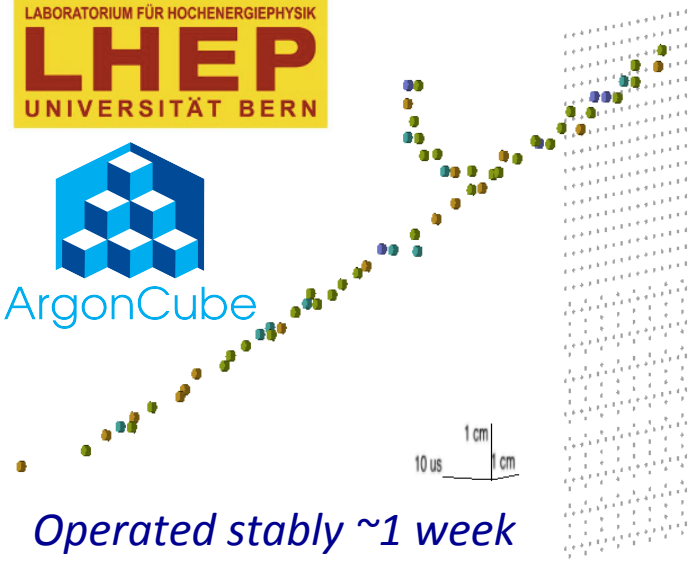
**Feb 2018:**
128-pixel system @ LBNL
10 cm drift, 200 V/cm





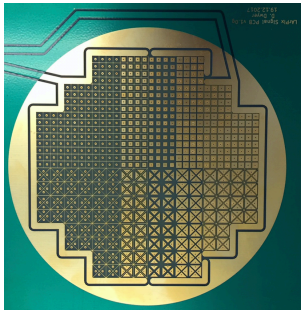
**Apr 2018:**
512-pixel system @ Bern
60 cm drift, 1 kV/cm

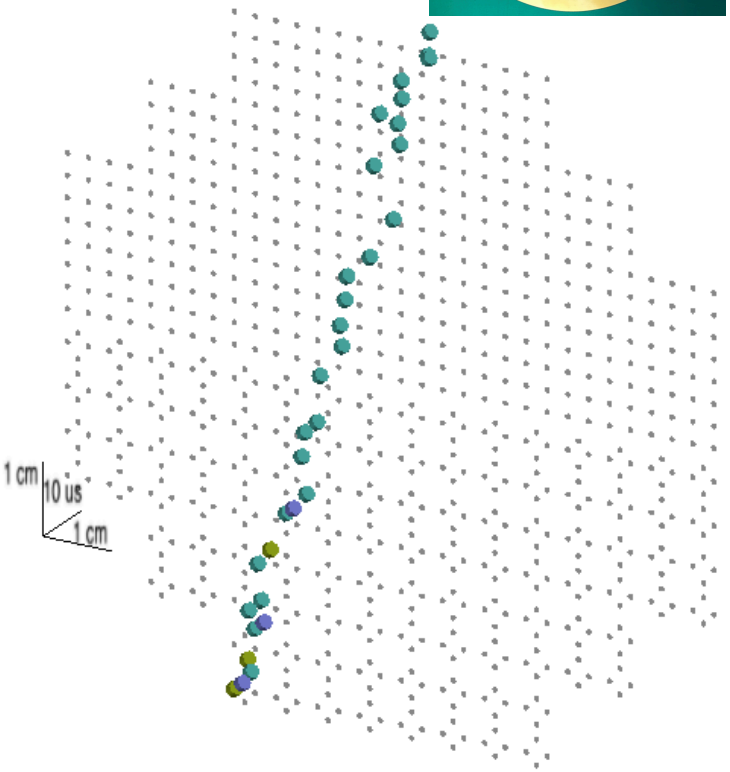





*Operated stably ~1 week*

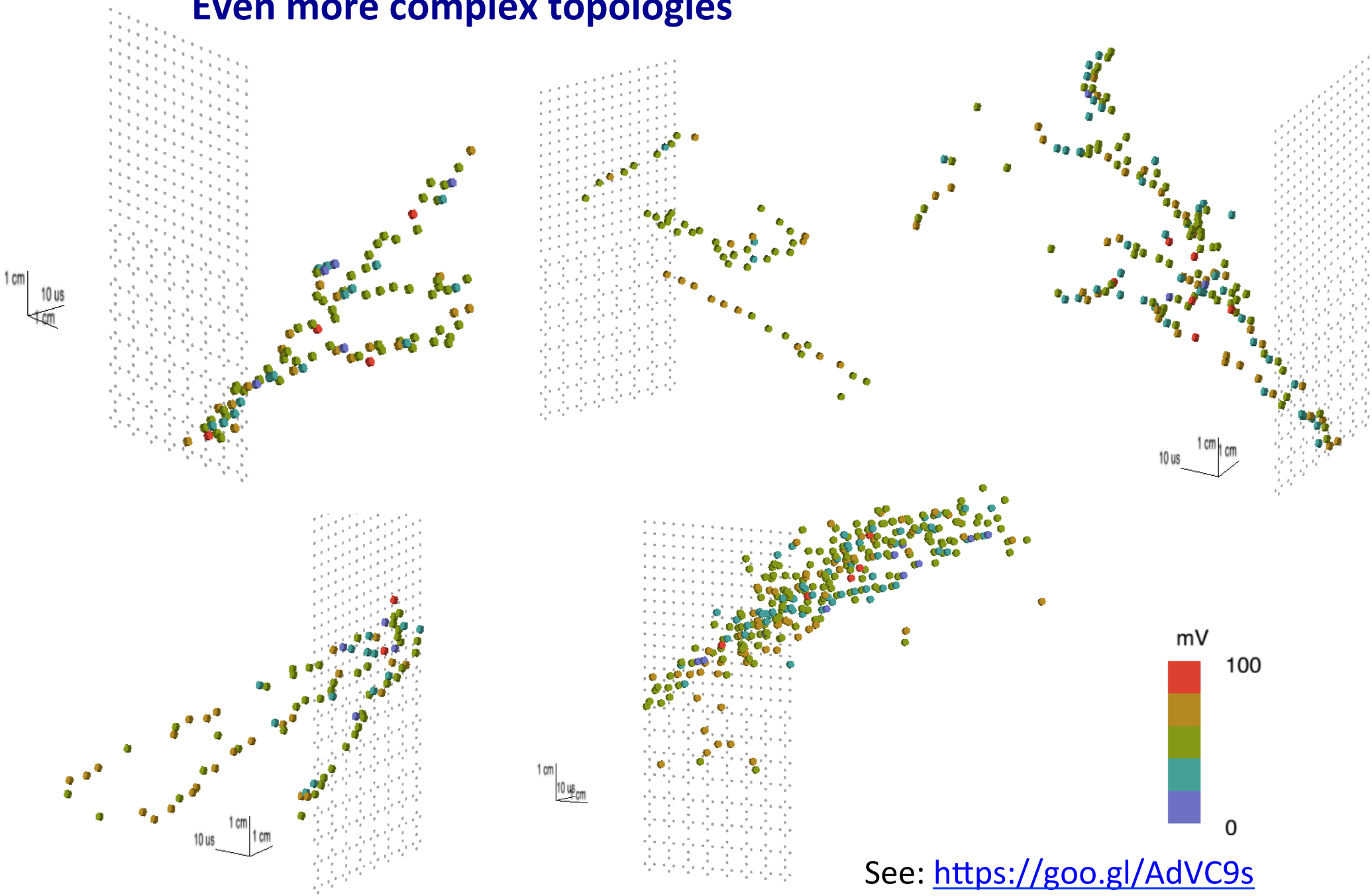
**May 2018:**
832-pixel system @ LBNL





# LArPix @ Bern

## Even more complex topologies




See: https://goo.gl/AdVC9s

# LArPix Raw Data

## Brief description of raw LArPix data

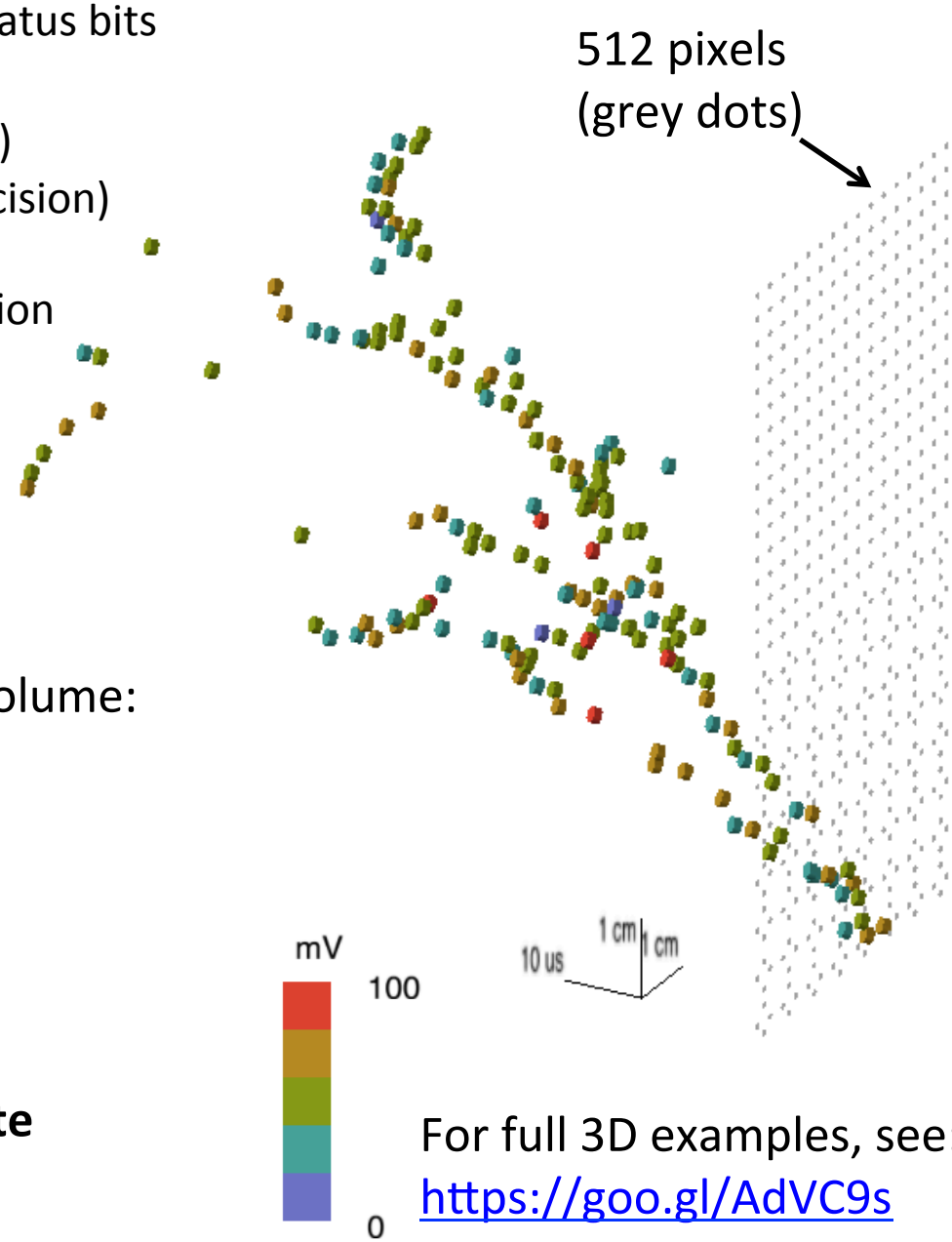
54-bit hit record: Pixel ID, ADC value, timestamp, status bits

Each colored point shows one self-triggered hit

- Hit x, y position from pixel location (3 mm precision)
- Position along drift given by timestamp (200 ns precision)
- Color shows hit amplitude (2 mV precision)
- ADC value converted to mV based on initial calibration

No filtering, manipulation applied to raw data.

→ Noise is very low: *>20:1 SNR for MIPs*




## Comment on LArPix data rates:

Pixel self-triggering substantially reduces data volume:

<u>LArPix operation @ Bern:</u>

60cm drift at surface

512 pixels, ~0.3 Hz/pixel → **~3 kB/s total rate**

<u>DUNE Near Detector:</u>

50cm drift underground

8M pixels, ~0.01 Hz / pixel → **~2 MB/s total rate**

For full 3D examples, see: https://goo.gl/AdVC9s

# LArPix Triggering

## Self-triggering with pulsed reset ≠ Zero suppression

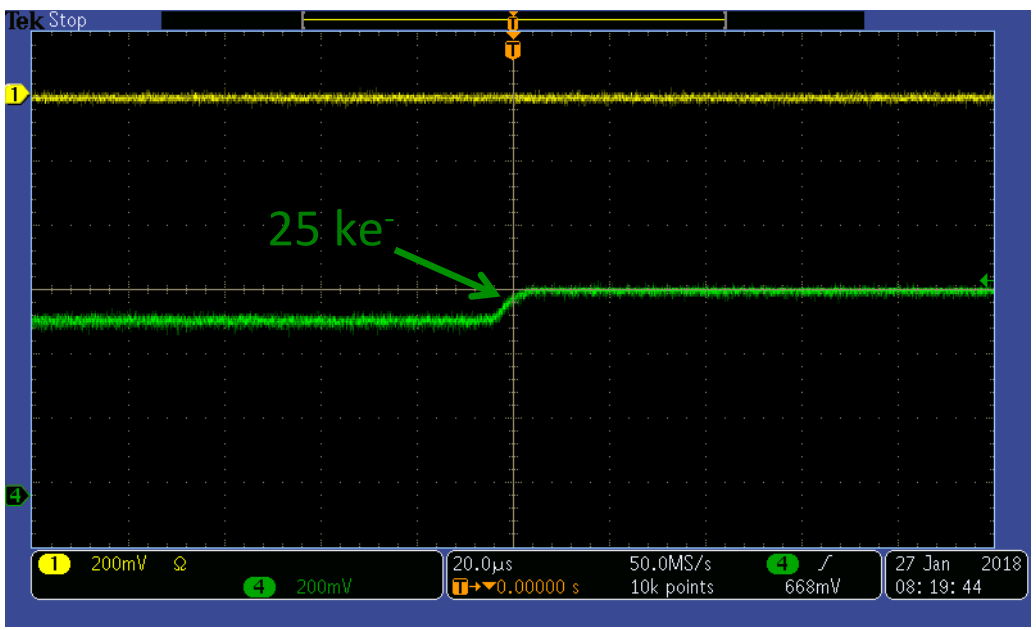
**LArPix has no resistive feedback**

→ Charge stays on pixel until you do something with it

**Your choices:**

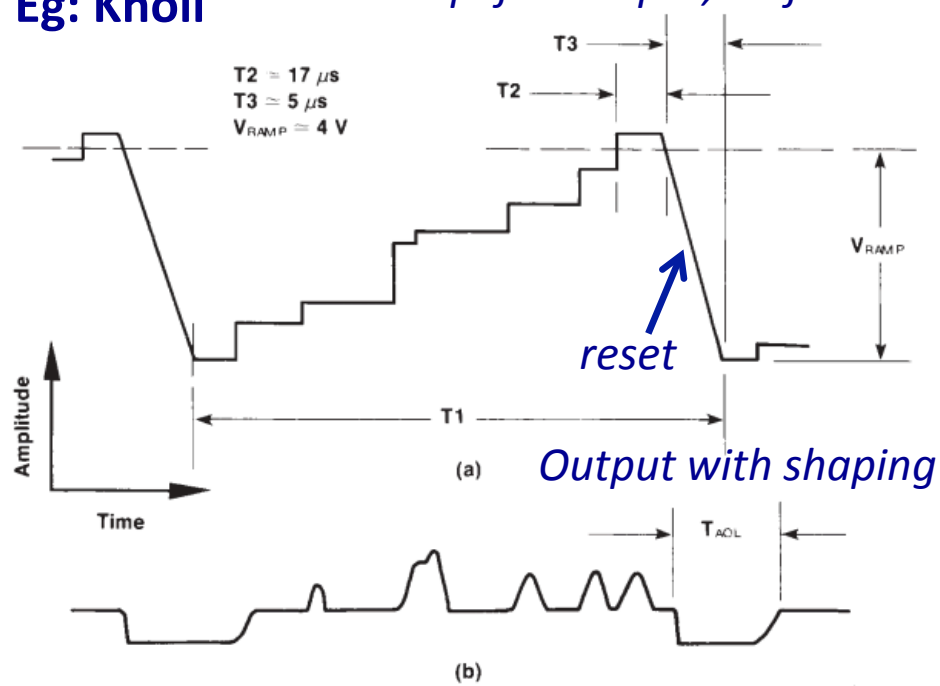
- Self-trigger reset: digitize and drain charge after threshold crossed
- External-trigger reset: digitize and drain sub-threshold charge based on external signal
- Cross-trigger reset: digitize and drain sub-threshold charge based on self-trigger of another pixel
- Periodic reset: periodically discard sub-threshold charge without digitization

*Example MIP-scale signal, without reset*



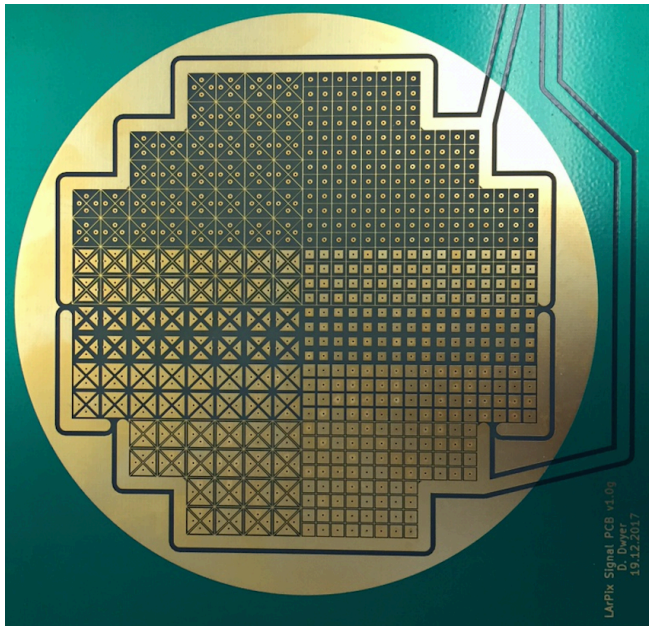

**Eg: Knoll**

*Amplifier output, no feedback*



# Recent Progress: 832-channels

## Completed full instrumentation of first-generation readout system

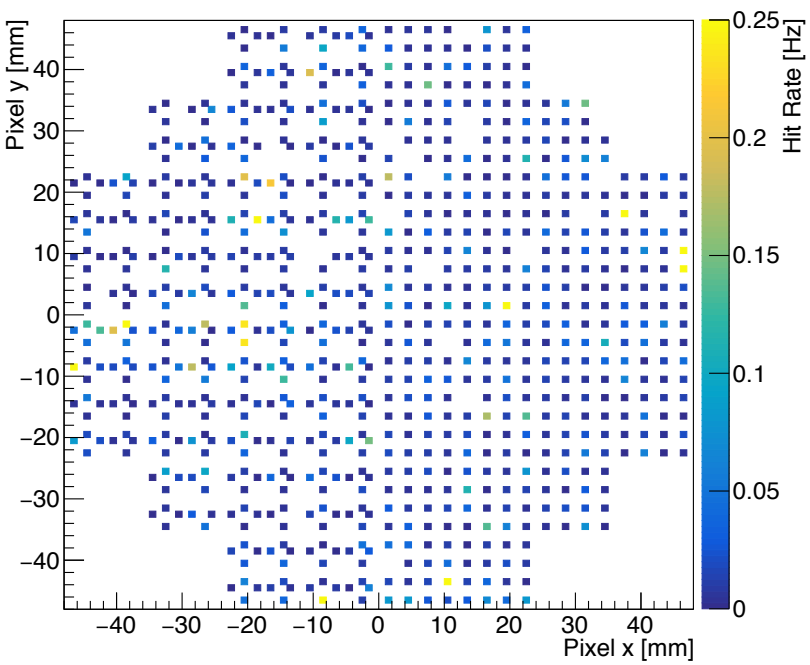


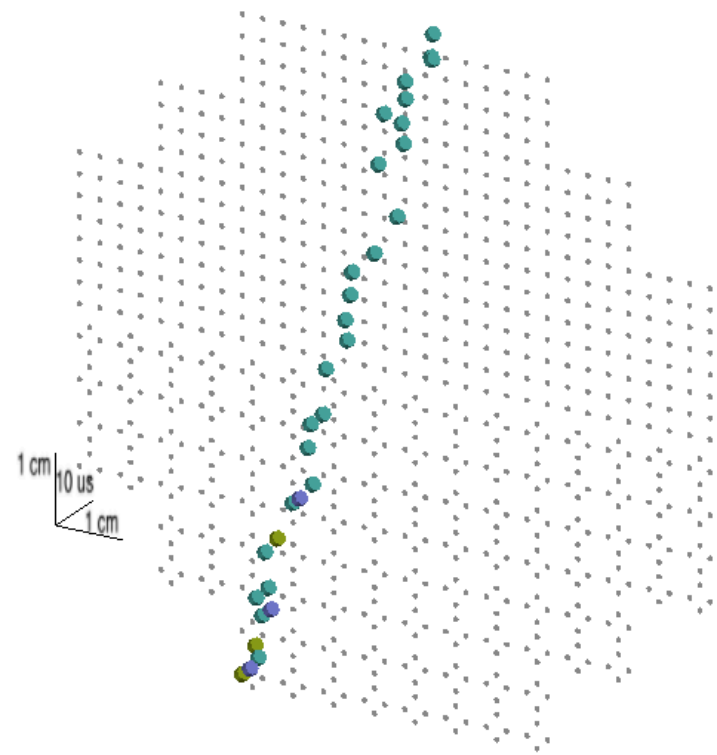
**May 21:**

Began readout upgrade: 512 → 832 channels

**May 25:**

Completed testing in LArTPC @ LBNL



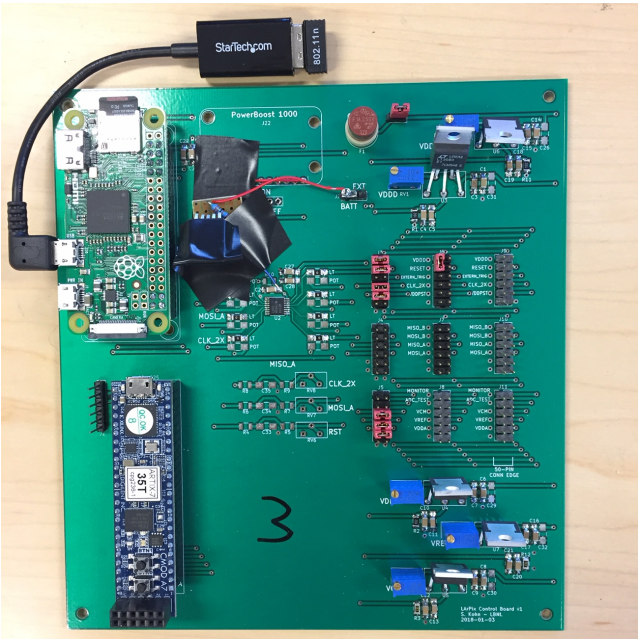

**Initial results from LArPix testing program:**

*arXiv:1808.02969, Accepted by JINST*

# Recent Progress: Control System

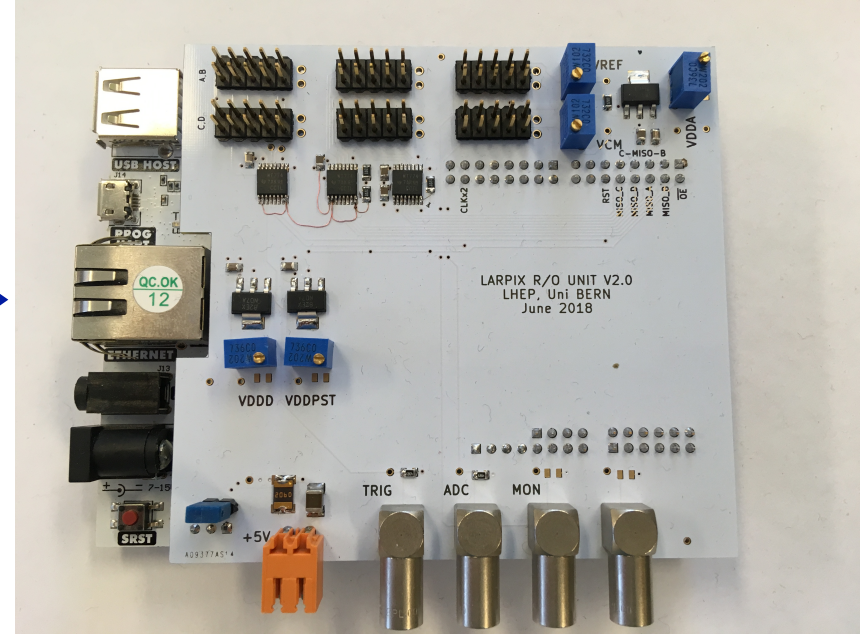
## Improved LArPix DAQ electronics for large-scale detectors

### Current Control Electronics




Developed at LBNL
Controls O(10k) pixels
Not easily scalable to larger systems
Very effective during initial R&D

### Improved Control Electronics



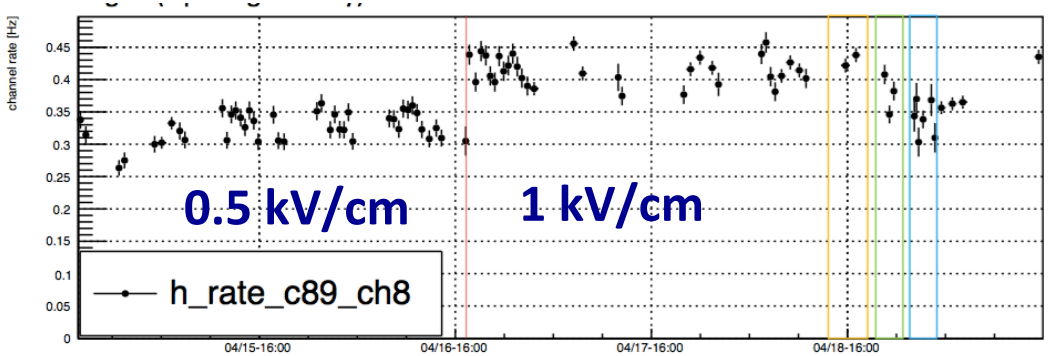

Developed at Bern *Thanks, Igor!*
Individual module: O(100k) pixels
Highly Scalable: Multi-module control via ZeroMQ over GB ethernet
Very affordable: O($100) per unit

# Recent Progress: Analysis

## P. Madigan:

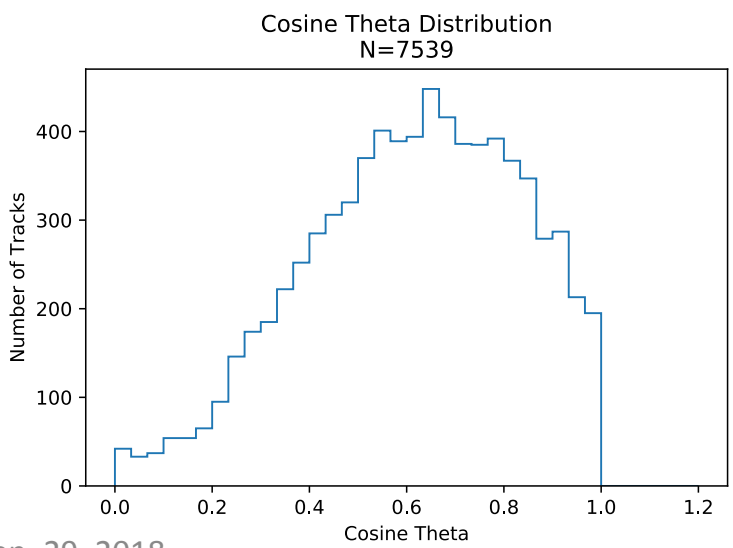
Established data processing software for calibration and reconstruction

**Stable pixel rate vs. time** (~1 week)



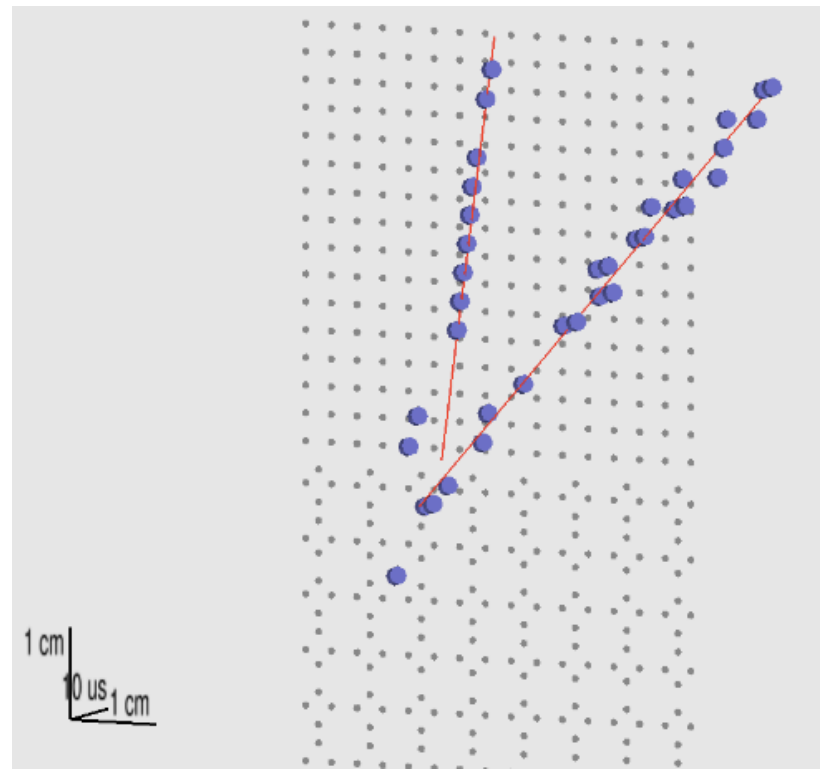

## V. Barnard (U-Penn):

Examined reconstructed cosmic rays




## S. Kohn:

- Improved LArPix interactive 3D event display
- Developed 3D track reconstruction algorithm




*Pursuing collaboration on native 3D LArTPC reconstruction techniques with SLAC.*

# Recent Progress: LAr System

**Designed and commissioned new High-purity LAr system at LBNL**


*Special thanks to P. Madigan for successful system assembly and commissioning!*

## Description:

- Single-pass purification
- Easier operation than previous system
- Dedicated to LArPix testing
- Cycle time (fill, test, purge) should be ~24 hrs.

## Aug. 13:

First LAr fill and successful safety evaluation

## Past week:

Completed activation of new LAr purifier.

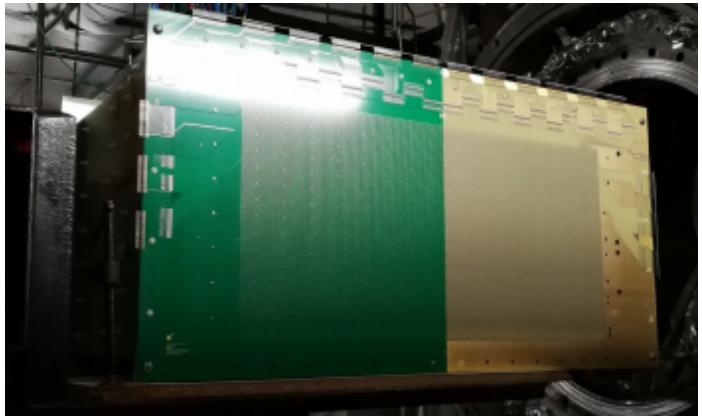
## Next Steps:

- Assess system noise
- Demonstrate $e^-$ drift
- Acquire cosmic ray data

# Next Steps: Demonstrators

## Roadmap of potential demonstrations at increasing scales:

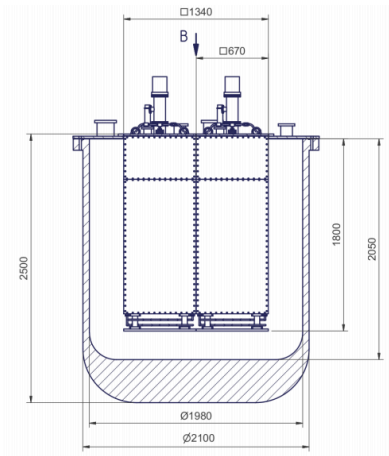
### LArIAT LArTPC

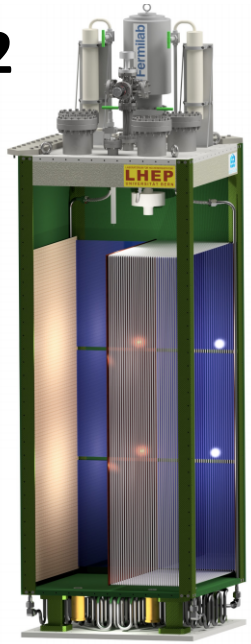


Readout area: 0.36 $m^2$
# pixels: 22.5k
# ASICs: 350
Target: Mid 2019

Provide known particle beam for detailed assessment of PID and energy performance.

### ArgonCube 2x2 Demonstrator

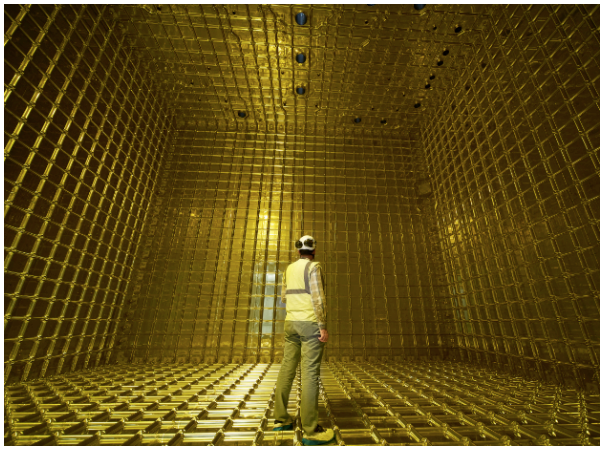



Readout area: 6.4 $m^2$
# pixels: 400k
# ASICs: 6.3k
Target: Late 2019

First module currently under construction. Demonstrator for DUNE Near Detector

### ProtoDUNE (Run 2)?



Readout area: 13.8 $m^2$ / APA
# pixels: 860k / APA
# ASICs: 13.5k / APA
Target: 2020-2021

Side-by-side comparison with DUNE wire readout technologies.

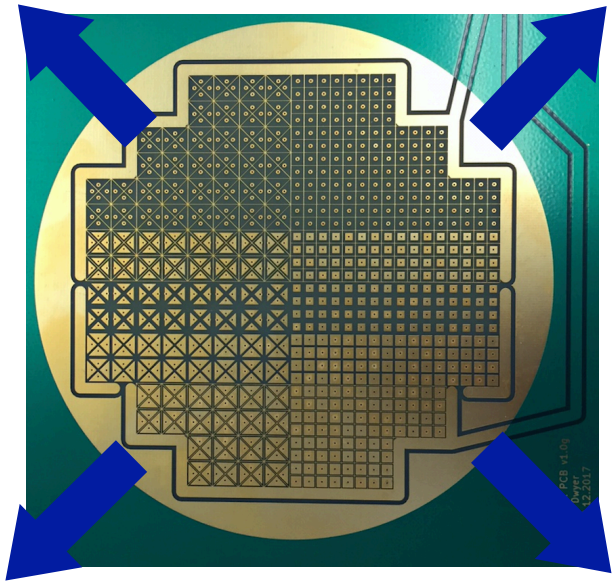
*Also pursuing LArPix readout for High-pressure Ar gas TPC Near Detector Module with FNAL, others*

# Next Steps: Scalability

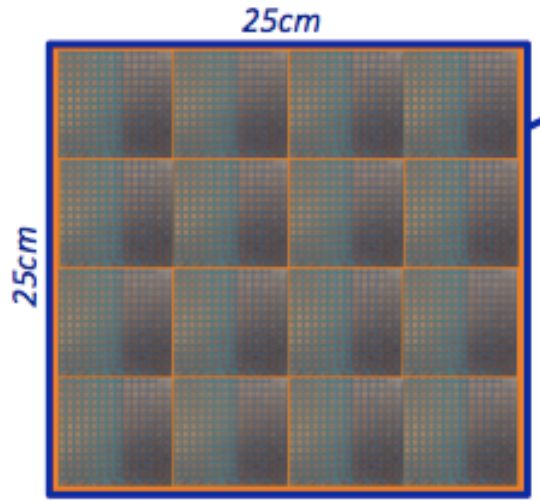
## Design modular pixel tile for instrumenting large area sensors

- Standard size (e.g. 25cm x 25cm, or 32cm x 32cm) for easy industrial production
- One tile = one LArPix daisy chain
- ASIC-only: no other active components

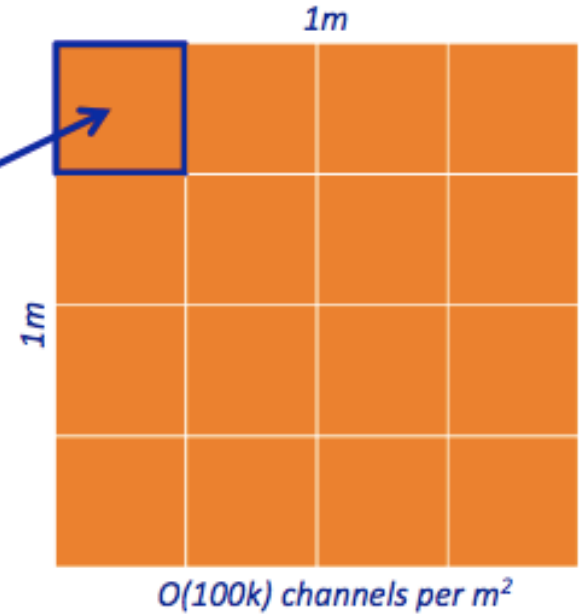
*Extend pixels edge-to-edge*



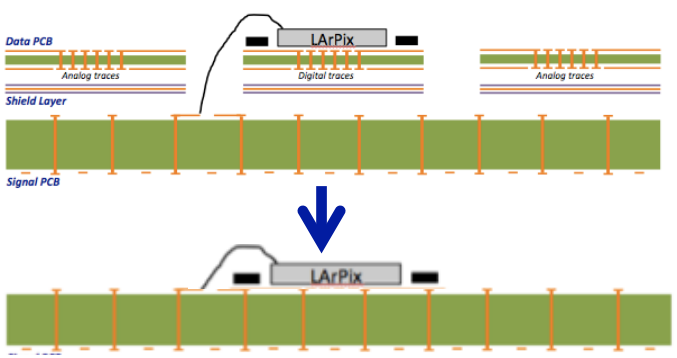
*Increase size*



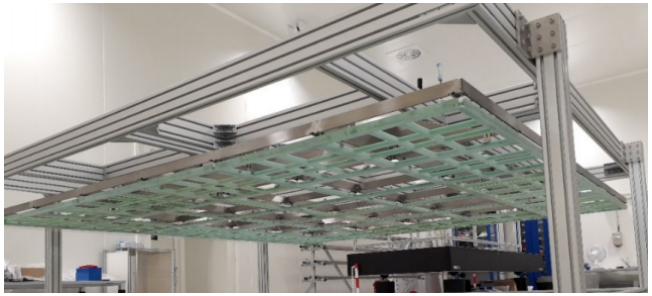

*Tile anode*




*Reduce to single PCB*




*e.g. Dual Phase G10 frame*



**Anode Frame?**

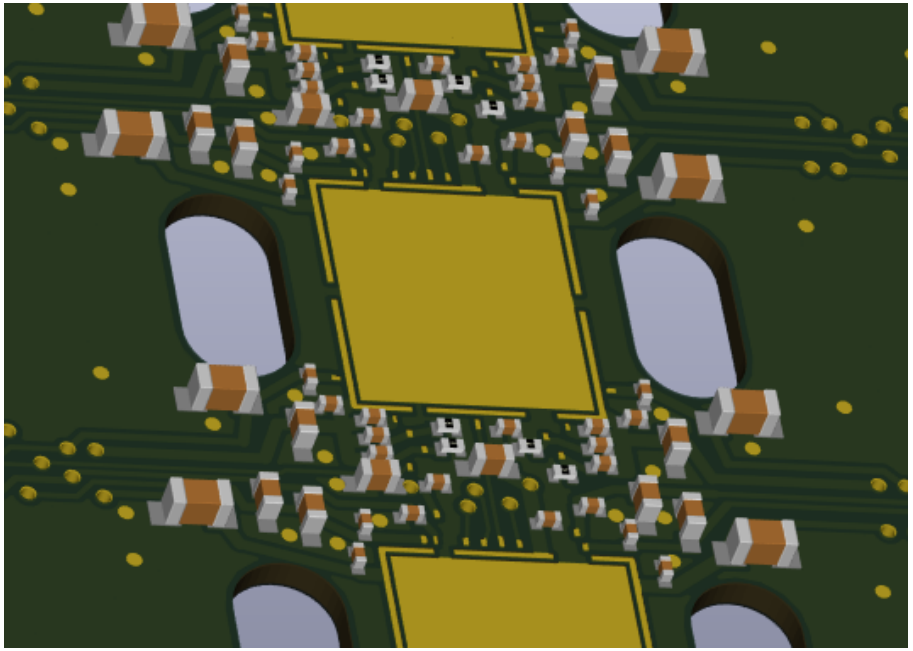
- Support tiles from backside
- Support cabling
- Handle thermal contraction
- Maintain required tolerances

# Next Steps: LArPix-v2

**Exploring LArPix-v2 for scalable assembly and improved physics performance:**

Increase dynamic range for charge signal
Double number of channels per chip (32→64)
Make daisy chain I/O robust to chip failure.
Substantially reduce external circuitry
Improve hit timestamp
Increase channel threshold range
Improve front-end pulser
Tailor bandwidth of discriminator
*Plus a number of other changes*

*Currently crowded PCB layout*



→ *Integrate external circuits into ASIC*

**Test LArPix in packaged form:**

Many advantages for assembly and testing

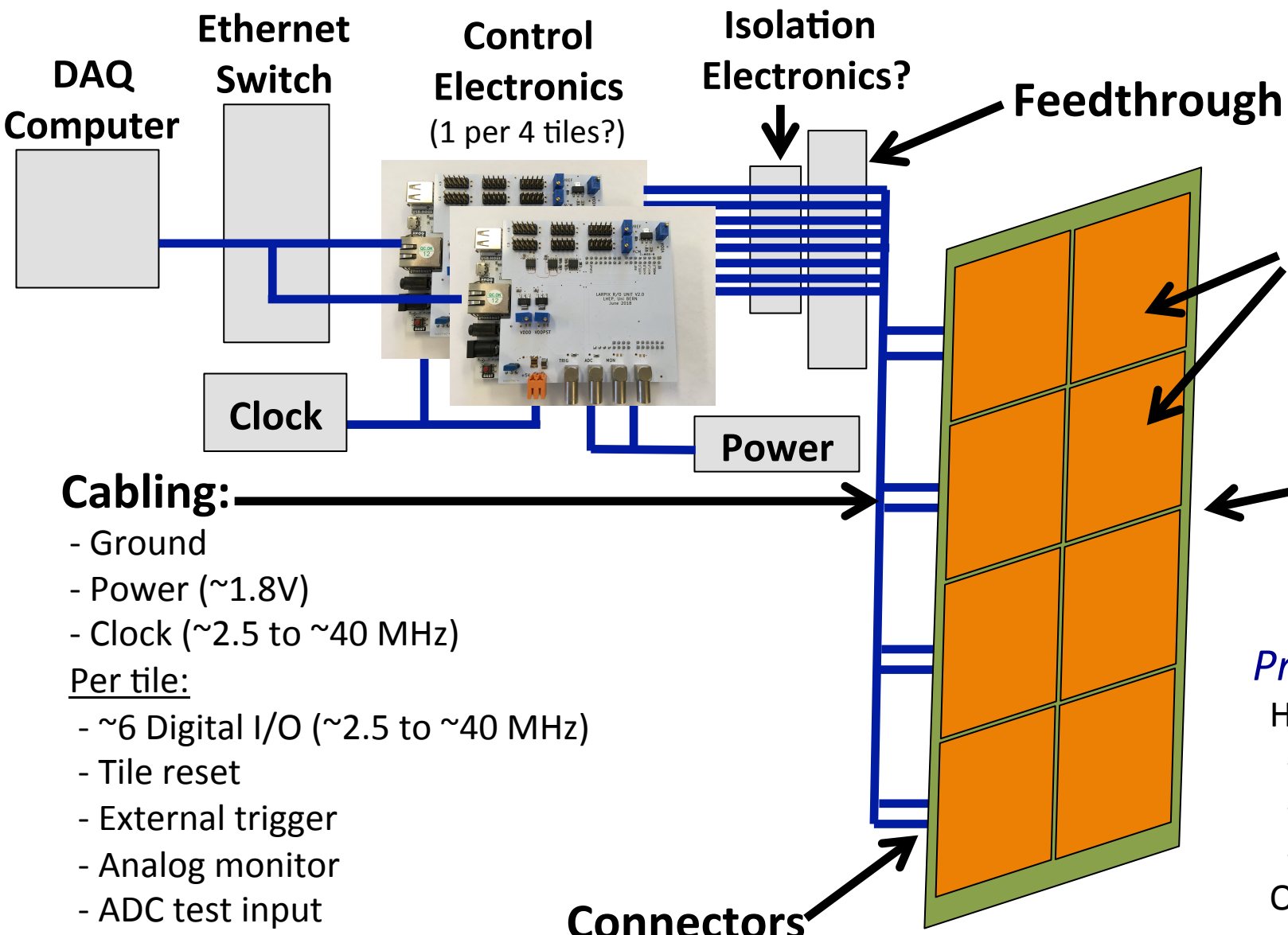
Layout seems manageable, but must demonstrate no adverse issues after packaging.

**Goal:**

*Dec. 2018:* Complete v2 design
*Apr. 2019:* Complete v2 production

# Next Steps: System Design

**Must establish a complete design for a detector-scale pixel readout system**




**Pixel Tiles,**
32cm x 32cm
~6.4k pixels each
~100 ASICs each

**Anode Frame,**
with tile and cabling attachments

**Cabling:**
- Ground
- Power (~1.8V)
- Clock (~2.5 to ~40 MHz)

Per tile:
- ~6 Digital I/O (~2.5 to ~40 MHz)
- Tile reset
- External trigger
- Analog monitor
- ADC test input
- ?

*Preliminary Concept:*
Have designs for:
- LArPix ASIC
- Pixel Tile (partial)
- Control Electronics

Other components are currently fictional.

# Next Steps: Cost Model

## Establishing production cost model for ArgonCube 2x2 and DUNE ND

**Model details:**
- Based on actual vendor quotes, or similar prior experience
- 4 mm pixel pitch
- 5m x 4m x 3m Near Detector, with 50 cm drift

**Model includes:**
- Cost to fully produce pixel tiles
- 10% spares
- 20% overhead

**Not included:**
- System design effort
- QA/QC, Testing effort
- Related systems (<< $5000/m$^2$): anode frame, cabling, feedthroughs, etc.
- Contingency

| | ArgonCube 2x2 | Near Det. |
|---|---|---|
| Readout Area [m2] | 6.4 | 120 |
| # Pixels (4mm pitch) | 4.02E+05 | 7.50E+06 |
| # ASICs | 6,282 | 117,188 |
| # Tiles (32x32cm) | 63 | 1,172 |
| | | |
| Cost, Wafer Production | $100,780 | $280,807 |
| Cost, Die Preparation | $1,571 | $29,297 |
| Cost, Packaging | $6,910 | $128,907 |
| Cost, PCB Production | $3,735 | $52,806 |
| Cost, PCB Components | $2,073 | $38,672 |
| Cost, PCB Assembly | $1,176 | $15,690 |
| | | |
| **Total Cost** | **$116,245** | **$546,178** |
| **Total Cost (+20% Ovhd)** | **$139,494** | **$655,414** |
| **Cost, per square meter** | **$21,796** | **$5,462** |

~$3.8k @ 5mm
~$9.1k @ 3mm

*General conclusion: production costs seem very reasonable*

# Next Steps: Partners

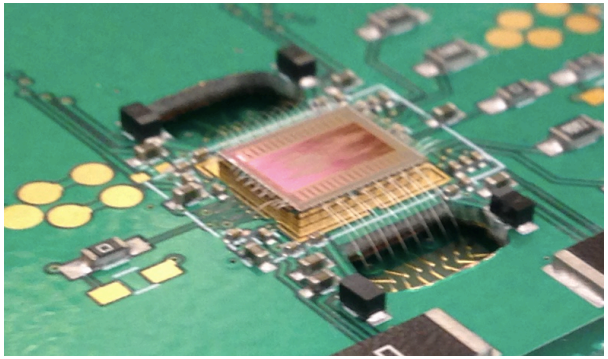
## Substantial effort required to develop detector-scale system

**LArPix ASICs:** Integrated circuits for charge signal amplification, digitization, and readout
**Pixel Anode Boards:** Circuit boards which host charge-sensitive pads and readout ASICs
**Internal Cabling:** Transmits power and I/O from feedthrough to anode
**Anode Frame:** Provides structural support for anode PCBs and cabling
**Readout Feedthroughs:** Transmits power and I/O passage through cryostat
**Isolation Electronics:** Provides isolation and filtering of power and I/O at feedthrough
**External Cabling:** Transmits power and I/O from DAQ electronics to Isolation electronics
**Power Supplies:** Provide power needed to drive the electronics
**DAQ Electronics:** Generates clock and provides I/O bridge from ASICs to DAQ computer
**DAQ Computer:** Issues input commands, receives output data packets, records data
**DAQ Software:** Formats input commands, interprets output data packets.
**Calibration:** Dedicated techniques for pixel readout calibration
**Pixel LArTPC Analysis:** Studies, simulation, algorithms needed to guide development and prepare for large-scale pixelated data analysis.

*Many open roles for partners for design, production, and testing of all system aspects!*

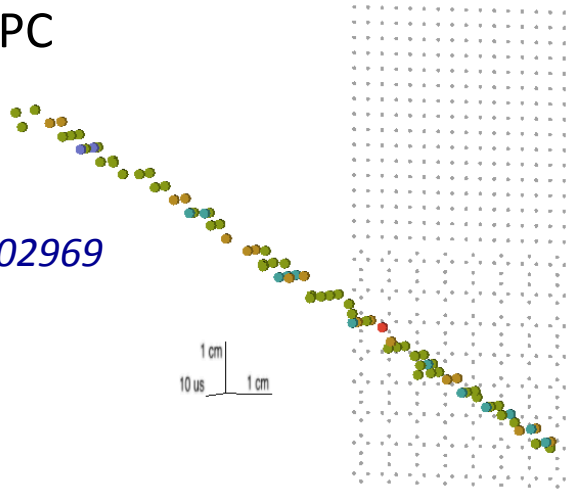
*Please attend the Pixel LArTPC workshop (Sep. 29, 2018 @ FNAL): https://indico.fnal.gov/event/18172*

# LArPix Summary



## 3D pixelated charge readout for LArTPCs:

LArPix demonstrates feasibility of low-noise low-power 3D readout
Unique front-end channel for every pixel
Key purpose: overcome neutrino pileup in DUNE Near Detector LArTPC

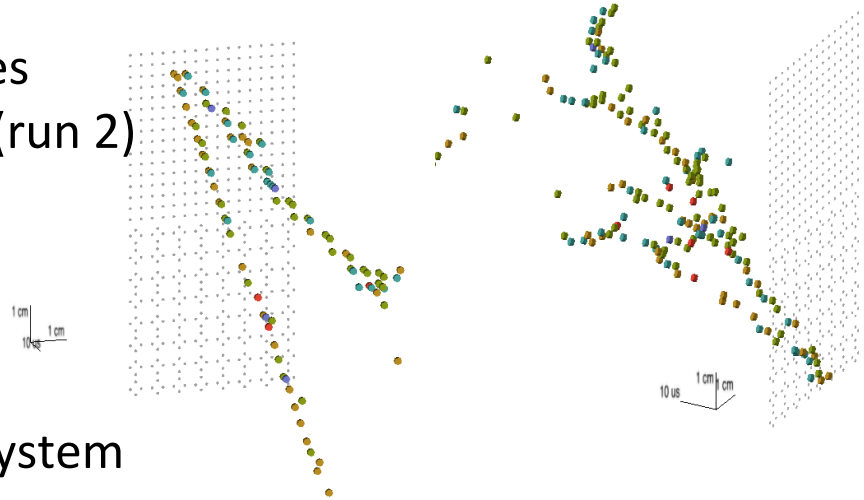



## Recent Progress:

Operation of complete 832-channel LArPix readout system *arXiv:1808.02969*
Development of new control electronics
Progress in LArPix analysis, reconstruction
Commissioning of new high-purity LAr system

## Next Steps:

Aiming for technical demonstrations at increasing scales
→ LArIAT, ArgonCube 2x2 Demonstrator, ProtoDUNE (run 2)
Many developments to ease large-scale production
- Modular pixel tile design
- Version 2 of LArPix ASIC
- Production cost model
- Partnerships for development of complete readout system




*Learn more at Pixel LArTPC Workshop (Sep. 29 @ FNAL): https://indico.fnal.gov/event/18172*