VELO Upgrade Data Acquisition System

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October 2, 2018

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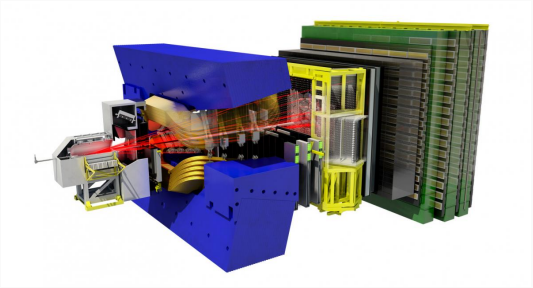
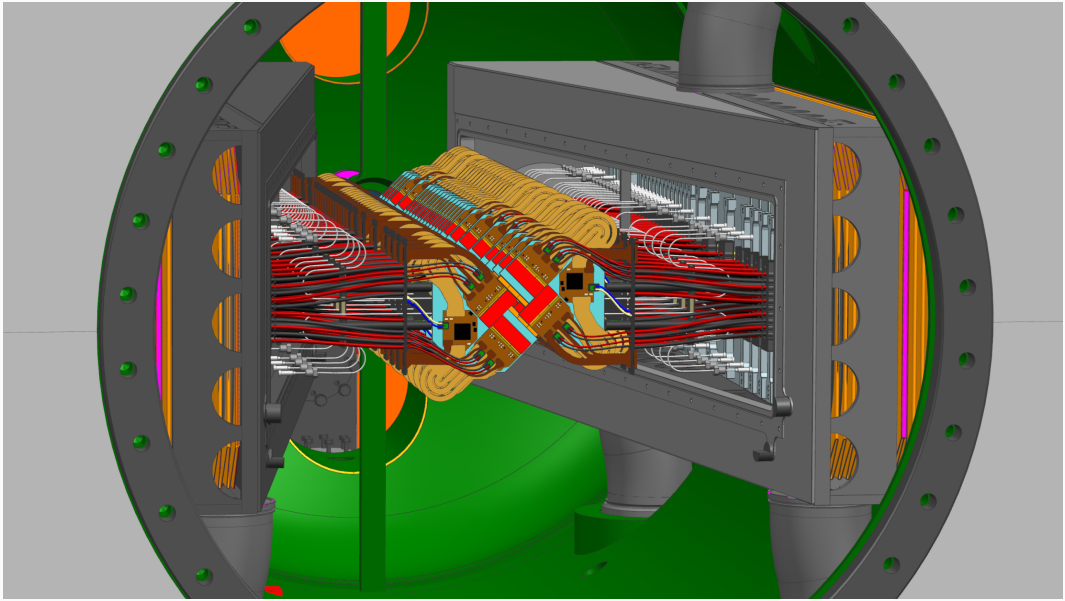
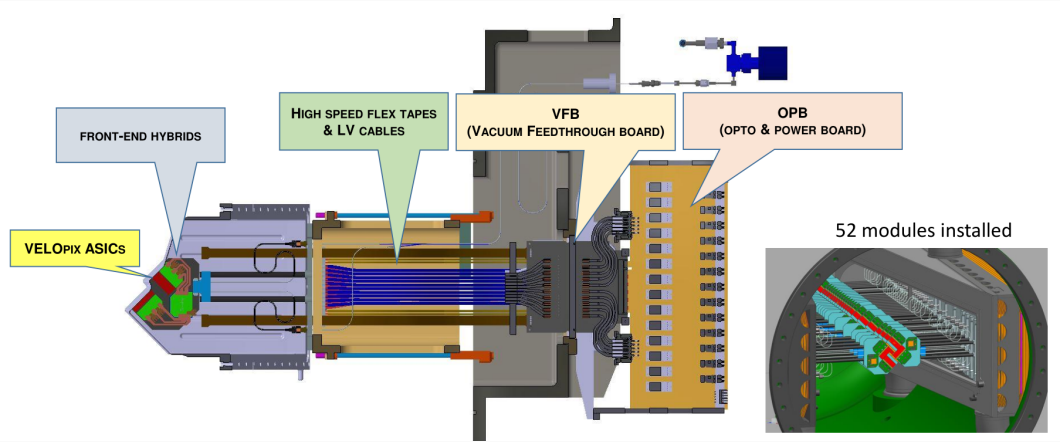
VELO Upgrade

- Vertex Detector for the LHCb upgrade
- 52 silicon pixel modules around the LHC beam interaction region
  - Very high radiation environment
  - 50fb^{-}1 integrated luminosity
  - maximum fluence approx. 8×10^{15} $\mathrm{MeV}\cdot\mathrm{n_{eq}}/\mathrm{cm}^2$
- In vacuum
  - Requires active cooling - microchannel CO_2
- LHCb Upgrade has triggerless readout - full detector readout @ 40 MHz

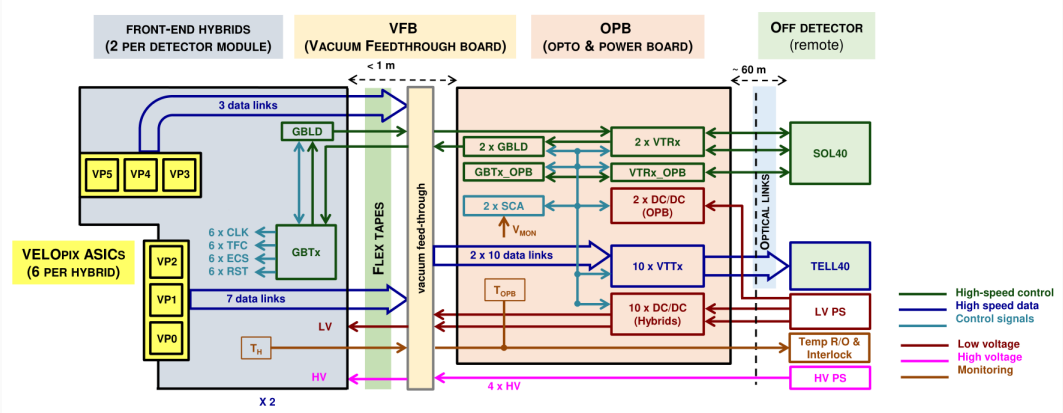




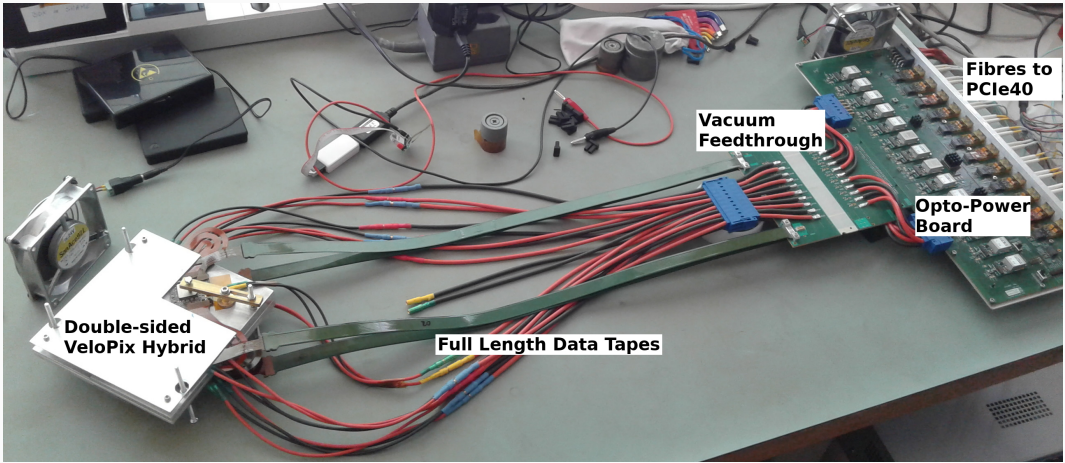
VELO Upgrade CAD



VELO Upgrade Electronics



VELO Upgrade Electronics



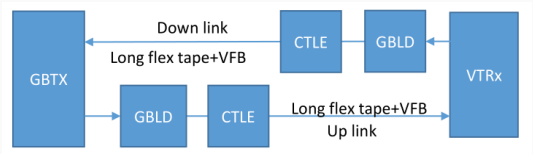
VELO Upgrade in Numbers

Feature	
Sensors	Pixels
# of modules	**52**
Detector Active area	0.12 m^2
	$\sim$41 M pixels
Technology	electron collecting
	200 μm thick
Max fluence	8×10^{15} $\mathrm{MeV n_{eq}/cm^{-2}}$
HV tolerance	1000 V
ASIC Readout rate	**40 MHz**
Total data rate	**2+ Tb/s**
Total Power consumption	2.2-2.3 kW

Pathways

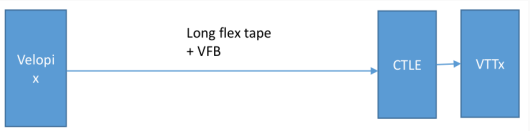
ECS - Experiment Control System

- Bi-directional with GBTx ASIC
- 4.8 Gb/s
- Use of GBLD as electrical line driver (emphasis and amplification functionality)



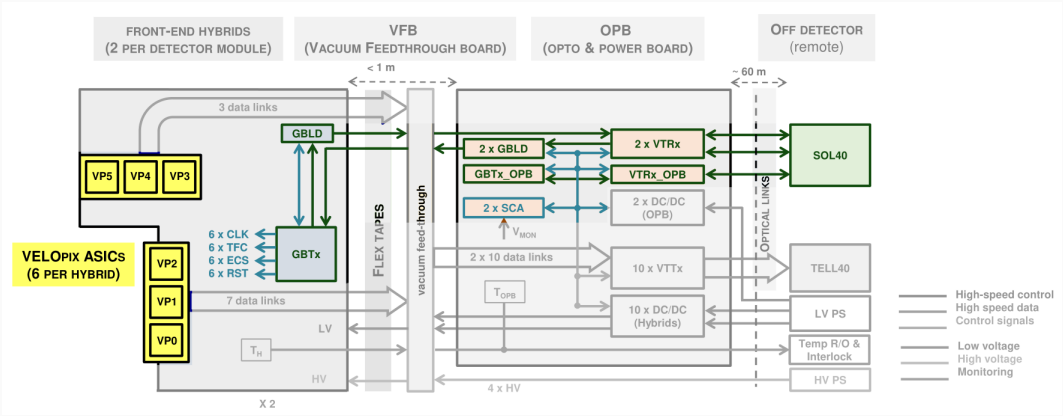
DAQ - Data Acquisition

- Uni-directional (from VeloPix to back-end)
- 5.12 Gb/s
- VeloPix has some internal emphasis



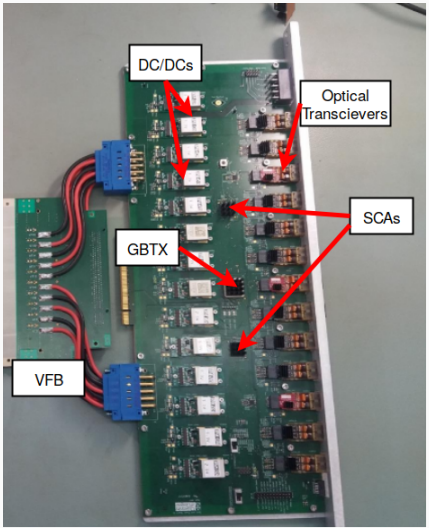
Similar electrical transmission lines for ECS and DAQ - expect similar performance.

ECS Path


FRONT-END HYBRIDS
(2 PER DETECTOR MODULE)
VFB
(VACUUM FEEDTHROUGH BOARD)
OPB
(OPTO & POWER BOARD)
OFF DETECTOR
(remote)
< 1 m
~ 60 m
3 data links
GBLD
VP5
VP4
VP3
VELOPIX ASICS
(6 PER HYBRID)
VP2
VP1
VP0
6 x CLK
6 x TFC
6 x ECS
6 x RST
GBTx
7 data links
LV
HV
X 2
FLEX TAPES
vacuum feed-through
2 x GBLD
GBTx_OPB
2 x SCA
VMON
2 x 10 data links
TOPB
2 x VTRx
VTRx_OPB
2 x DC/DC
(OPB)
10 x VTTx
10 x DC/DC
(Hybrids)
OPTICAL LINKS
SOL40
TELL40
LV PS
Temp R/O &
Interlock
HV PS
4 x HV
High-speed control
High speed data
Control signals
Low voltage
High voltage
Monitoring

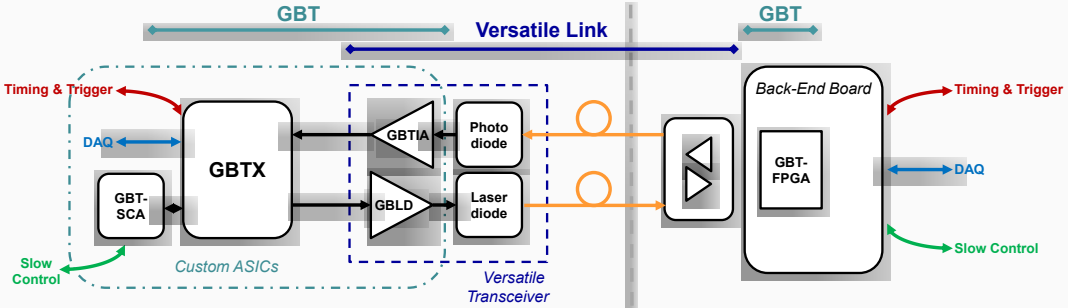
Opto-Power Board

- Situated on VELO tank exterior
  - Vacuum Feedthrough Board interfaces electronics inside VELO tank
  - Fibres to counting room at surface ($\approx 300\,\mathrm{m}$)
- Interface for data, control, monitoring signals and powering for VELO modules
  - DC/DCs for power
  - Voltage monitoring
  - Optical transceivers for driving to/from backend
- Control via GBT chipset



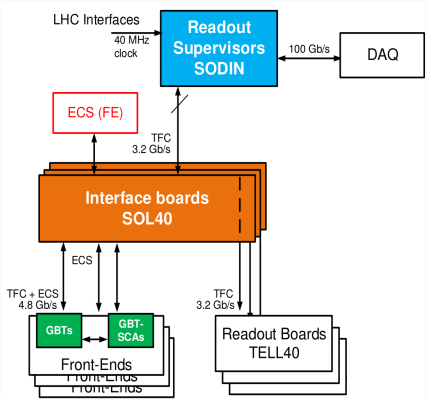
GBT - ECS interface

- The **GBTX** chip is a radiation tolerant chip for LHC upgrade experiments
- GBT Protocol can utilise three logical data paths
  - Trigger and Timing Control (TTC)
  - Slow Control (SC) - via companion SCA chip
  - Data Acquisition (DAQ) - *(NOT used for VELO)*
- All three logical paths can be encapsulated on a single physical interface

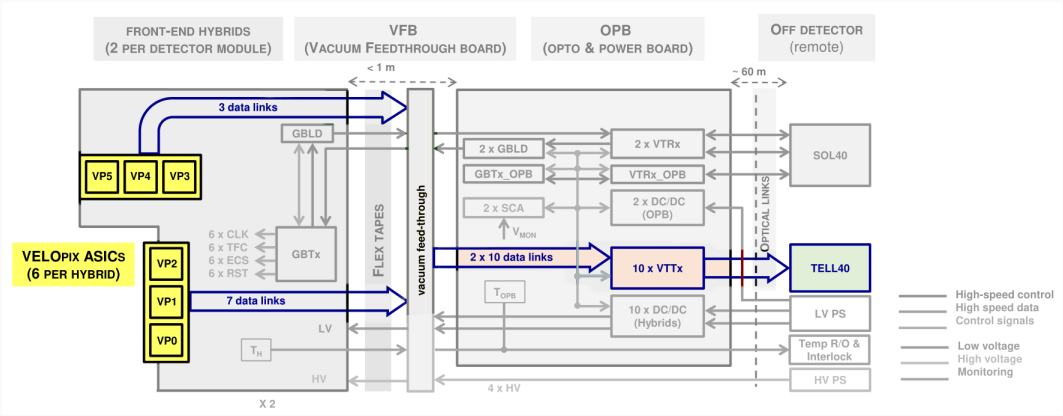


Timing and Fast Control (TFC)

- Single Readout Supervisor provides a clock and timing commands to front-end and back-end electronics
  - BXID Reset, FE Reset, BE Reset, Sync, ...
- Interfaces with LHC
- TFC commands are fixed latency
- Data are *NOT* fixed latency
- For VELO, TFC synchronisation commands form “special” GWT packets and sent immediately from front-end
  - (standard data packets are sent out-of-time)
- 10G PON network with optional feedback



DAQ Path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GBTx
7 data links
LV
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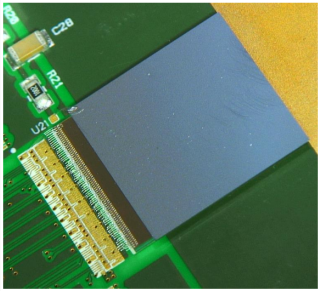
X 2
FLEX TAPES
vacuum feed-through
2 x GBLD
GBTx_OPB
2 x SCA
V_MON
2 x 10 data links
T_OPB
2 x VTRx
VTRx_OPB
2 x DC/DC
(OPB)
10 x VTTx
10 x DC/DC
(Hybrids)
4 x HV
OPTICAL LINKS
SOL40
TELL40
LV PS
Temp R/O &
Interlock
HV PS
High-speed control
High speed data
Control signals
Low voltage
High voltage
Monitoring

VeloPix ASIC

- Front-end ASIC driving the design of the VELO data acquisition system
- Operates at LHC clock rate $\sim$ 40MHz
- Designed for high radiation tolerance and low power consumption
- Custom output serialiser - Gigabit Wireline Transmitter (GWT)
- Slow control via SLVS protocol
- 12 VeloPix chips per module
- 20 readout links (more links for hotter chips)

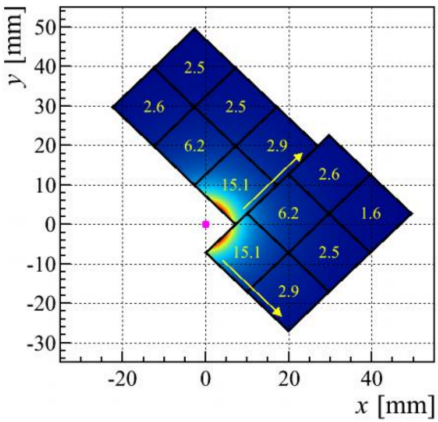


VeloPix ASIC

- Readout is data driven - SuperPixels are *only* read out when they have “hits above threshold” (a.k.a. zero-suppression)
- **Binary readout** @ 40 MHz
- Based on the Timepix3 ASIC
- VeloPix is optimised for high speed readout

Peak hit rate	900 Mhits/s/ASIC
Max data rate	20.48 Gb/s
Total VELO	2.85 Tb/s

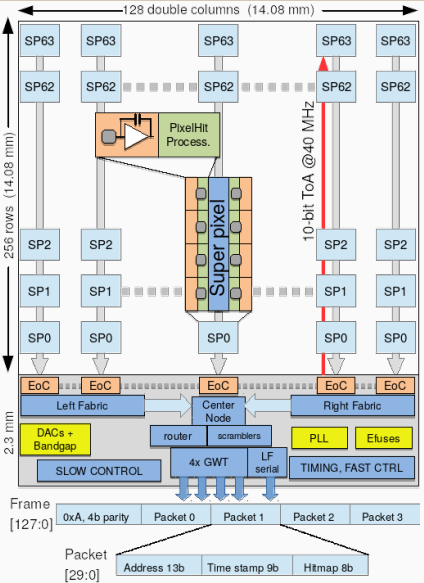
- Power consumption < 1.5 $W{\cdot}cm^{-2}$



Data rate [Gbit/s] for hottest module.

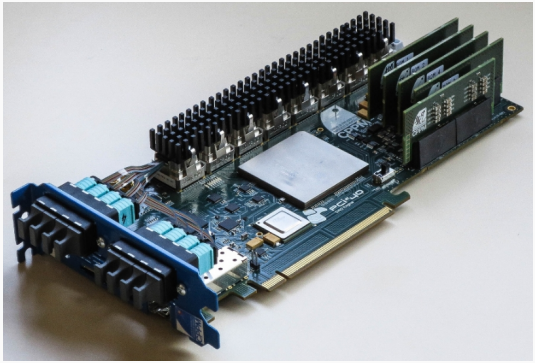
VeloPix Data readout

- Pixel data is aggregated into groups of 2×4 called SuperPixels
  - 30% reduction in data size
- Data is sent out-of-time ⇒ timestamp stored in SuperPixel data packet
- Custom serializer - Gigabit Wireline Transmitter (GWT)
  - Low power - 60 mW
  - 5.12 Gb/s line rate
- GWT protocol
  - scrambled data
  - parity check, no error recovery
  - ⇒ minimise bit error rate



Backend DAQ and Slow Control - PCIe40

- Single control and readout board for the entire experiment
- Can be used for TFC, SC, or DAQ or all
- Common hardware, shared firmware components
- PCIe Gen3 x16
- Intel Arria10 FPGA (10AX115S4F45E3SG)
  - High power consumption - up to 80W FPGA, 157W card
- up to 4 PCIe40 per chassis (ASUS ESC4000-G3, 2x Xeon 3 GHz, 8x 8 GB DDR4)

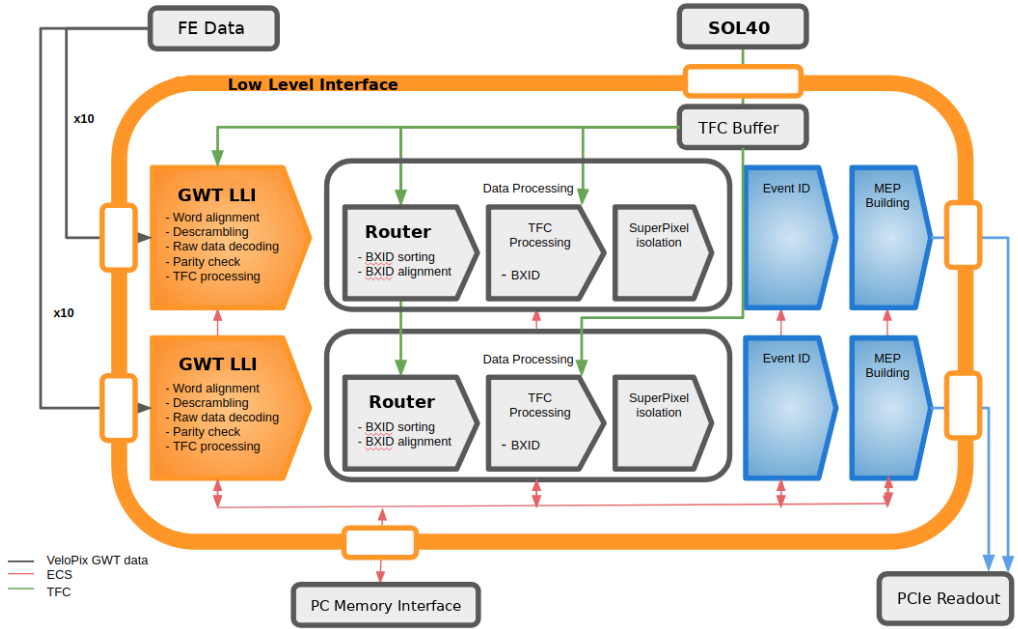


- 48 bi-directional links (or 96 uni-directional) @ ∼5 Gb/s
- Output bandwidth 100 Gb/s (measured).

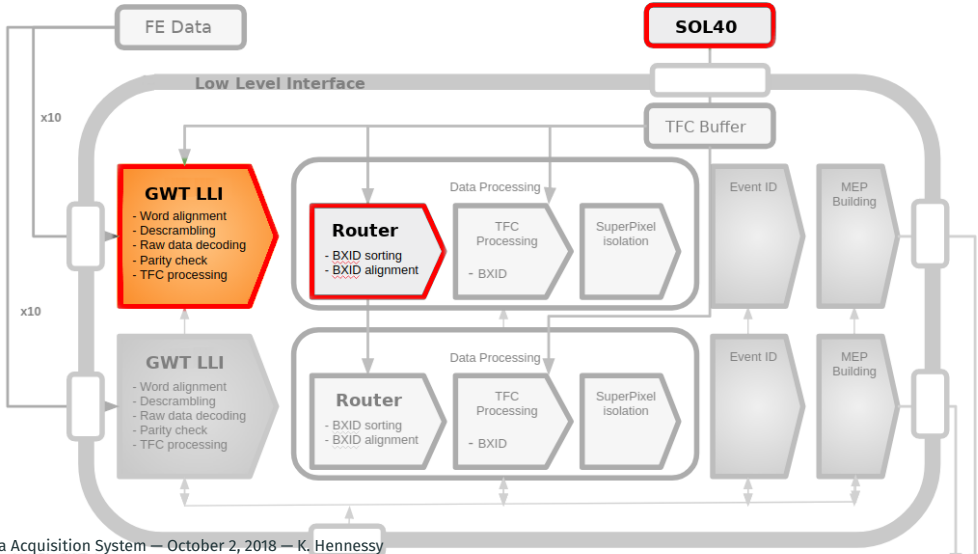
MiniDAQ - All in one solution

- MiniDAQ = PCIe40 + server
- The MiniDAQ platform allows for controls, DAQ, and software all to run in a standalone system
- The server is provided with the PCIe40 installed, necessary programming cables and OM3 fibres
- WinCC JCOP software comes pre-installed (a licence is needed)
- All necessary drivers and support software is installed
- With one server, one can control the front-end hardware and at the same time read out its data.

VELO Firmware


FE Data
SOL40
Low Level Interface
x10
x10
TFC Buffer
GWT LLI
- Word alignment
- Descrambling
- Raw data decoding
- Parity check
- TFC processing
GWT LLI
- Word alignment
- Descrambling
- Raw data decoding
- Parity check
- TFC processing
Data Processing
Router
- BXID sorting
- BXID alignment
TFC Processing
- BXID
SuperPixel isolation
Data Processing
Router
- BXID sorting
- BXID alignment
TFC Processing
- BXID
SuperPixel isolation
Event ID
MEP Building
Event ID
MEP Building
VeloPix GWT data
ECS
TFC
PC Memory Interface
PCIe Readout

VELO Firmware

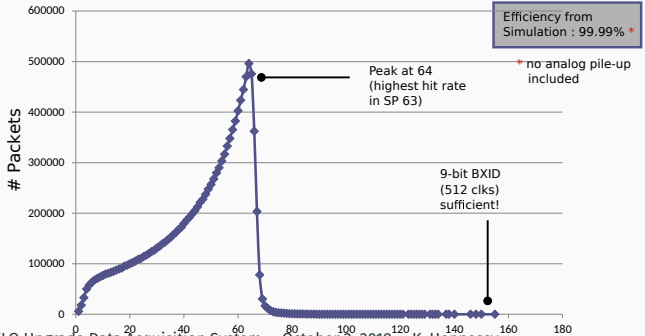


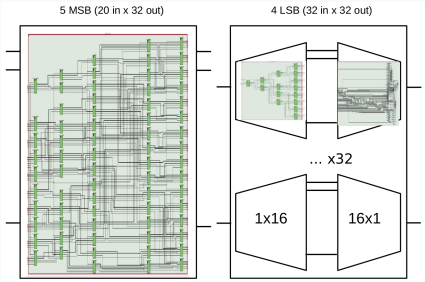
VELO Firmware

- VELO SOL40
  - GBTx is connected directly to the VeloPix rather than through the SCA
  - Requires custom SLVS component in the SOL40 firmware
- GWT LLI
  - GWT word alignment
  - Descrambling
  - Parity check
  - TFC Synchronisation functionality
  - SuperPixel packet extraction
- Router
  - Primary function of the Velo firmware
  - Re-ordering the data in time
- Optional components (if FPGA resources allow)
  - SuperPixel Isolation flagging (proto-clustering)
  - Phi Ordering

BXID Router

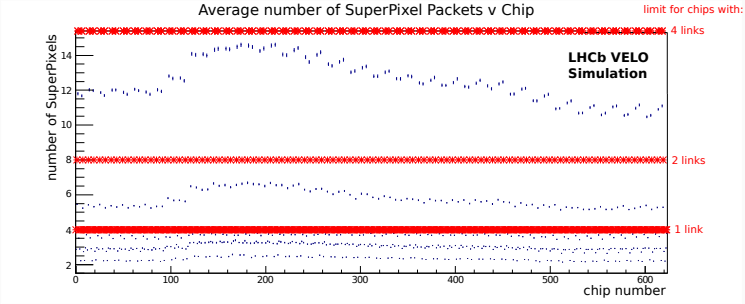
- Time-ordering SuperPixel data
  - 9-bit router sorts data 1 bit at a time
  - Extensive simulation required - both to maximise speed (>160 MHz) and minimise FPGA resource usage
  - Latency limit < 512 clock cycles

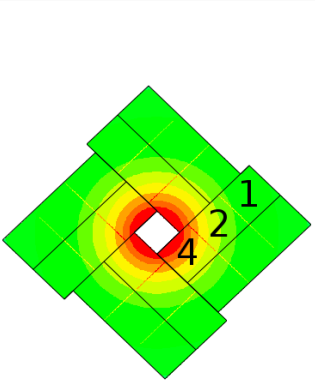




VeloPix Simulation/Emulation

- Emulating VeloPix using LHCb Monte-Carlo data
  - Software emulation for simulation
  - Hardware emulation using FPGA (Xilinx VC709)

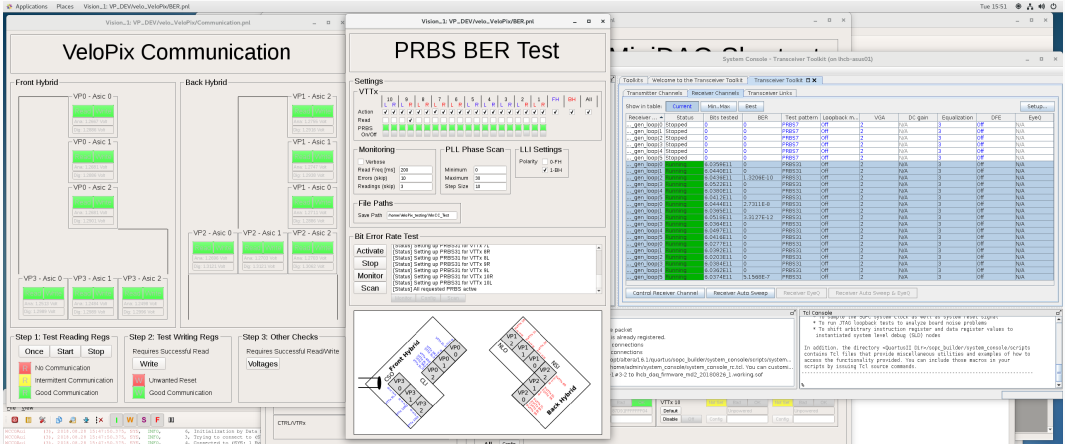




Software and Testing

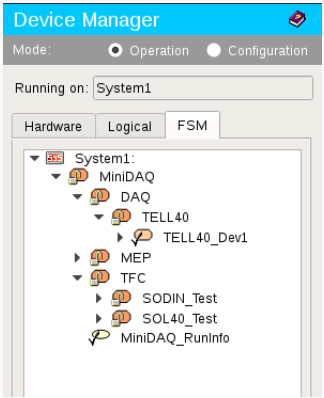
ECS Software

- Software for configuring the electronics and readout
- Joint COntrols Project @ CERN (JCOP)

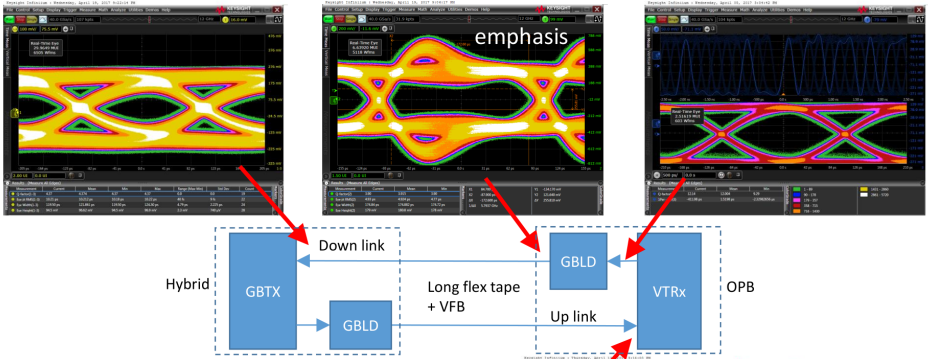


ECS Software

- Control system modelled with finite state machine tree
  - commands propagate down; status propagates up
- Integrates with SOL40, TELL40, SODIN
- Can integrate with COTS hardware (CAEN, ISEG, Wiener...)
- Rapid development
- Oracle database backed
- Archiving, trending, alarm functionality...



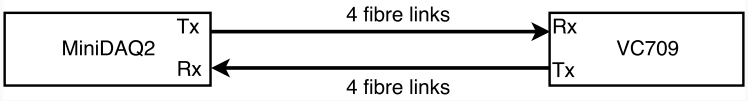
Link Performance



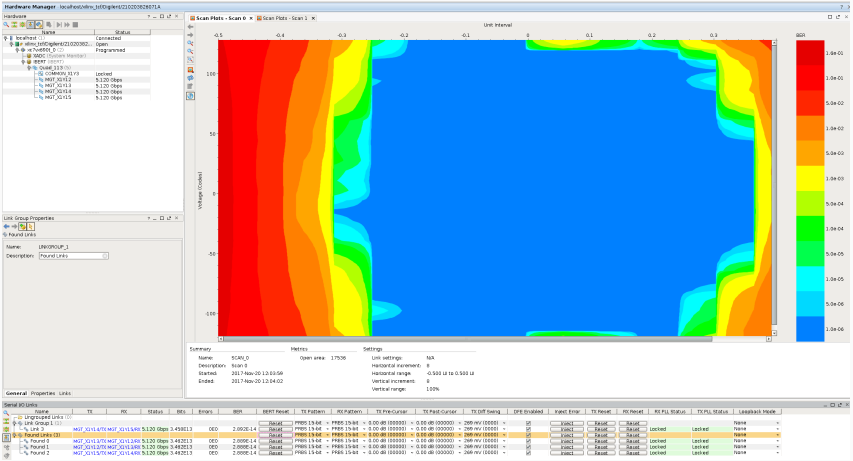
- Good eye quality.
- GBLD works excellent as line driver with emphasis.
- Some degradation in final setup due to some more trace length in OPB, VFB and hybrid.
- Will add a CTLE (on OPB) to improve eye.
- The GBLD can still amplify by factor 2.

MiniDAQ2 Transceiver testing

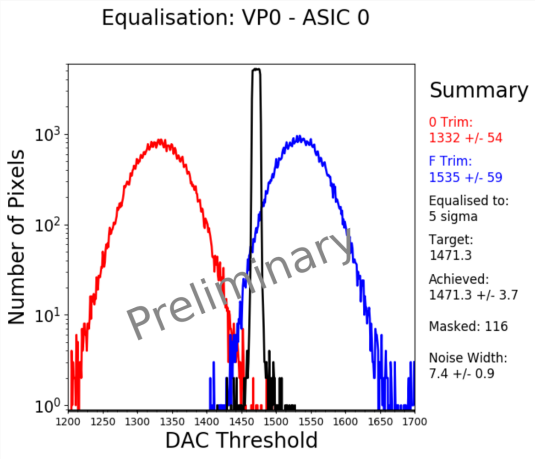
- Goals
  - Mitigate the kind of transceiver problems seen with MD1
  - Generate working transceiver block for GWT with 240 MHz reference (change from MD1)
- Use PRBS signals between VC709 Xilinx board and MD2
- Use *independent clocks* and recover signals in both directions

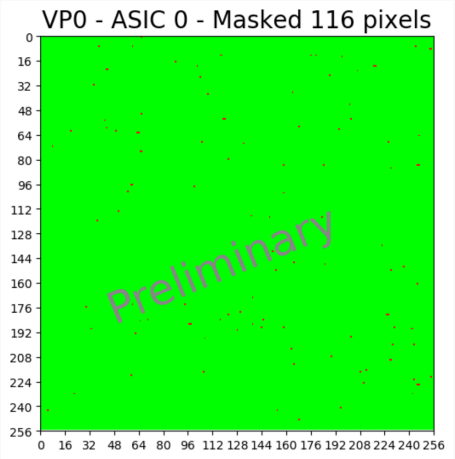


MiniDAQ2 Transceiver testing



VELO Module Testing





Concluding remarks

- LHCb Upgrade using GBT and PCIe40 platforms
  - Uniformity of hardware
  - Large knowledge base
- PCIe40/MiniDAQ platform allows common hardware but custom “user” firmware
- Exploited for VeloPix with many customisations whilst profiting from common LHCb developments
- Future work - FPGA vs. CPU
  - LHCb @ 40 MHz puts huge demand on computing
  - Must endeavour to exploit FPGA *where possible*

Backup

Links

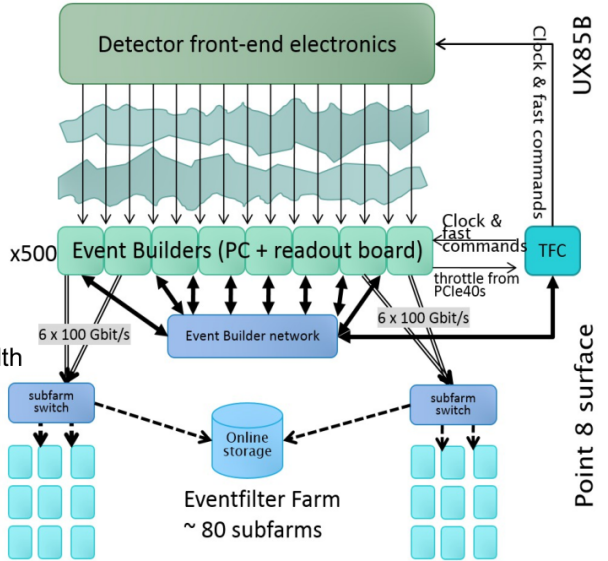
- More info at GBT Project

SCA

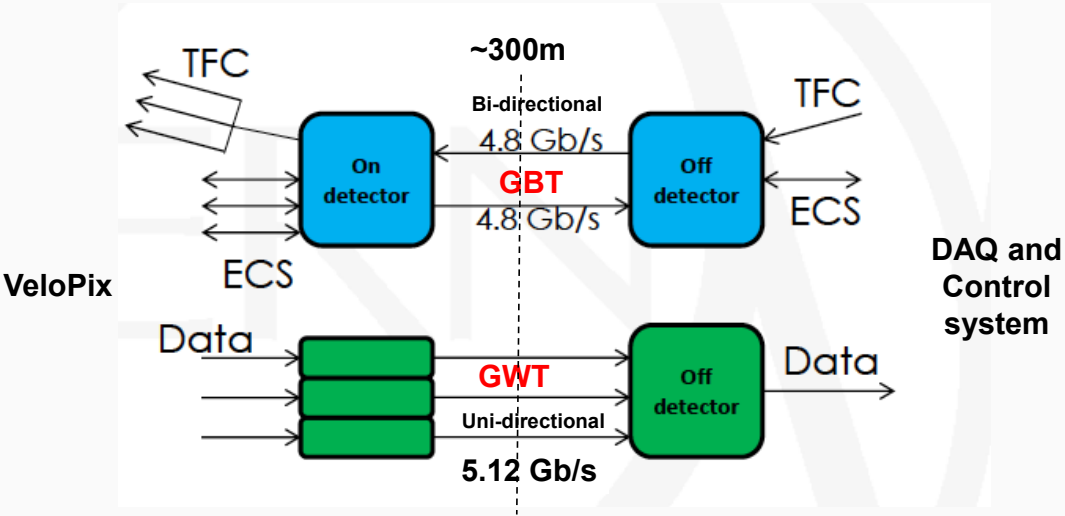
- Companion to the GBT is the Slow Control Adapter (SCA)
- Implements multiple protocols
  - 16x I^2C, 8x SPI, 1x JTAG, 31x GPIO
  - 31x ADCs and 4x DACs

Architecture

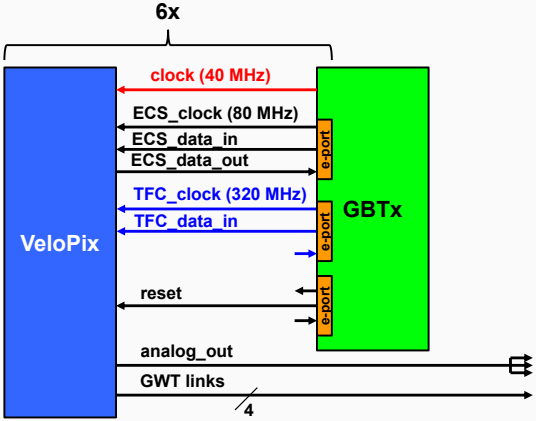
- Readout located on surface
  - Distance between FE and RO : ~350m
- ~15000 optical links
- ~ 500 readout boards
- ~24 links in average on each board
- ~100 kbytes per event
- ~32 Tb/s aggregate bandwidth



VeloPix Links



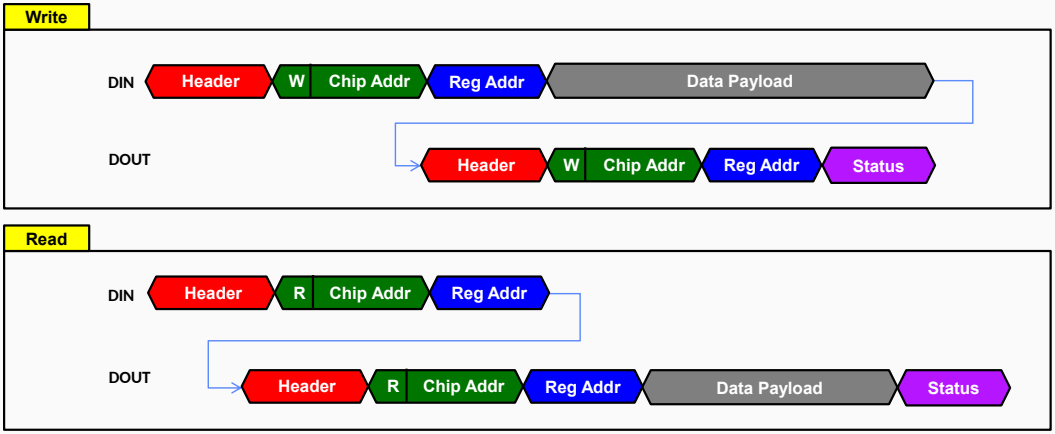
VeloPix Hybrid - ECS

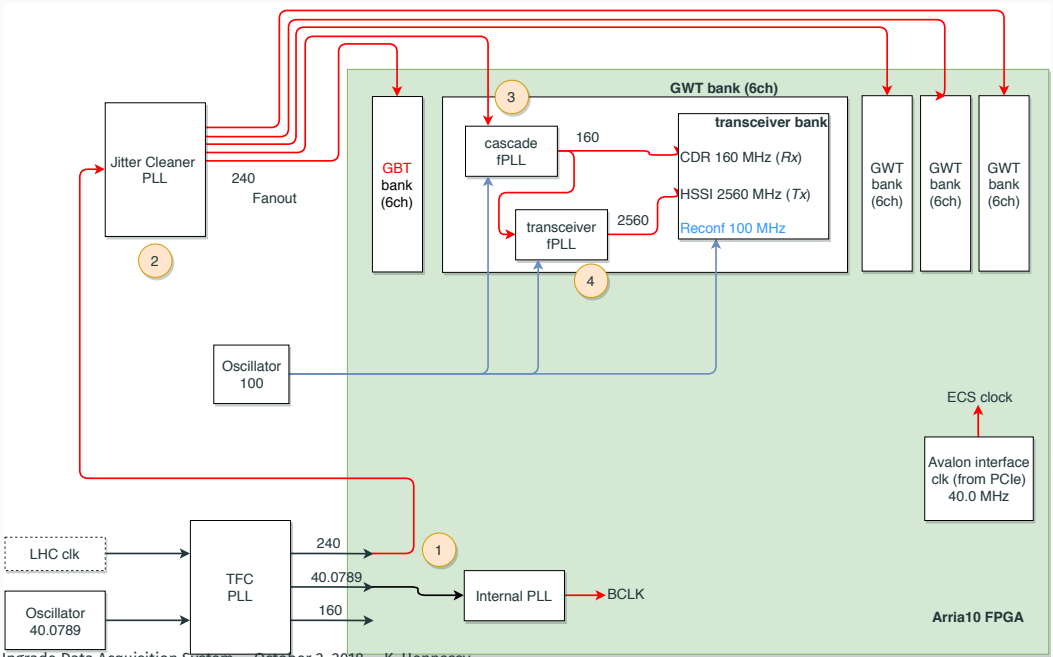


	half-scale	full-scale
TFC	3	6
ECS	3	6
[illegible]	2	4

- Baseline - 1 GBTx + 1 SCA
- NO SCA for Front-end ASIC
- Connecting GBT e-ports directly to VeloPix ASIC
- Requires custom SOL40 firmware
- GBT/Ctrl Hybrid prototype - Jan
- VeloPix Hybrid prototype - May

VeloPix - ECS


Write
DIN
Header
W
Chip Addr
Reg Addr
Data Payload
DOUT
Header
W
Chip Addr
Reg Addr
Status
Read
DIN
Header
R
Chip Addr
Reg Addr
DOUT
Header
R
Chip Addr
Reg Addr
Data Payload
Status


GWT bank (6ch)
transceiver bank
Jitter Cleaner PLL
240
Fanout
GBT bank (6ch)
cascade fPLL
160
CDR 160 MHz (Rx)
HSSI 2560 MHz (Tx)
transceiver fPLL
2560
Reconf 100 MHz
GWT bank (6ch)
GWT bank (6ch)
GWT bank (6ch)
1
2
3
4
Oscillator 100
ECS clock
Avalon interface clk (from PCIe) 40.0 MHz
LHC clk
Oscillator 40.0789
TFC PLL
240
40.0789
160
Internal PLL
BCLK
Arria10 FPGA