protoDUNE-SP Cold Electronics Status

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representing the Cold Electronics team

protoDUNE DAP Meeting
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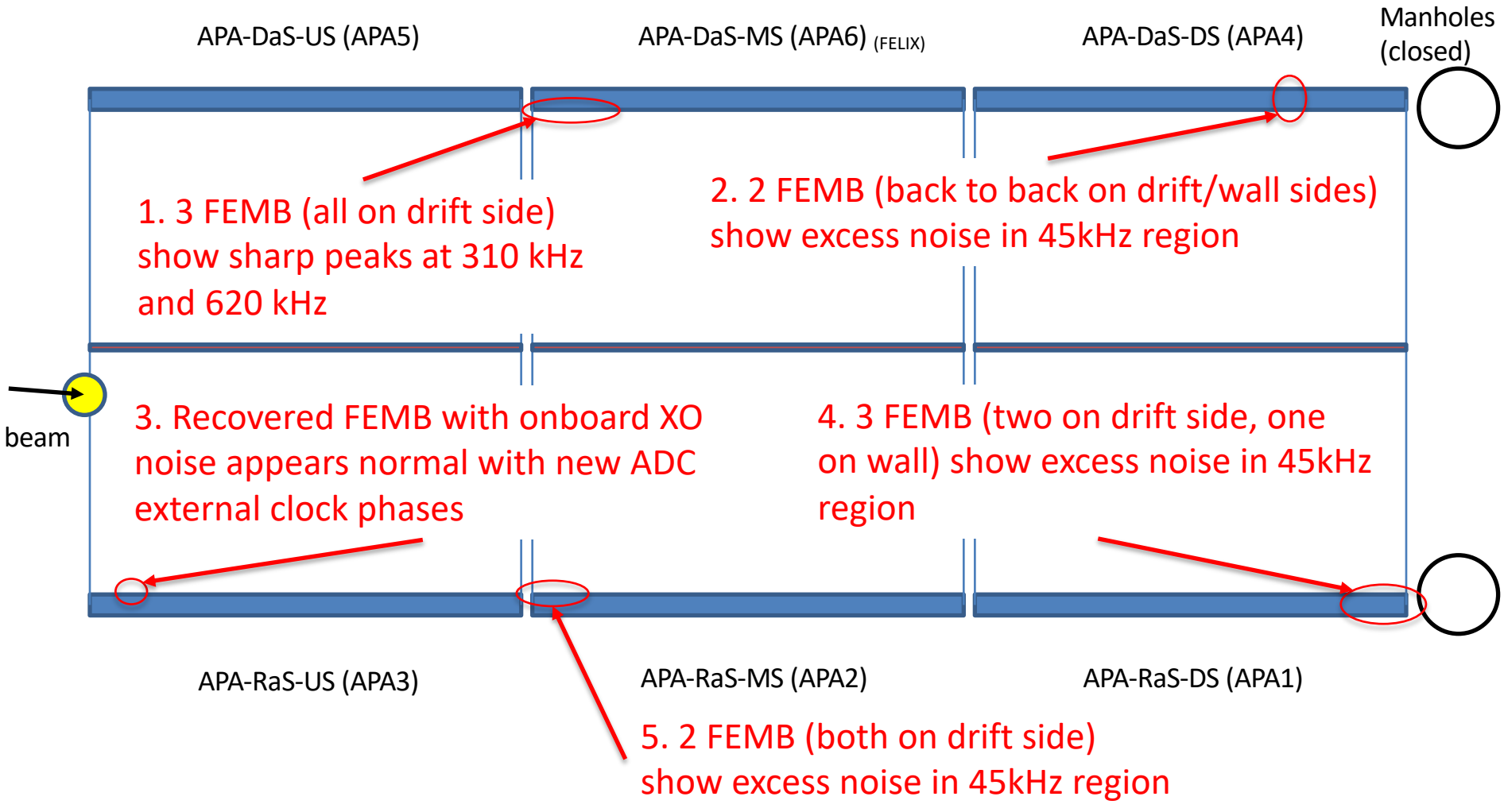
Last Week's Activities

- FEMB submerged in LAr on 9/10
  - Noise monitored by DAQ runs
- Filling complete around 01:00 9/13
  - Took CE expert data on all APAs on 9/13
- Drift HV to -120kV on 9/13
  - Wire bias ramped proportionally
  - Noise monitored by DAQ runs
  - Held stably overnight
  - Took CE expert data on all APAs on 9/13
- Took CE expert data on all APAs on 9/16
  - No drift, wire bias = 50% and 100% of nominal

protoDUNE-SP noise status

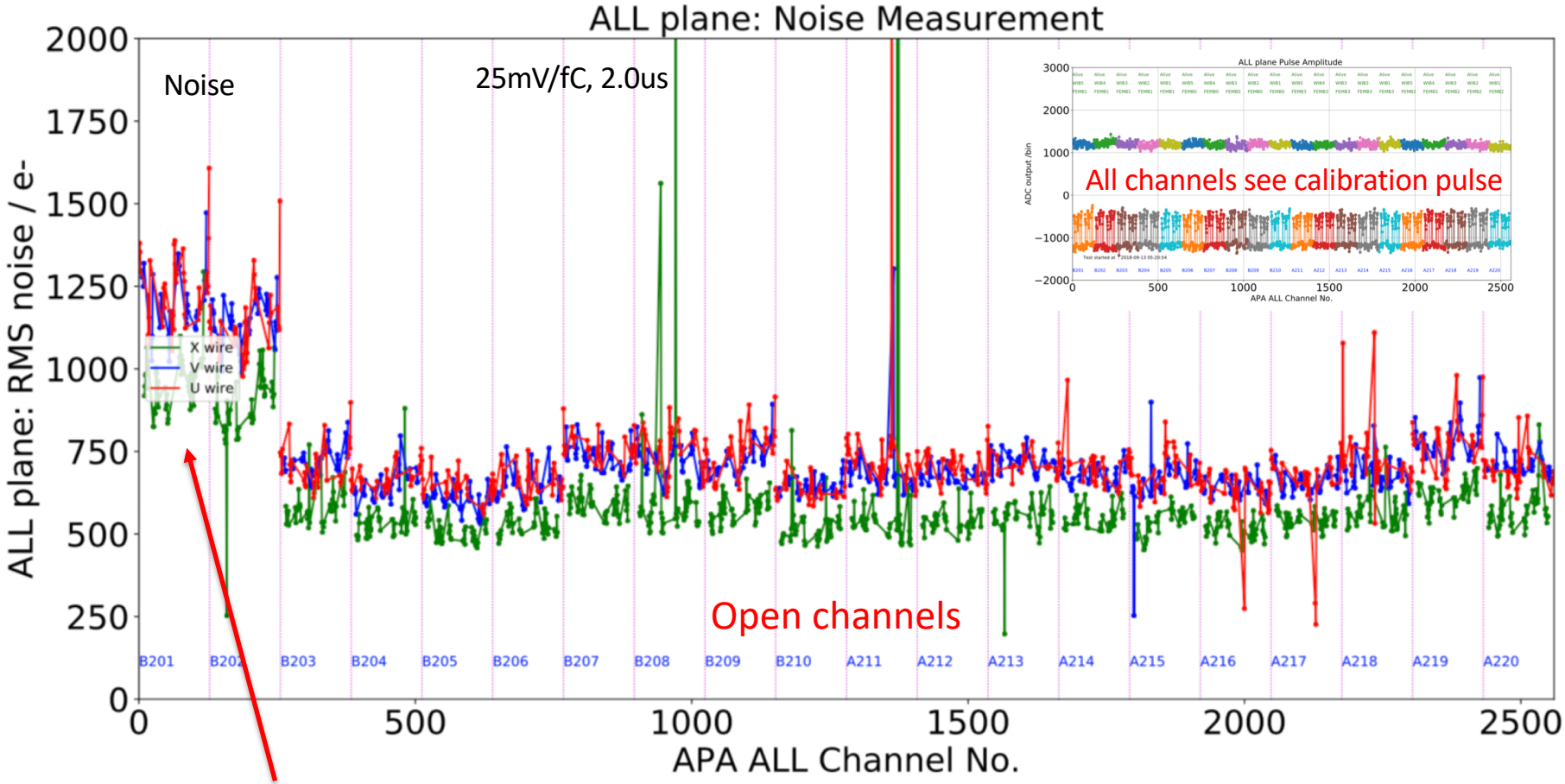
Using 9/13 expert data (DAQ noise is consistent)



9/13 Detector Status

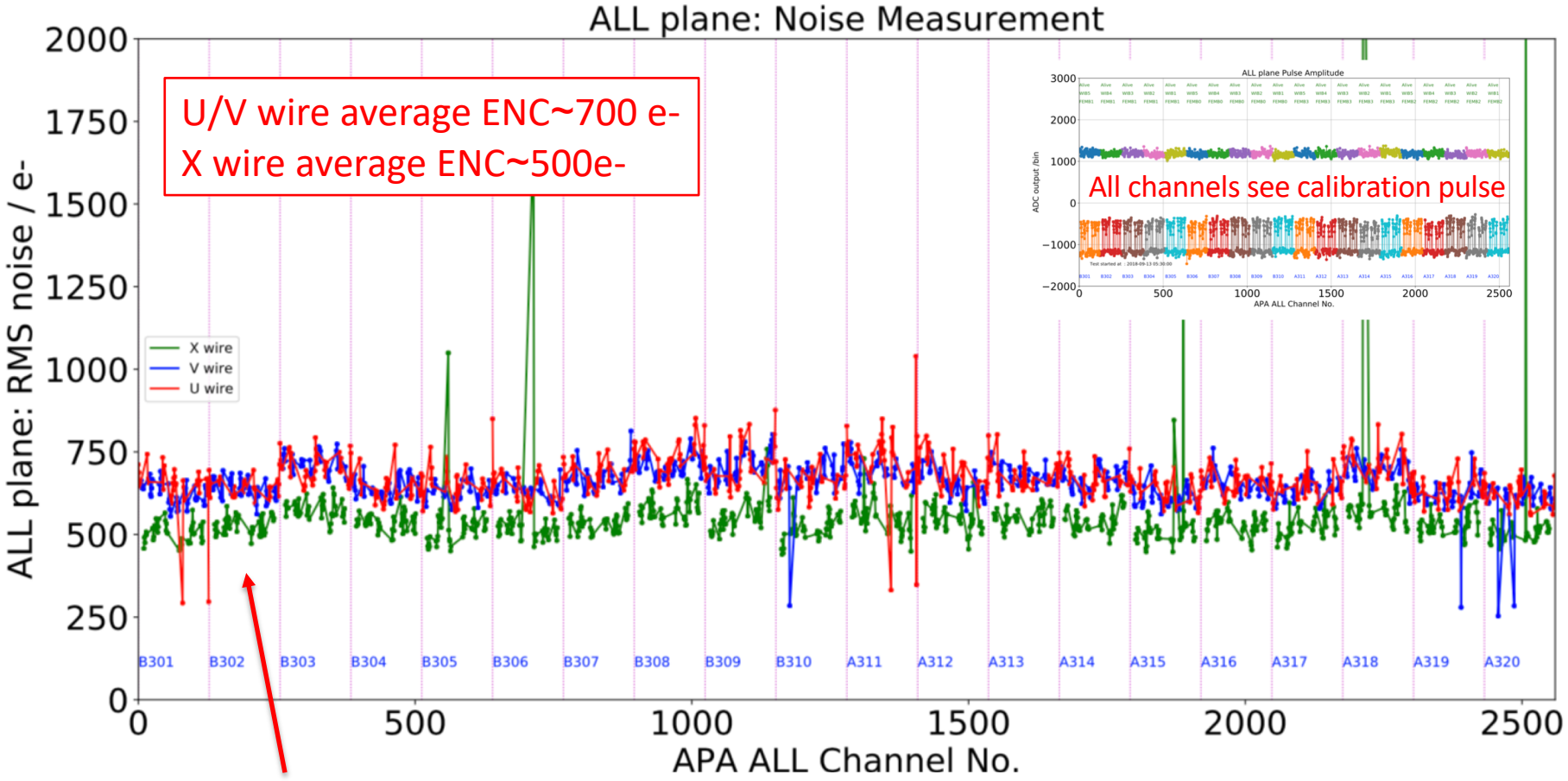
- For CE expert DAQ runs:
  - LAr filled, no recirculation
  - All FEMBs on
  - Drift HV = 0kV
  - Wire bias = 0V, all planes
  - Cameras on
  - LEDs off
  - PD and PD bias off

APA2 (from 9/13)



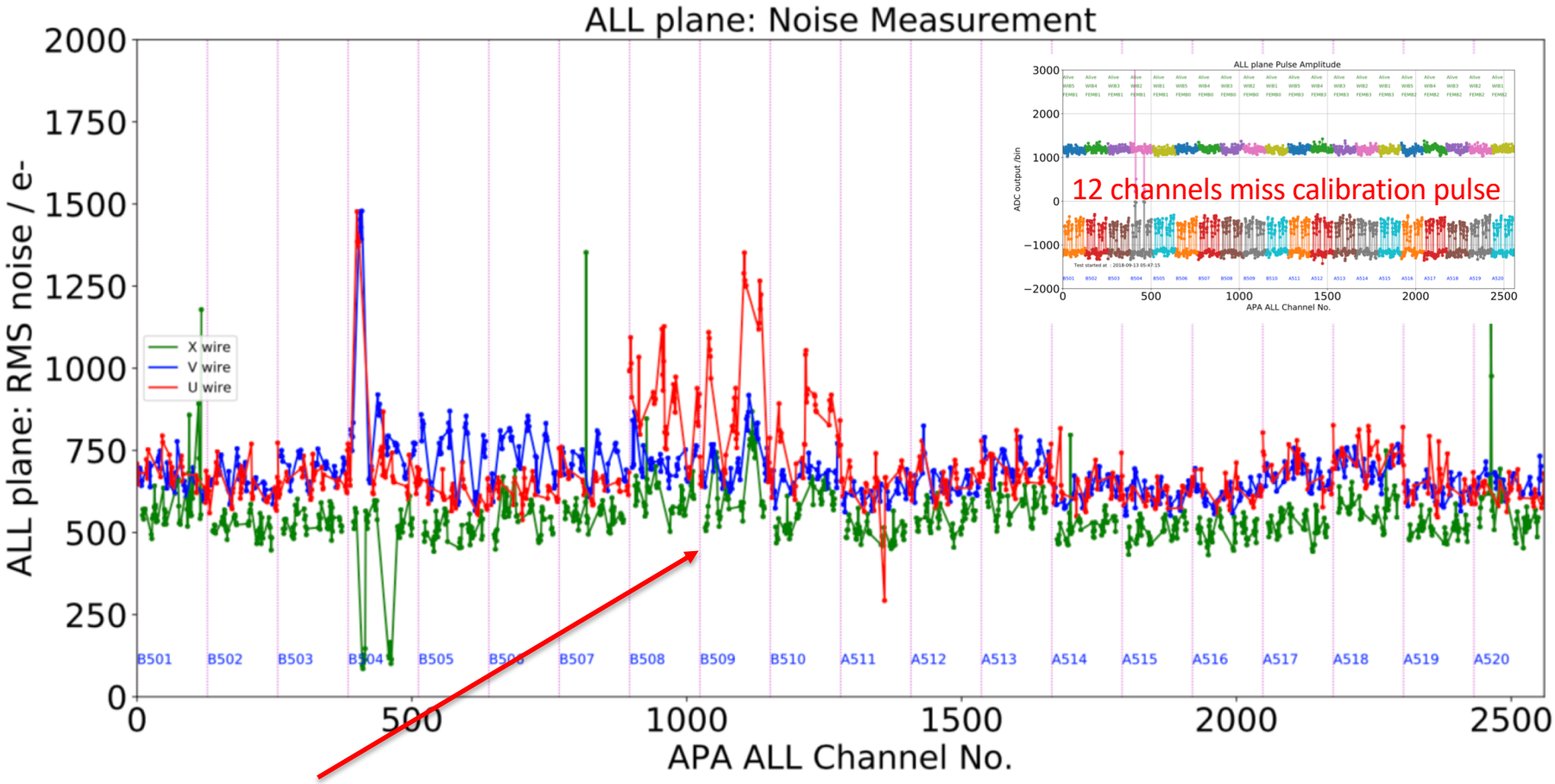
5. 2 FEMB (both on drift side) show excess noise in 45kHz region
Tested twice without power cycle, same result

APA3 (from 9/13)



3. Recovered FEMB with onboard XO, noise appears normal with new ADC ext. clock phases

APA5 (from 9/13)



1. 3 FEMB (all on drift side) show sharp peaks at 310 kHz and 620 kHz

CE 9/13 Status

- Known issue with WIB304FEMB2: OK
  - Recovered with onboard oscillator clock
  - Applied new ADC clock phases has made effects from sticky codes the same as other FEMB, noise is consistent
- APA1, 1 ADC ASIC has a sync indicator error: OK
  - However, data from this ADC is good, bypassed error in DAQ configuration
- APA4, 1 FE-ADC SPI readback fails: OK
  - However, FE-ADC can be configured, bypassed error in DAQ configuration
- APA5, abnormal FE baseline at 200mV setting: checking
  - Collection channels of 2 FE ASICs on WIB502FEMB2 were inactive
  - Possibly ASICs not starting up in good configuration
  - Might be recovered by setting internal FE baseline to 900mV

CE 9/16 Status

- Abnormal FE baseline at 200mV setting: checking
  - Now effects 6 FE ASICs
  - Does not seem to be correlated to HV ramp or beam: most occurred after first ASIC power cycle before ramp
  - Checking if 900mV baseline setting is ok after power cycle
- Sync loss on ADCs: checking
  - 7 ADCs have abnormal RMS that looks like a sync loss even if the chip reports in sync during configuration
  - Some were present at cooldown, some appeared after the first CE power cycle
  - Can be fixed by new ADC sync phases
- WIB105FEMB2 appears to have lost I2C control: OK
  - Swapped 2 WIBs and all control lines worked properly
  - Likely a bad connection between WIB and backplane
- 2 inactive channels (1 on APA1 and 1 on APA6) appeared: BAD
  - No response to internal FE calibration circuit
  - Need to cross check with DAQ data

Summary

- Cryostat filled and HV tests ongoing
- In progress diagnosing and recovering CE issues
  - Open channel numbers consistent with Cold Box
- Overall noise performance on very promising
  - X;U/V wire average ENC~500;700e- on all APAs
  - Except for localized “hot spots”
- Data analysis of expert runs with drift HV = 120kV; PD on; wire bias at 50% and 100%, all planes is ongoing
  - Will update with more results
- Offline group is analyzing all runs from the DAQ
  - Results broadly consistent with CE expert data
  - See David’s slides