DUNE FD Data Selection System: Baseline, Options, and Downselect Timeline

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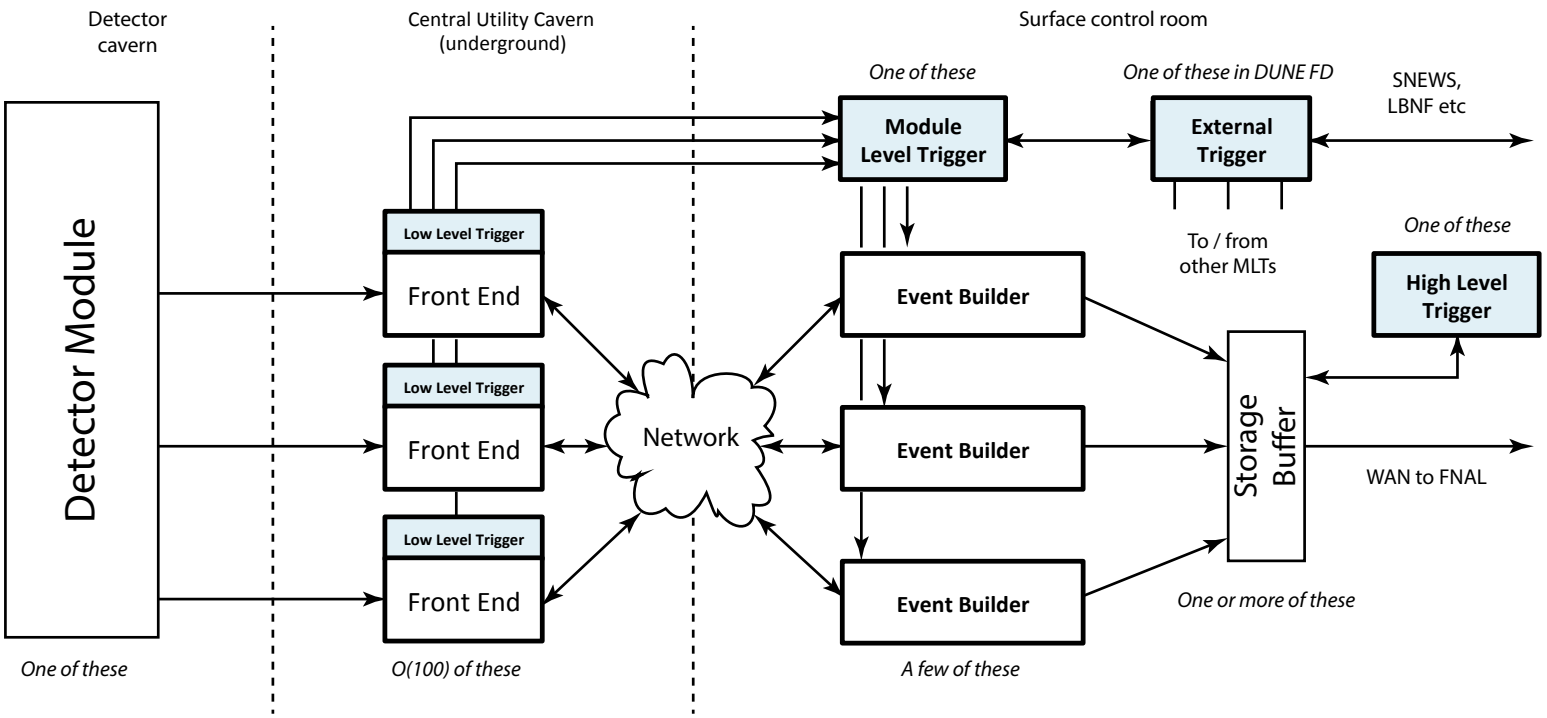
Baseline/Options: Same Conceptual Design



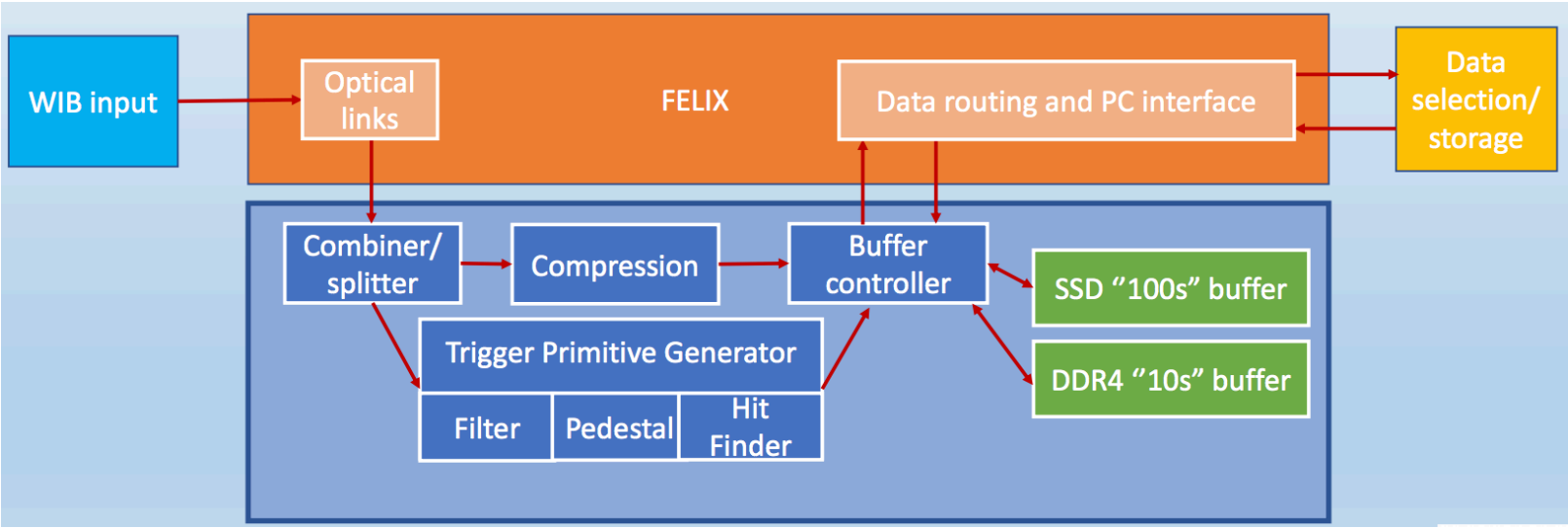
Difference: In implementation of Low Level Trigger

Baseline

- TDR baseline

Felix + FPGA co-processor

Trigger Primitives formed in FPGA and aggregated into Trigger Candidates in CPU (part of Low Level Trigger)



Other Low Level Trigger options currently explored

1. Felix + CPU
    1. Trigger Primitives formed in Felix FPGA, data stored in server memory, TP aggregated into Trigger Candidates in host server CPU
    2. Minimal data reorganization in Felix FPGA, data stored in server memory, TP generated and aggregated into Trigger Candidates in CPU

2. Felix + GPU

    (if power utilization, i/o overhead is viable)

    Optional pre-processing in Felix

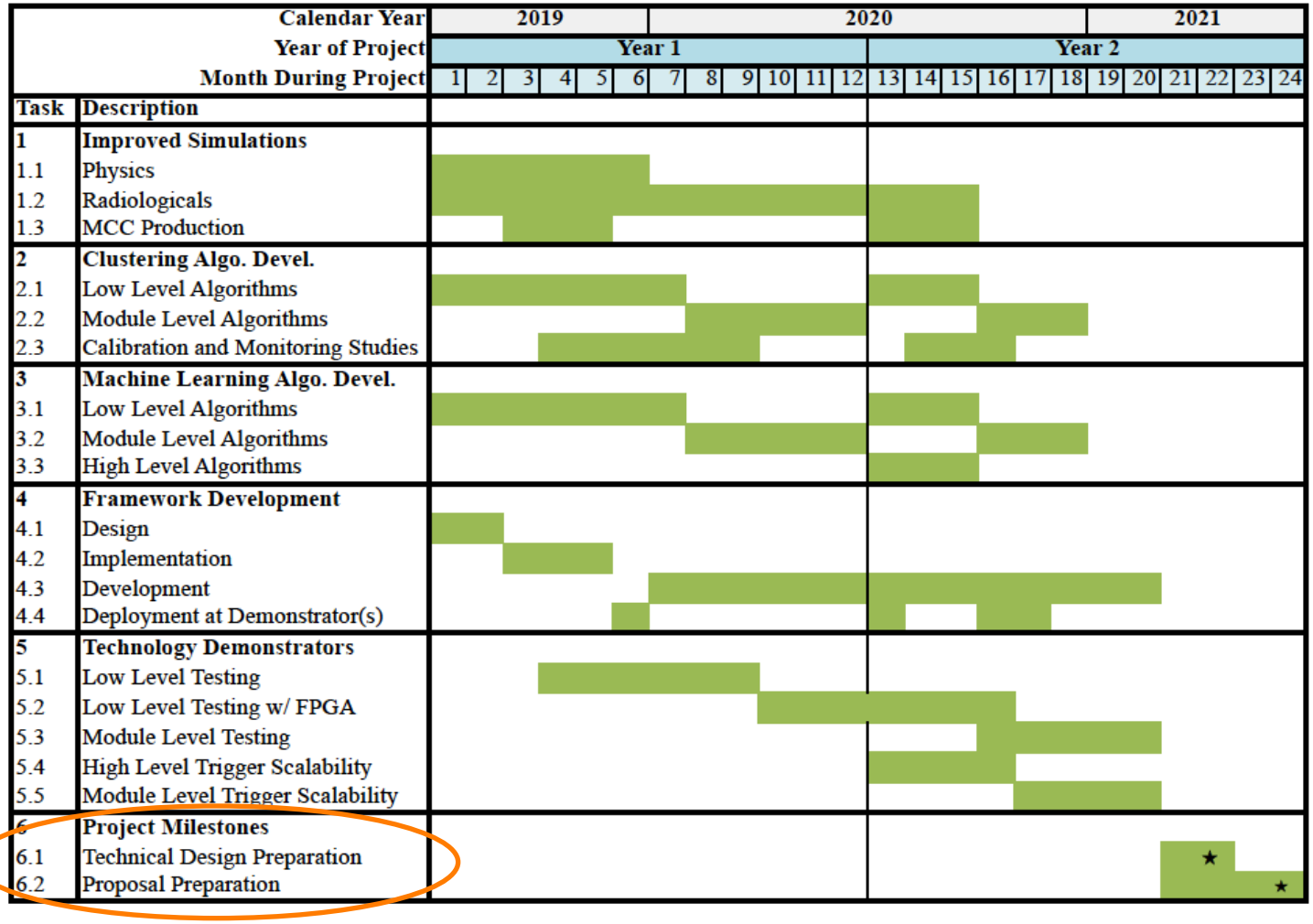
    Ideas being explored are CNN online classification, w/ or w/o a priori ROI localization

Data Selection System

Current thinking for baseline:

- Overall scheme for online data selection implementation: Distributed applications which talk to each other bidirectionally across trigger levels over network offers option for dynamic Low Level Trigger reconfiguration (depending on implementation)
- Low Level Trigger sends TC's to Module Level Trigger over network.
- Module Level Trigger is a single server; it aggregates TC's over full module and makes trigger decision; distributes it to Back-end DAQ.
- MLT decision: TC's accumulated over a "sliding window of time". Will likely choose to wait before Trigger Command distribution sufficiently long (TBD, up to "10 sec buffer – decision latency") to avoid overlap of triggers and duplication of streams.

Seeking NSF support for development & design



Seeking NSF support for development & design: Timeline for Technology Demonstrators

	Calendar Year	2019						2020												2021					
	Year of Project	Year 1												Year 2											
	Month During Project	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Task	**Description**																								
5	**Technology Demonstrators**																								
5.1	**Low Level Testing**																								
	Design and Component Procurement																								
	Construction																								
	Framework Deployment																								
	Demonstration with Fake Data																								
5.2	**Low Level Testing w/ FPGA**																								
	FPGA Co-processor Integration																								
	Fake Data Demonstration Tests																								
5.3	**Module Level Testing**																								
	Design and Component Procurement																								
	Construction																								
	Framework Deployment																								
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	Fake Data Demonstration Tests																								
5.4	**High Level Trigger Scalability**																								
	Spec./Procurement of HPC Allocation																								
	Deployment at HPC node(s)																								
	Fake Data Demonstration Tests																								
5.5	**Module Level Trigger Scalability**																								
	Spec./Procurement of HPC Allocation																								
	Deployment at HPC node(s)																								
	Fake Data Demonstration Tests																								

Additional ongoing efforts within consortium

- FPGA co-processor development and algorithm simulations (UK)
- Felix development (CERN, Nikhef, BNL, PNNL, …)