The DAQ Front-end

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DUNE CDR: DAQ Review

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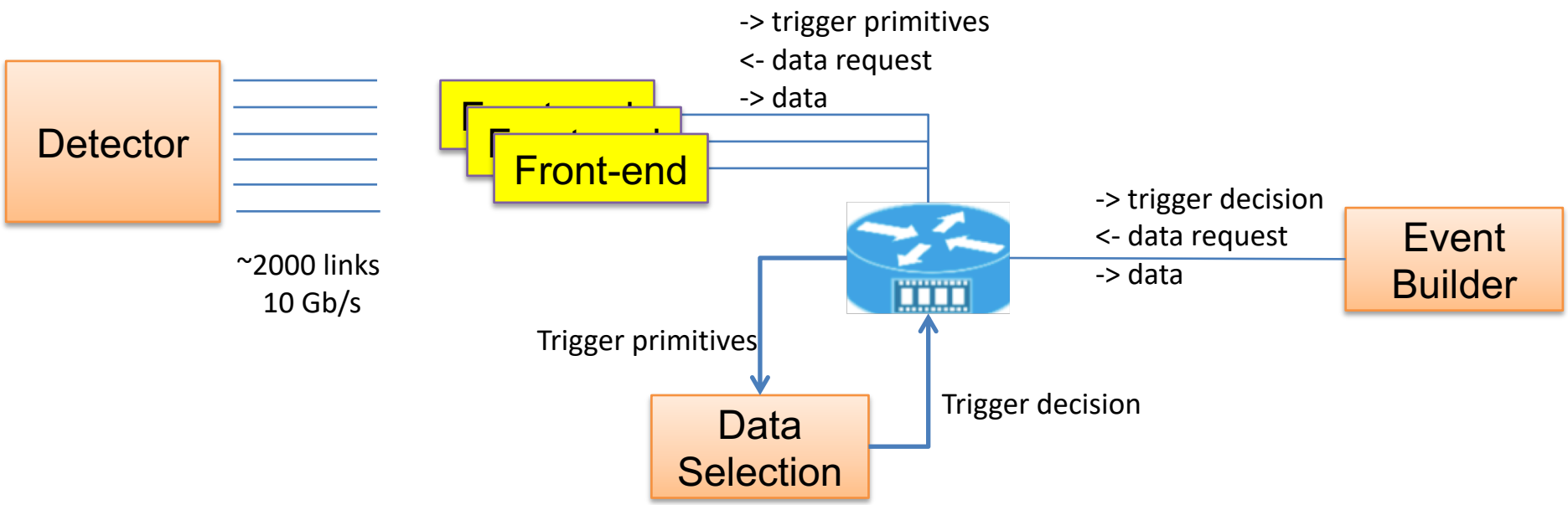
EP-DT
Detector Technologies

Content

- The DUNE DAQ front-end system and its interfaces
- Requirements and specifications
- Technical constraints, key challenges
- System design
- Any validation / simulation already done (e.g. in ProtoDUNE)
- The development plan up until the EDR
- The production plan following the EDR

The DUNE Front-end System

- Receives data over point-to-point links from the detectors
- Generates trigger primitives and forwards those to the Data Selection
- Buffers the data
- Responds to data requests from the Event Builder



Requirements

- Receive data over 10 Gb/s optical point-to-point links
- Produce trigger primitives at a granularity of 1 APA
  - Trigger primitive = channel address, time of hit, time over threshold, ADC sum, error flag, …
- Send trigger primitives over a switched network to the Data Selection (DS) system
- Buffer data for sufficient time to allow the DS to take a decision and the event builder (EB) to make a data request (10+ seconds)
- Upon reception of data request (switched network)
  - ”normal trigger”: reply to the EB with data corresponding to the requested time window and detector area
  - “SNB trigger”: transfer requested (past + future) data to non-volatile storage and start sending out data to the EB

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Constraints, key challenges

- The Front-end system will be housed in the CUC
  - Space:
    << 12 racks per module (aiming at 3-4 incl. patch panels and NW)
  - Power:
    < 100 kVA per module (aiming at 60 kW incl. NW)
  - Accessibility:
    Limited, i.e. full remote control capability needed (power cycling, reprogramming, stand-by nodes, …)
- High performance I/O and compute system
  - Detector input (~1.5 TB/s)
  - Primitives generation (FW or SW)
  - Intermediate buffer of ~15 TB with throughput of ~2 TB/s
  - Non volatile buffer of ~150 TB with throughput of ~1.5 TB/s
  - Network connectivity to DS + EB (10 Gb/s)

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System design

- Modular design of many identical components
- Servers (CPU+NW), volatile and non volatile buffers, FELIX cards, co-processor
- Subdivision of tasks:
  - Server deals with network I/O (to DS, to/from EB), control, configuration, monitoring, primitives generation, data buffering
  - FELIX deals with data reception from detectors, data exchange with co-processor and server
  - FELIX possibly relays control, config, monitoring to/from detectors
  - Co-processor performs data re-organization, noise filtering, primitives generation, data buffering

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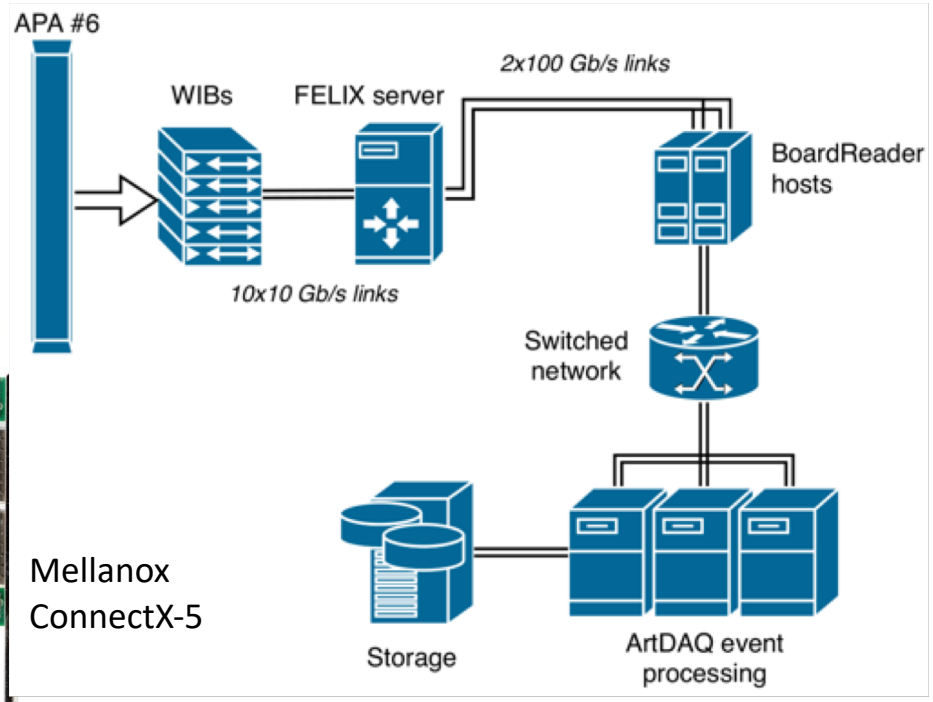
System design

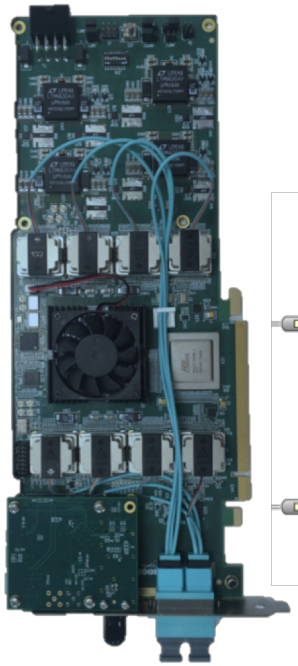
- Possible implementation scenario for one Front-end unit:
  - 1 FELIX card per server
  - 1 co-processor
  - 256 GB volatile RAM, 2 TB non-volatile storage
- 75 readout units needed for SP module

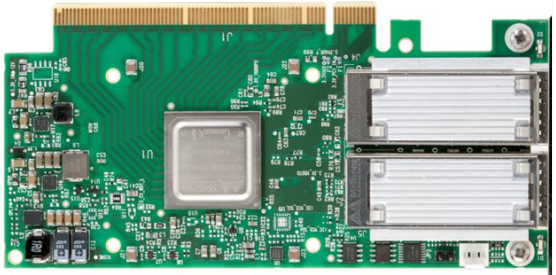
FELIX based readout in ProtoDUNE

- P-to-p link throughput ✓
- 10 links -> host memory over 1 FELIX card ✓
  - Need to switch to PCIe4 or greater to do 20 links
- HW aided data compression using Intel QAT technology ✓

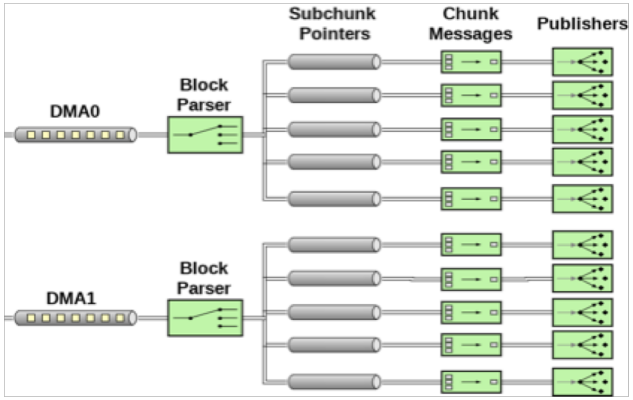


FLX-712 card





Mellanox ConnectX-5



- Full I/O over InfiniBand for ProtoDUNE ✓
  - Need much less network I/O for DUNE
  - Need longer and high throughput storage (but new technologies like 3D XPoint go in the right direction)
    - Joint R&D with ATLAS, CMS, DUNE and Intel on DAQ DB

Ongoing work with ProtoDUNE

- Data re-ordering in FELIX FW: split channels by wires planes to facilitate hit finding (only on collection plane used for triggering)
- Hit finding in software (and generation of sw trigger)
- Hit finding in standalone co-processor (and generation of sw trigger)
- HW layout of demonstrator FELIX card
- Any development will be deployed and tested at ProtoDUNE with data provided by the installed APAs and electronics.

Development plan up to EDR

- Use ProtoDUNE-SP as Front-end test stand
  - Complete ongoing work and demonstrate all building blocks of the DAQ Front-end
  - Determine the best sharing of duties among SW/FW/HW
  - Aim at self-triggered readout of ProtoDUNE by Q1 2020
- Refine interfaces with detectors
  - Only readout or also control, config, monitoring?
  - Data format and transport protocols
  - Try out prototype implementations with WIBs/PD electronics

Production plan following EDR

- Final FELIX card layout -> Q1 2021
  - FW, SW development & integration
- Test boards, test servers -> Q4 2021
  - FW, SW testing & optimization
- Pre-production -> Q2 2022 (also for detector commissioning)
  - Overall readout system validation
- Production -> Q2 2023
  - Installation and commissioning