FPGA co-processor

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Introduction

- Co-processor will take care of data compression and trigger primitive generation

- Co-processor will also perform data buffering for supernova trigger

- Sits on FELIX cards and processes data from warm interface boards (WIBs) before it is passed to PCs

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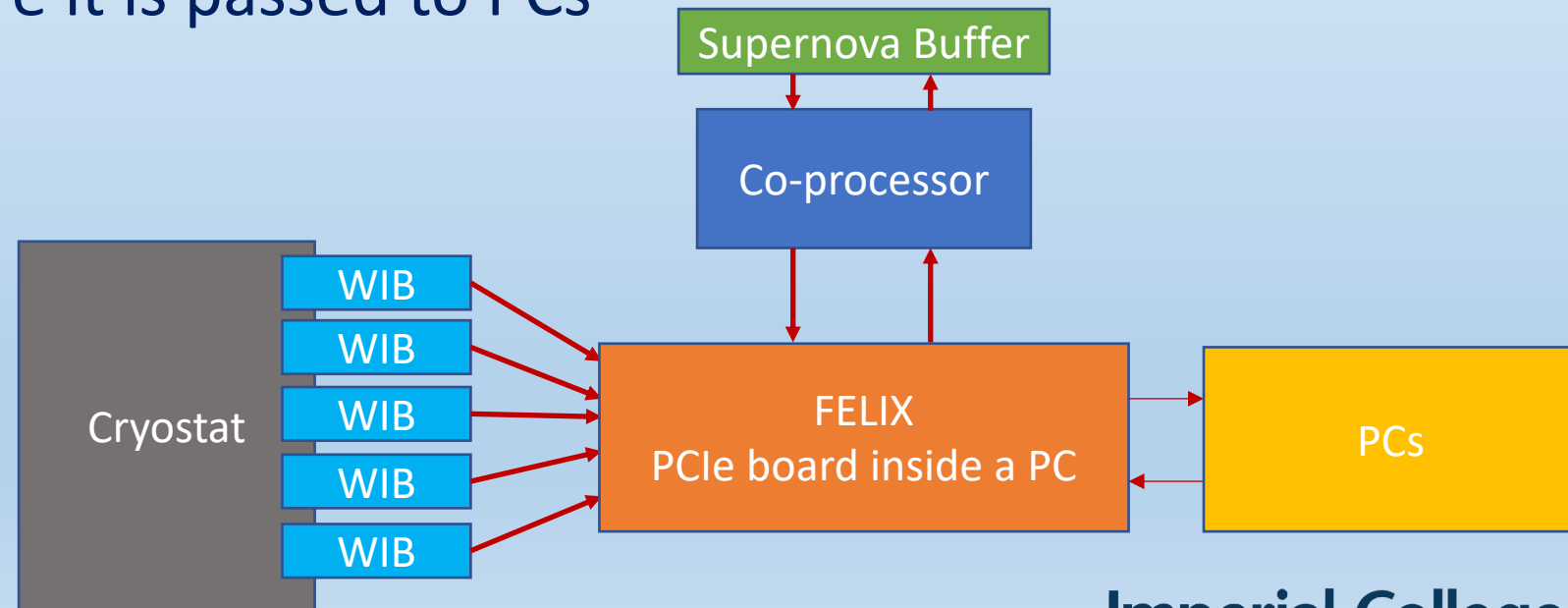
Requirements and specifications

- On receipt of supernova trigger must be able to record 100s of full waveform data including O(10s) before the trigger signal

- Must buffer data until non-supernova trigger decision can be made and read out selected events to back-end

- Should compress data losslessly by at least a factor of 2

- Must form trigger primitives (filtered waveforms, hits etc.)

- Need a software framework that can control, configure and monitor the health of the board and detector via trigger statistics

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Interfaces, constraints

- Input via FELIX card covers one APA using 10x10 Gb/s optical links from WIBs
  - Contains data from 2560 channels sampled at 2MHz 12 bit
- Board will contain 64 GB of DDR4 RAM for the O(10s) buffer
- Board will contain 2 NVMe SSDs for 100s buffer
  - Each drive has a 4x Gen3 PCIe interface
- Firmware and software currently being developed using a dev board
- Final production will be a daughter card mounted on FELIX

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Key challenges

- Demonstrating correct/adequate performance with a realistic LArTPC
- Optimise split of functionality between FPGA and CPU given stringent power constraints
- Produce hardware with sufficient reliability to meet system requirements and verify this (i.e. design adequate QA processes)
- Most of these challenges can be met through extensive testing of the system at ProtoDUNE

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System design

- Board will have parallel instances of TPG (15 instances) and Compression blocks (40 instances) each processing 64 channels
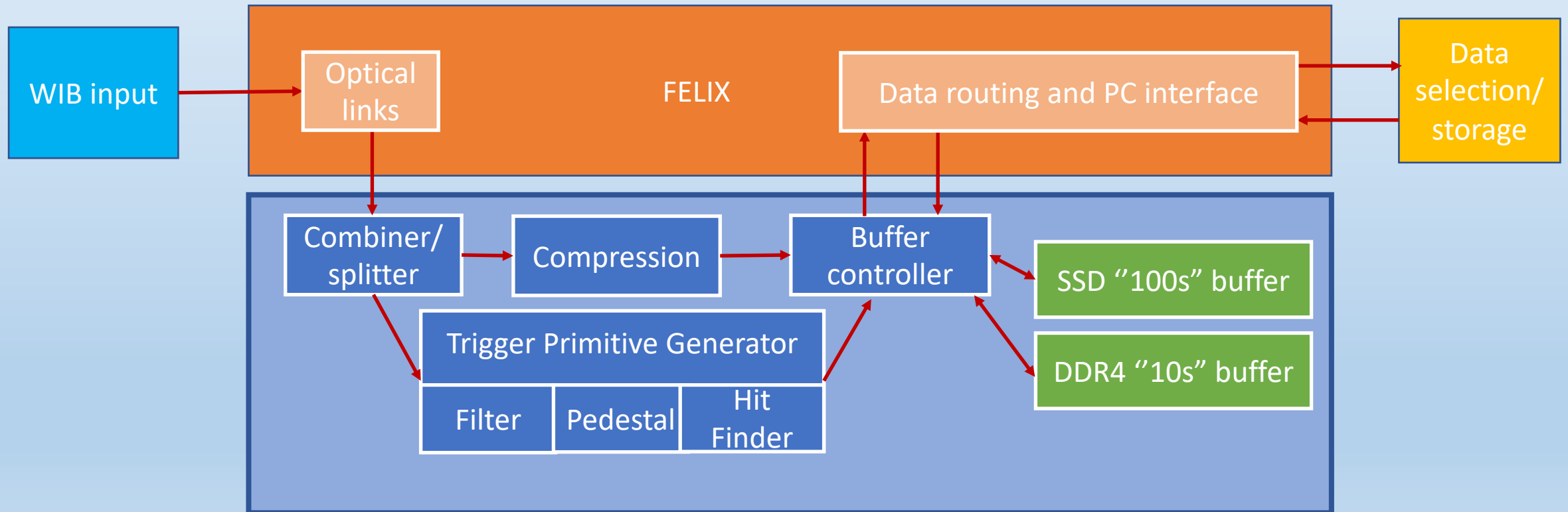
Filter/pedestal subtraction

- Filter is 32 tap FIR filter

- Firmware written and simulated

- Pedestal subtraction in development

- Resource use estimates indicate should fit in reasonable FPGA:
  - 32-tap FIR (x15): 5.52% LUTs, 2.12% FFs, 8.69% DSPs (percentages of KU115 resources)

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Hit finding

- Starts from filtered, pedestal subtracted samples

- Record peak height, length of hit, start of hit, integrated ADC

- Firmware synthesised and simulated

- Resource estimate suggests no problems
 - IO estimate below assumes 32 bit input (12 bit in final design)
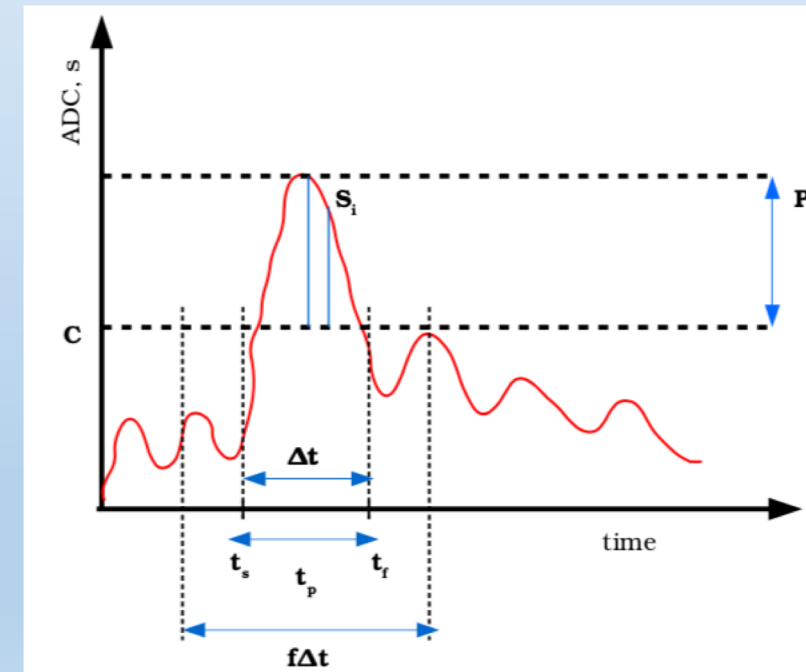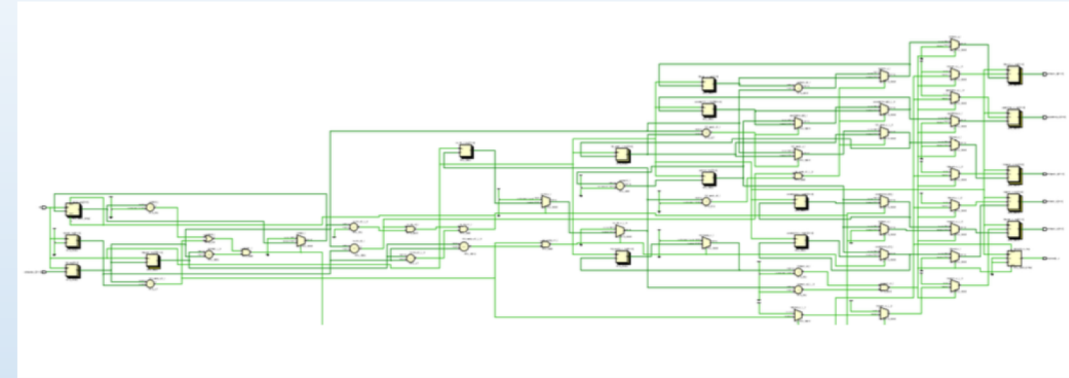
| Resource	Utilization	Available	Utilization %
LUT	514	242400	0.21
FF	420	484800	0.09
IO	194	520	37.31
BUFG	1	480	0.21

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Compression

- Fibonacci encoding via LUT implemented in firmware and simulated
  - Encode delta from previous sample so most entries are zero
  - Compression factor depends on noise profile of samples

- Resource estimate suggests ~1% of Block RAMs used per compression stream
  - 40 instances should fit on the FPGA without issues
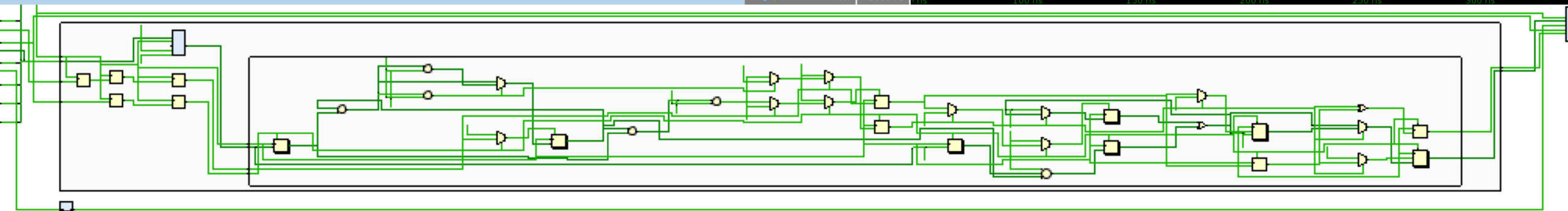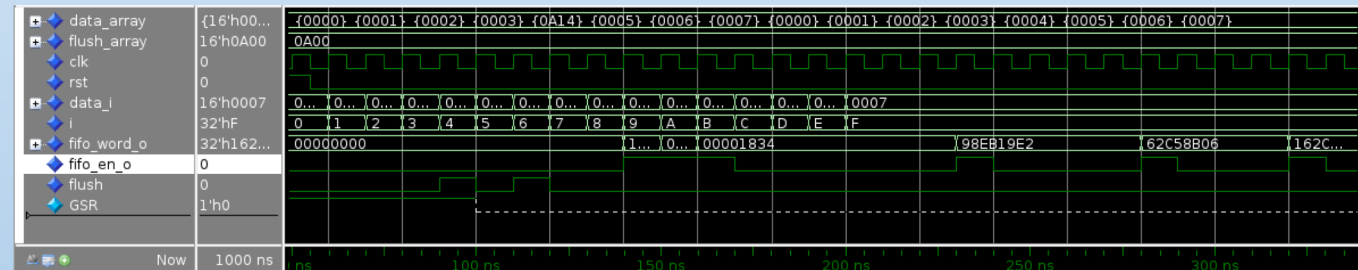
Validations so far

- Daughter board layout produced based on design initially made for previous version carrier board
  - Design revisions underway for prototype manufacture
- Firmware:
  - Compression block (Imperial), hit finder (Bristol), filtering and pedestal subtraction (RAL) are written and simulated, integration ongoing
  - Buffer controller (UCL) is being developed and simulated
  - Initial resource estimates indicate it will fit in a cost-effective FPGA

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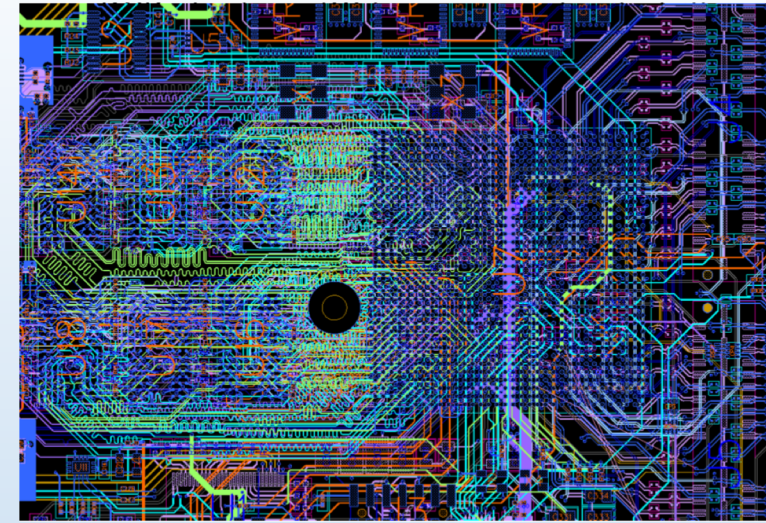
Hardware: Development up to the EDR and production

- Early 2019:
  - Prototype based on current DPM design using FMC+ daughter-card format
  - Detailed specification of FELIX-daughter card mechanical interface
- Later 2019:
  - Second prototype based on lessons learned from first, final mechanical spec (FELIX) and production optimisations
  - Build testing platform
  - Medium-sized production O(20) boards
- 2020:
  - Third prototype with robustness and testability improvements, manufacturer final optimisations
- 2021:
  - Pre-production and QC implementation
- 2022-2023:
  - Staged production over 18 month timescale is achievable given past experience

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Development plan up to the EDR – Integration/Firmware/Software

- Early 2019:
  - Firmware framework and algorithms slice tested on a development card
  - Ensure algorithms that fit FPGA meet physics requirements

- Later 2019:
  - Firmware interface for data IO to FELIX card designed, test platform to generate fake data built
  - Firmware ported to DUNE hardware daughter card
  - Prototype control software ready that allows O(20) boards to be used together

- 2020:
  - Production ready firmware, software and test platforms
  - Software work will focus on automation and integration with general DUNE backend electronics control framework

- Planning several slice tests as hardware/firmware is ready
  1) All co-processor firmware on a development board
  2) Development board interfaced with FELIX and dummy WIB interface
  3) Co-processor daughter card hardware on FELIX with dummy WIB interface
  4) FELIX plus co-processor card interfaced to real WIB at ProtoDUNE

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DUNE

Summary

- We have a well understood specification
- The first iteration of hardware development is taking place now based on an existing layout
- The key question is do hardware constraints allow physics requirements to be met and we have a plan to answer this using ProtoDUNE
  - 2019: Test of concept using full slice of system
  - 2020: Testing of full system to check reliability is sufficient

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