1 LRO front end status

1.1 Work done

FINE uCLinux link with the micro controller FINE µCLinux working when the mezzanine card is connected

Simulation the GHDL simulator is used instead of free ModelSIM VHDL because free and faster than the former

Electric tests all voltage and reference levels (2,5 V et 3,3 V . . .) validated

I/O Ancillary input/output signals (1,2 V et 0,4 V refs. comparators and level shifters) perform as expected

Pinout All interface signals between FMC board and the S4AM card have been validated (pinout, problem with 100Ω adaptation fixed)

Firmware the CATIROC IP controller (slow control, data capture, etc.) already validated using similar hardware for the Juno experience

Firmware data capture out of the ADC works property when using the provided template provided by IPNL

Firmware original code provided by IPNL adapted (using generic parameters) so that to comply with the needs of the front end (1 ADC / 16 channels); tested and simulated ok

Software Porting of the acquisition software Labview IPNL to a new C/Python software with an html server GUI is done (Jaime). It works in the same way as the provided one by IPNL. Data coming from the board is stored on disk. Decoding of the CATIROC configuration file into a binary array is executed via an ancillary program written in Matlab and developed for Juno (Cayetano)

1.2 Difficulties

Hardware

- We appreciate a (non symmetric) saturation at high amplitudes in the FMC card, which implies we are loosing in dynamic range (~25%), reducing available (negative) coding range to ~750 mV. This is not understood as for today. Improbable to be fixed

- PMT signals must all be attenuated and accommodated to the front end range of ~750 mV.
- When injecting a fake single electron signal (5 ns pulse) and changing its amplitude, we observe that for an input amplitude lower than 10 mV, no signal reaches the ADC input stage. After consultation with the engineer responsible for the design of the analog stage, we understand that the cut-off frequency of the low-pass filter has been designed to be -6 dB, instead of -3 dB. This is something which may be fixed by replacing some passive components on the pcb, attenuating this effect

JTAG When the mezzanine board is connected, the JTAG chain is broken. This means that no direct programming (immediate) of the FPGA in the mother board is available in this case during the development cycle. Unable to be fixed

Upgrade When the mezzanine is plugged, the new firmware to be tested can only be downloaded to the board by accessing the ftp in the ancillary FPGA running uCLinux OS, which is a slow process. Just an inconvenience.

Sync Synchronisation of several different boards need to go through the back plane. Problem is PORT 1 is booked for the clock distribution during the experiment in its most general working mode, and PORT 0 is only available for the FINE micro controller. Two options arise here

- Option 1: the slow control goes through the FINE and the FPGA Stratix IV
- Option 2: slow control and data readout use the 10 Gbps link. This is the option to privilege.

1.3 Currently working on

Firmware Once the simulation is fully understood, it becomes necessary to embed the code into the main project; currently a non well understood behaviour is under study

Firmware random behaviour is observed in the original code, non well understood but probably not unexpected, mail exchange with IPNL ongoing for support

1.4 Still to do

Hardware (multi-board mode)

- we yet have to verify the viability of current architecture (probable hardware modification in the S4AM mother board, different from the one used in the general DAQ)
- test the daisy chain addition of local trigger by board (combination and propagation of 12 channel signals to produce a global one)

Firmware

- include extra features requested by collaboration (triggering, coincidence, etc.)
- needed evolution to go to a multi board mode
- implementing a 10 Gbps mode
- integration of ASIC IP controller within the general NIOS processor architecture; develop a streaming based architecture

Software

- Adapt current software (8x8 channels) to working mode with one ADC x 16 channels
- Validation with new firmware (data decoding and displaying)
- Sending of slow control to CATIROC, reading it back and comparison to check correct setup
- Adding new slow control orders to take into account ancillary features (coincidence, triggering, etc.)
- Implement multi card mode

Acquisition

- Decoupling of data acquisition from the slow control
- Integration of the data acquisition side to the global data acquisition of the experiment

- Adapting software to a 10 Gbps mode from a 1 Gbps mode
- Synchronisation of data flows within the experiment with help of the WR board from IPNL

All

- Testing and debugging in single card, multi card stand alone and multi card coupled to the general system

2 Actions

- Cayetano Santos must concentrate all its project activities on this development, putting aside his other project engagements (up to a ~66% of his time since beginning of September, ~33% before). Jaime Dawson remains responsible of the software development
- APC envisions to increase the time Cayetano is available for this project by suppressing his other responseabilites no related to projects (electronics department), (up to a ~100 % of his time). Possible only if a candidate replaces him
- Following the same logic, Cayetano Santos is not allowed to attend next month, one week in2p3 training
- Follow up meeting is planned at APC on the 7 th of November