# Status of front end electronics

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APC - Astroparticule et Cosmologie

# Difficulties

## Firmware upgrade

When mezzanine present, JTAG chain is lost ... PROBLEM

When mezzanine present, FINE uCLinux is lost ... CORRECTED

To upgrade firmware whith mezzanine it is necessary to flash the eprom ... SLOW

## Simulation

ModelSIM VHDL simulator not available (free version very slow) ...

... use of alternative VHDL simulator, GHDL: gcc technology, much faster ... OK

## P0 / P1

Sync of several boards goes throught back plane

P1 taken by clock distribution

P0 only available to the FINe

Opt. 1: slow control through FINe and Stratix IV, how ? data readout using 10 Gbe

Opt. 2: slow control and data readout using 10 Gbe

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# Firmware/hardware: already done

## Electrical test OK

All reference voltage levels (2.5 V. Vadj, 3.3 V., etc.) ... OK

## IO spare signals OK

Reference 1.2 V. and - 0.4 V. levels ... OK

Comparators and level shifters ... OK

## All S4AM/FMC interface signals OK

Full pinout validated - No surprises there ... OK

Issue with 100 Ohms adaptation seems solved - measured, and confirmed by Bittware ... OK

## Firmware: CatiROC controller IP

Validated by experience with few different hardware (slow control, data capture, etc.) ... OK

Online under GPL3 at http://bit.ly/2JPJFOa

## Firmware: ADC

IPNL example template project running - all setup checked ... OK

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# Firmware: still to do

## ADC

Under adaptation from 8x8 ADCs to 1x16 ADC (same component) - Use of generics

Currently under simulation - Next to run in hardware

16 ch. / 64 ch. mode -> 16 ch. only mode, in parallel with software

## CatiROC

Adapt existing IP as a peripheral to NIOS II architecture

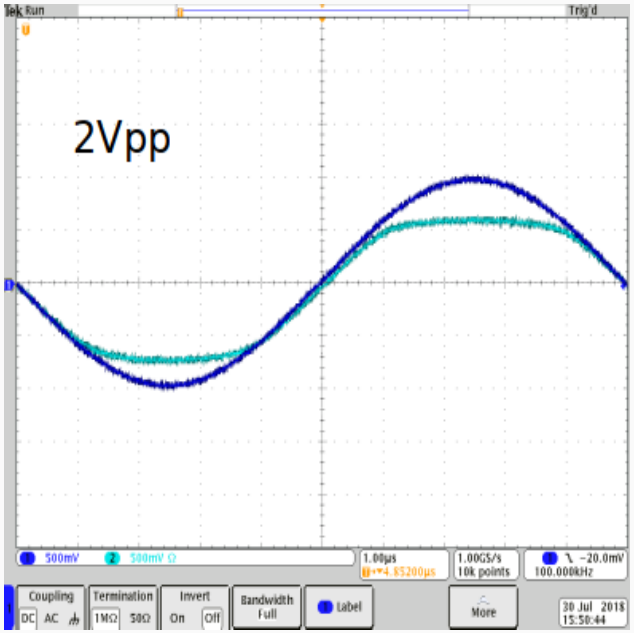
## Basic functionality

All functionality requested by CIEMAT collaborators (triggering, coincidence, etc.)

## 10 Gbps

Make it work at 1 Gps -> Make it work at 10 Gbps ... 10 Gbps Infrastructure ?

# Hardware: still to do. Debug and fine tune FMC

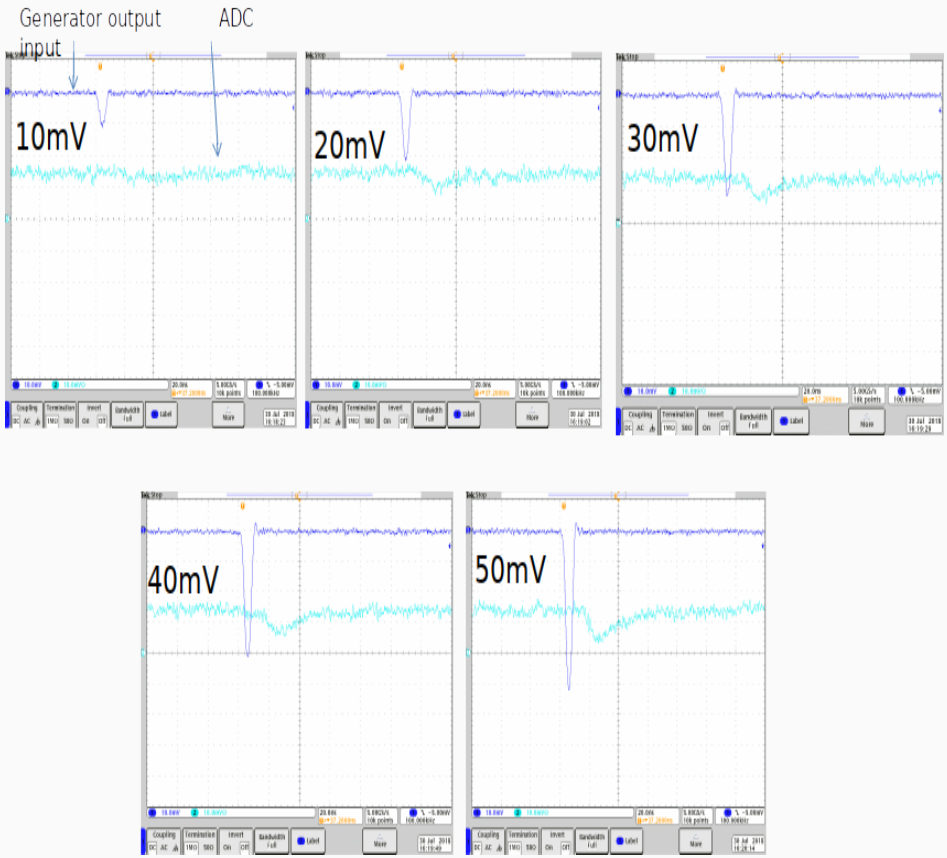



Saturation at high amplitude.

Need to tune hardware with diff. probe: fix low pass filter bandwidth, understand saturation, etc.

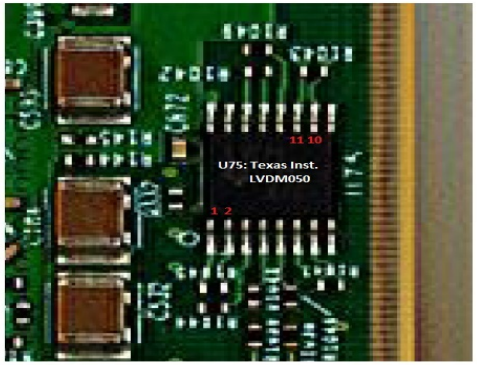
*All plots from A. Verdugo (CIEMAT)*

## SPE like (5ns) pulse response




Wrong LPF cutoff frequency.

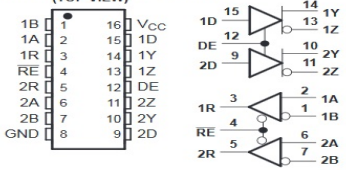
# Hardware: still to do. Multi card mode




**Carte S4M d'origine**
**U75 (convertisseur LVDS TTL)**

pin1 = TCLK_A- (pin 75 connecteur backplane µTCA)
pin2 = TCLK_A+ (pin 74 connecteur backplane µTCA)
pin10 = TCLK_D+ (pin 139 connecteur backplane µTCA)
pin11 = TCLK_D- (pin 138 connecteur backplane µTCA)

**SN65LVDM050D** (Marked as **LVDM050**)
**SN65LVDM050PW** (Marked as **LVDM050**)
(TOP VIEW)




ALTERA

Pin Information for the Stratix® IV GX EP4SGX230 Device
Version 1.4

| Bank Number | VREF | Pin Name/Function | Optional Function(s) | Configuration Function | Dedicated Tx/Rx Channel | Emulated LVDS Output Channel | F1517 | Dynamic OCT Support | DQS for X4 for F1517 | DQS for X8/X9 for F1517 | DQS for X16/ X18 for F1517 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 7C | VREFB7CN0 | IO | CLK13p | | | DIFFOUT_T47p | B20 | No | | | |
| 7C | VREFB7CN0 | IO | CLK12n | | DIFFIO_RX_T24n | DIFFOUT_T48n | A20 | No | | | |
| 7C | VREFB7CN0 | IO | CLK12p | | DIFFIO_RX_T24p | DIFFOUT_T48p | A21 | No | | | |
| 8C | VREFB8CN0 | IO | CLK14p | | DIFFIO_RX_T25p | DIFFOUT_T49p | B22 | No | | | |
| 8C | VREFB8CN0 | IO | CLK14n | | DIFFIO_RX_T25n | DIFFOUT_T49n | A22 | No | | | |
| 8C | VREFB8CN0 | IO data White Rabbit | CLK15p | | | DIFFOUT_T50p | B23 | No | | | |
| 8C | VREFB8CN0 | IO | CLK15n Tclk-C = 125Mhz White Rabbit | | | DIFFOUT_T50n | A23 | No | | | |

**carte S4AM de bittware modifiée:**
J'ai levée les pattes 1, 2, 10, 11
J'ai reliée TclkD- a la patte1, TclkD+ a la patte 2 *(liaison au borne de la 100 ohm de terminaison)*
J'ai laissée en l'air les pattes 10 et 11

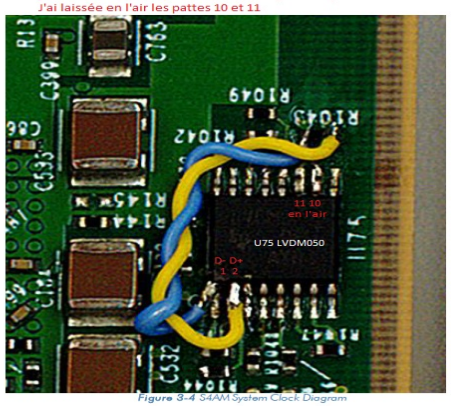
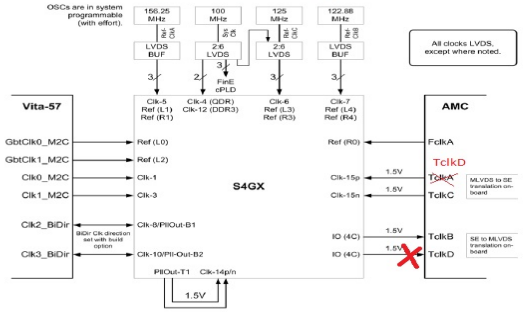



*Figure 3-4 S4AM System Clock Diagram*




3.8.1 Clock Implementation

The S4AM has four independent clock generation circuits that are all based on a Pletronics component that can either be populated by an oscillator (2.5V LV77D series) or a programmable clock generator.



Check viability of current architecture (S4AM hardware modification, etc.)

Local trigger sum up

Firmware upgrade to multi card.
Validate hardware
(trigger propagation, etc.)

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# Software: already done

## LabView Porting

Conversion from LV to C/Python + Web GUI ... OK

Compliant with IPNL template ... OK

Decoding data on disk and displaying it ... OK

Decoding of CatiROC config file into binary data (using matlab code) ... OK

# Software: still to do

## Next

Adapting to 1 ADC / 16 channels data format

Validating with new firmware / decoding and displaying

Readout of CatiROC binary data and compare

Slow control for ancillary functionality

Multi card mode

## Acq

Decouple acq and slow control

Merge acq into main DAQ

1 Gbps / 10 Gbps modes

# Conclusion

A lot still to do

Firmware still under development

DAQ support by IPNL / Slow Control at APC-LAPP

**CatiROC** Proved, tested and characterized on different projets

**uTCA** Standard rather time demanding: too many tricks to know ...

Existing example code running + proved firmware IP ...

... but reduced manpower

33 % one engineer time dedicated to this project ...

... 66 % one engineer time dedicated to this project since september

+ Jaime Dawson taking care of software since September