Status of Data from FEMBs 302 and 110

Tom Junk ProtoDUNE Sim/Reco Meeting October 24, 2018



FEMB 302

Fom Matt Worcester, Aug. 31:

The cause of the issue is that FEMB has lost both of the clock lines, likely due to a partially broken connector, as we saw with some FEMB in the cold box tests.

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It will need to use a special firmware that ignores the system clocks and uses the onboard oscillators as the clocks. Therefore it will always be asynchronous with the rest of the system. We believe there will be an offset within 500 nsec (1 tick) to the other channels that may drift over time. This data will also not have any timestamps from the FEMB. Finally, it won't receive any timing commands, so we can't align it with the external pulser (the internal pulser will still work for electronics calibration). Because of this, the default is for the WIB to mark the data bad, but still pass it along to the DAQ.

FEMB 302

• APA 3 is upstream, rack side. Right where the beam comes in



crate=3 (counting from 1)
slot=3 (counting from 0)
fiber=2 (counting from 1)



Fermilab DUNE

Beam

Example of Disease



A clue: different channels affected differently – WIB frames unable to do this, so must be software. Also, untrimmed data do not show X-shaped features.

♣ Fermilab DU(NE)

Investigating..

- The number of samples in the FEMB 302 data is 5996 and not 6000.
- The timestamps and the convert counts returned along with the WIB frames do not count sequentially. Some numbers are skipped (0.07%).
- Consistent with a clock running slow on the FEMB.
- The unpacking library, proto-dune-dam-lib, which is packaged up as the UPS product dunepdsprce, has a weakness that caused cumulative offsets in the unpacked data when this happened.
- JJ Russell has investigated and found the issue, and fixed it.
- Some little residual issues left (negative ADC values at the ends of waveforms, only when code is compiled with optimization !)

Pre and Post Fix: FEMB 302



Much better! Still some rubbish on the end. Not important for physics, but don't want a segfault.



Additional Features

- The new proto-dune-dam-lib gives timestamps at the beginning and the end of the waveform
- It also allows checking of the fragment for integrity before runing into our crashes and hangs (it's been a while...)
- We had put in stop-gap checks on the fragment size before calling constructors in proto-dune-dam-lib which had crashed or hung.
- Checking the size as a stopgap is not the greatest as a corrupt uncompressed fragment is bigger than a good compressed fragment. And events now contain a mixture – FEMB 302 is uncompressed.



Residual Issues

- Old band-aid filled in the missing ticks to make 6000.
- Now we have 5996 ticks and beginning and ending timestamps.
- No data may actually be "missing", just sampled slower.
- "stretch" the waveform? Shift the waveform? Put in "leap"-ticks?
- Problem is much smaller now 4 ticks instead of up to 100.
- Weird behavior seen negative ADC values appended to the waveforms of FEMB 302 channels. But only when proto-dune-dam lib is compiled with optimize flags, not when not optimized.
- Waiting on debug before release. Don't want a segfault in production.
- JJ pushed a fix on Tuesday evening will test soon.



FEMB 110

This was spotted in our Press Release track.

You have to look really close though.

This is another event in which tracks go through the problem area.

FEMB 110, ASIC 3 channels are off by ~20 ticks.

It's been in every event I've looked at. I haven't been systematic about checking how consistent the offset is however.

I was going to wait for JJ's update to see if it helped this one. It didn't. Source is not understood.



Since it follows the ASIC hardware boundary, I suspect it is in the hardware and not software.



Sliding the FEMB 110 waveforms

- Another band-aid: shift the waveforms by n=18 ticks (configurable by fcl, but only positive numbers so far allowed). Pad last 18 ticks with last value.
- physics.producers.tpcrawdecoder.RCEFIX110NTICKS: 18



With band-aid (18 ticks)



Sometimes More Ticks are Needed



sifted by 18 ticks



Shifted by 25 ticks



A Possible Mechanism

- LBNE DocDB 9028 (Hucheng Chen et al) explains that the FIFO on the ADC ASIC is 32 samples deep.
- There are global reset and a FIFO reset signals presumably shared by all FIFOs on all FEMBs.
- Maybe there's one that doesn't get the message.
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