

# **PD front-end electronics**

**Josh Spitz, University of Michigan  
30% DUNE Design Review, 11/12/2018**

**with: Dave Warner, Jon Ameel, Gustavo Cancelo, Rory Fitzpatrick, Chris Barnes, Matt Toups,  
Sten Hansen, Dante Totani, Joel Mousseau, Alex Himmel, and others**

# Introduction

- Commercial ADCs used in ultrasonic transducers (Texas Instruments) are being used for digitization in the SiPM-based mu2e cosmic ray veto scintillator.
  - Low noise, high gain, high dynamic range.
- 80 Megasamples per second, 12 bit
- Low cost (\$50/channel) and capable of handling the envisioned DUNE MPPC (SiPM) warm-side PD signals.

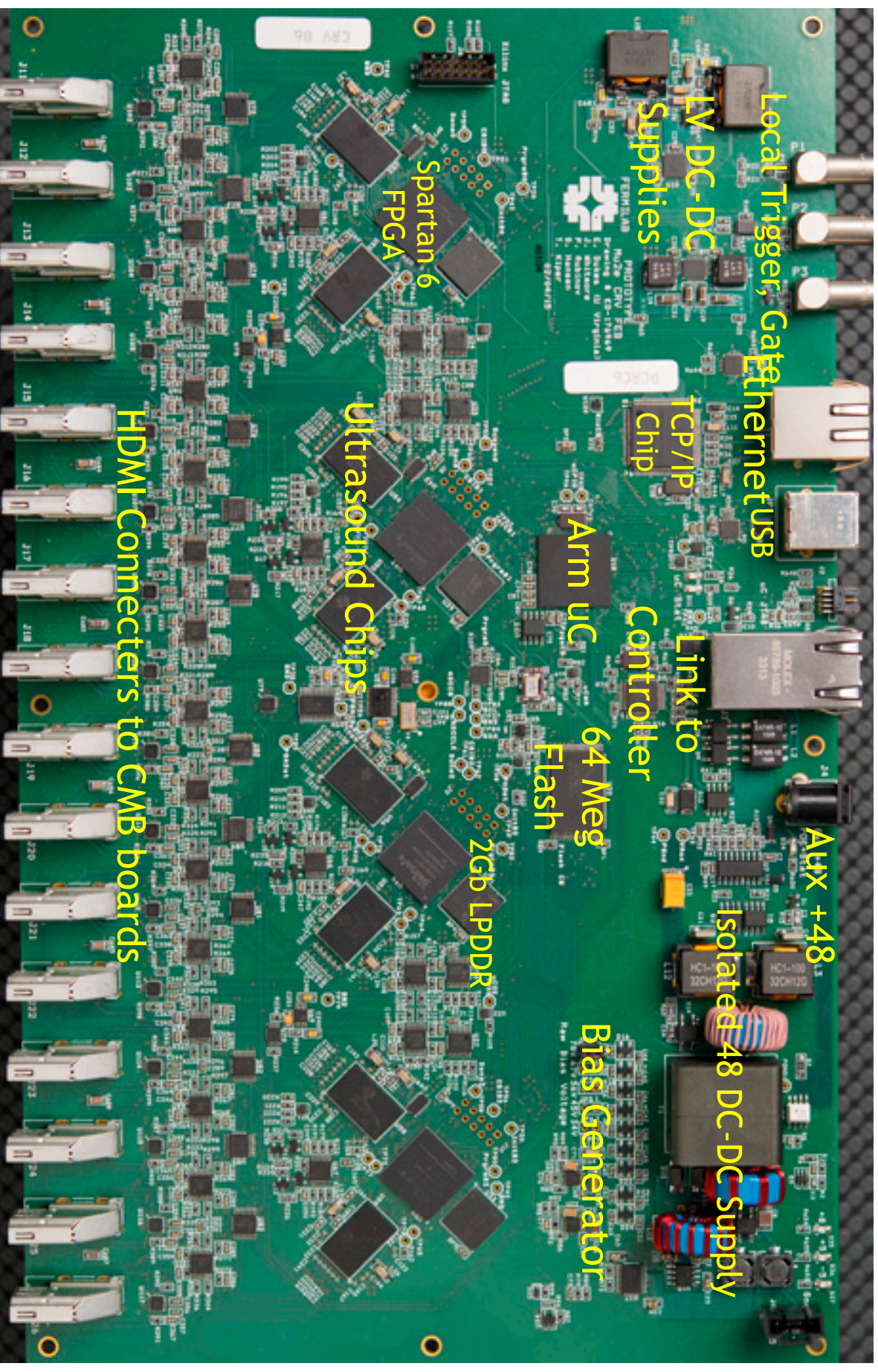


# Warm-side electronics elements

- Warm-side FEB
  - 64 channels of 80 MS/s, 12 bit ADCs
  - Bias generator (for SiPMs; 80 V max)
  - Current measurement (100pA resolution) for IV curves of SiPMs
  - Power-over-ethernet power (600 mA) for entire board's power. One Cat6-cable for data and power.
  - 1 GB DRAM data buffer, divided in 4 places (256 MB each) on the board, corresponding to the 4 FPGAs
  - Parallel flash ROM for fast FPGA re-load (50 ms)
  - Low cost, high bandwidth HDMI used to connect to cold-side
- Readout controller
  - 24 FEB link ports. Supplies timing, trigger, and power to FEBs
  - Can produce (e.g. TPC) triggers and also accept external (e.g. accelerator) triggers

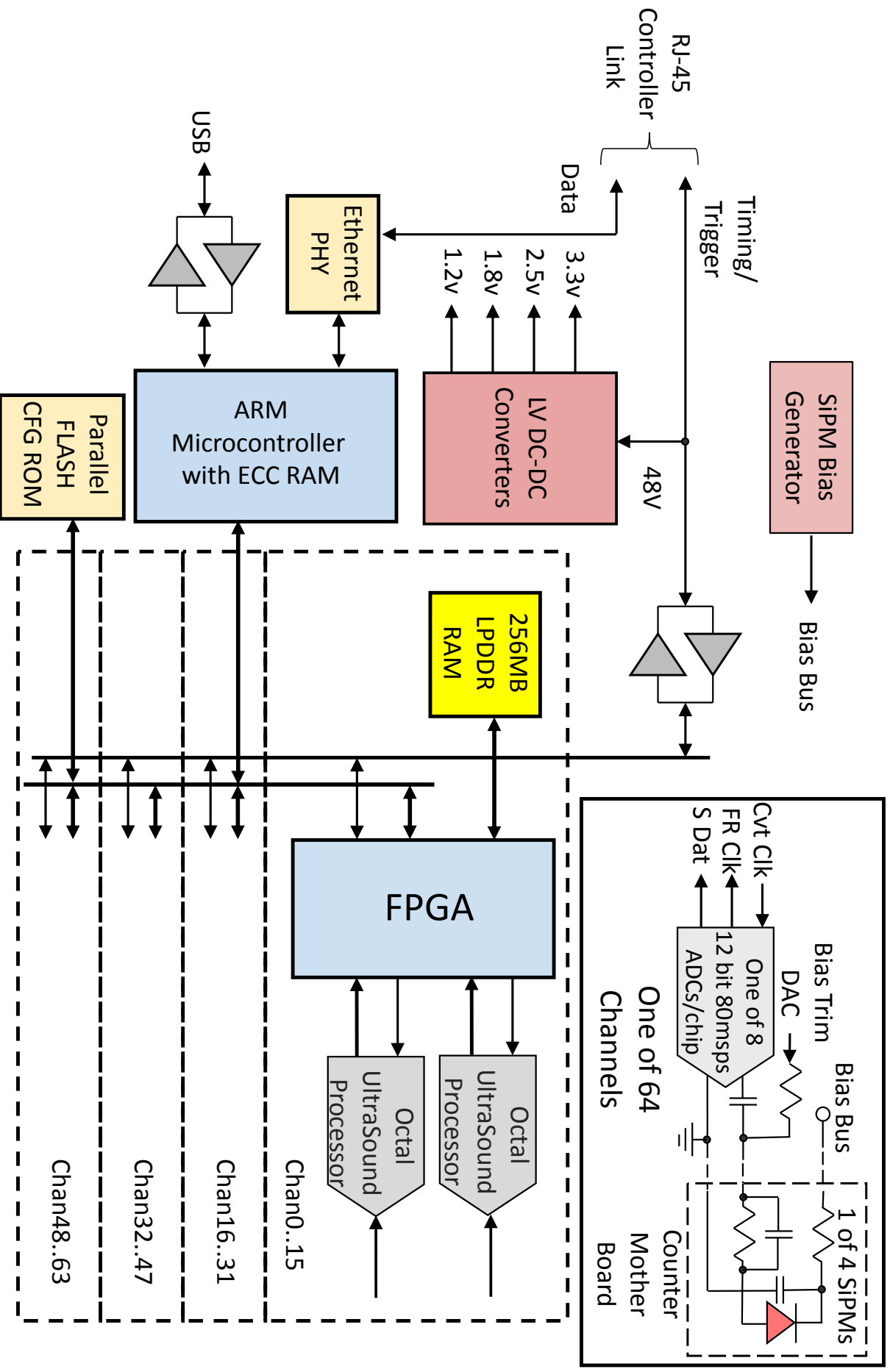
# Front-end board

(64 channels, 80 MS/s, 12 bit)



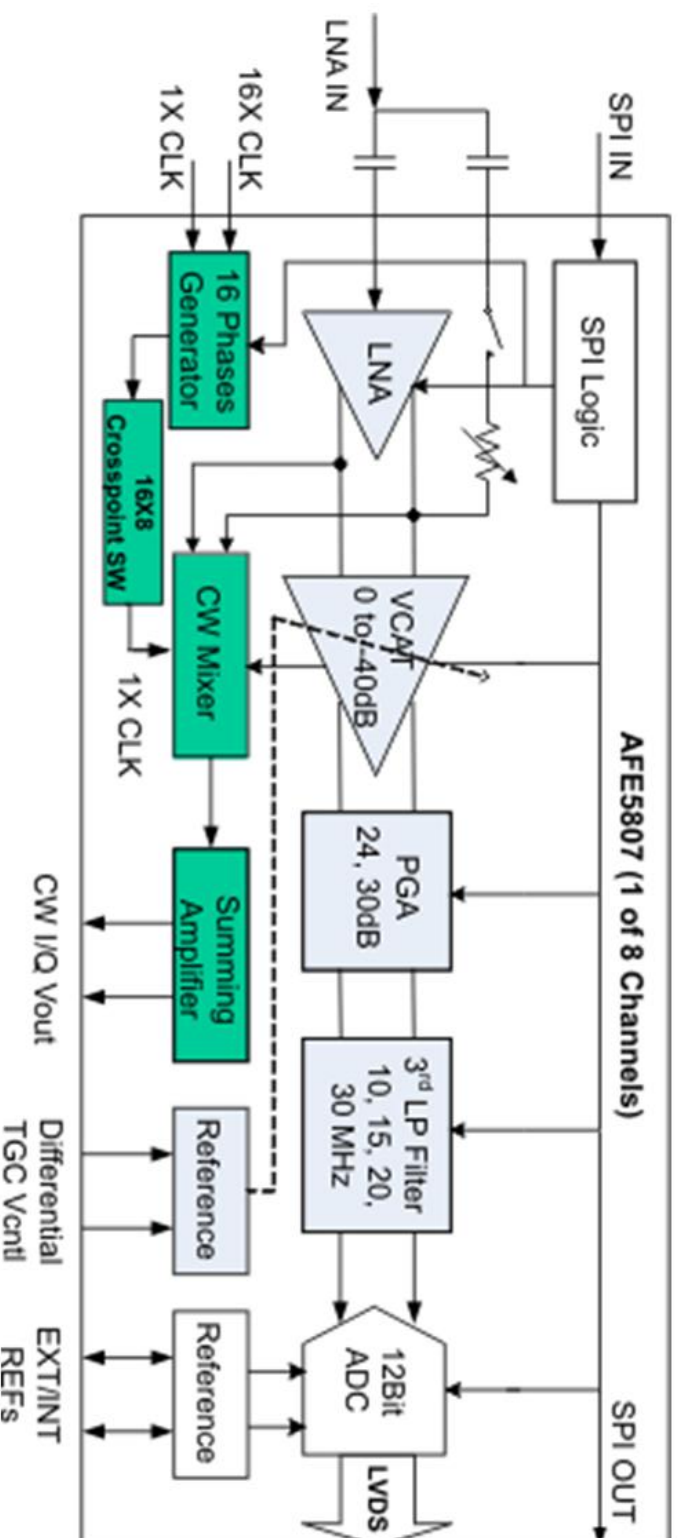
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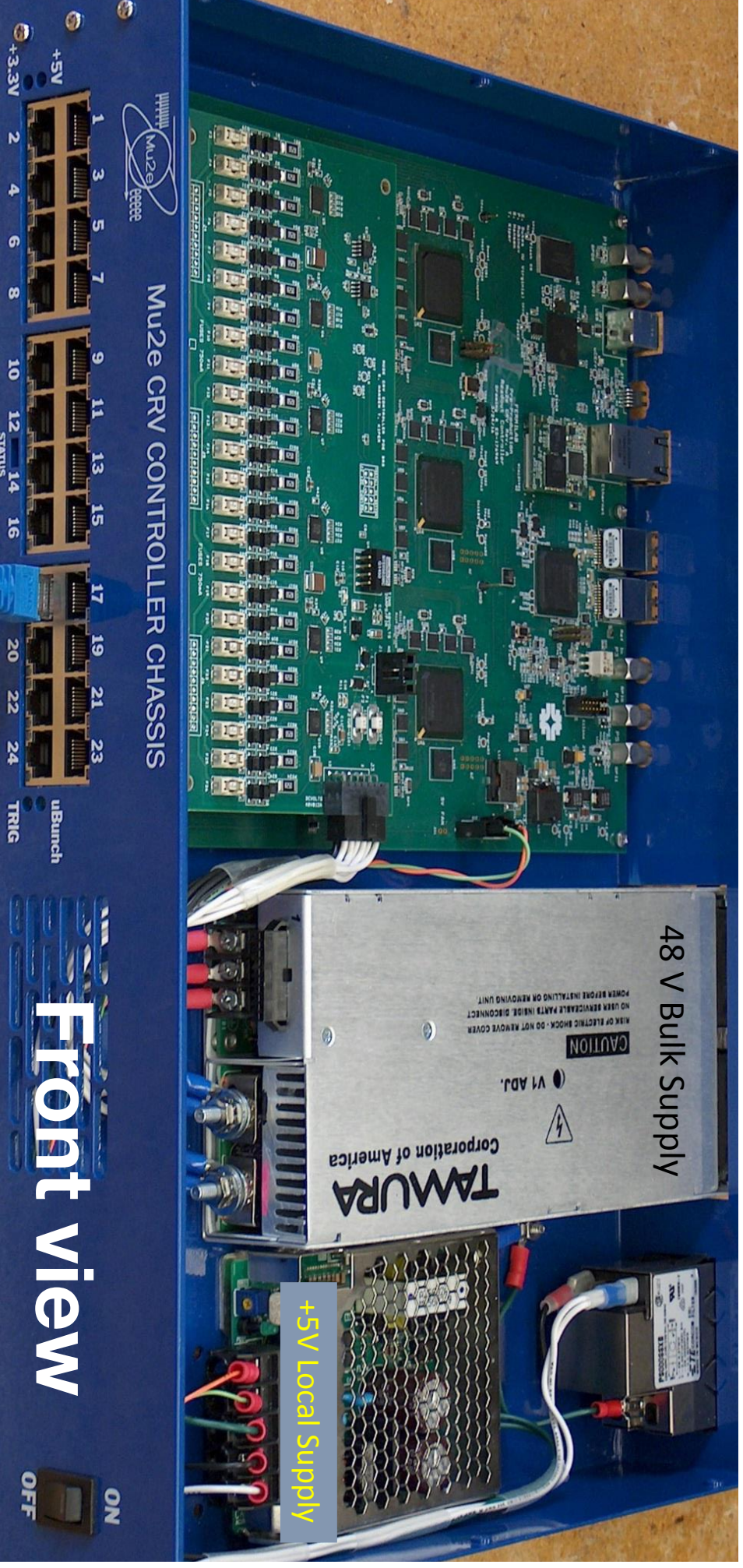
# Commercial Ultrasound ADC



**Eight channels of: low noise preamp, variable gain amp, programmable gain amp, programmable low pass filter, 80 MS/s, 12 bit ADC, \$8 per channel, 120 mW per channel. Can adjust gain so that 1pe=10 ADC**



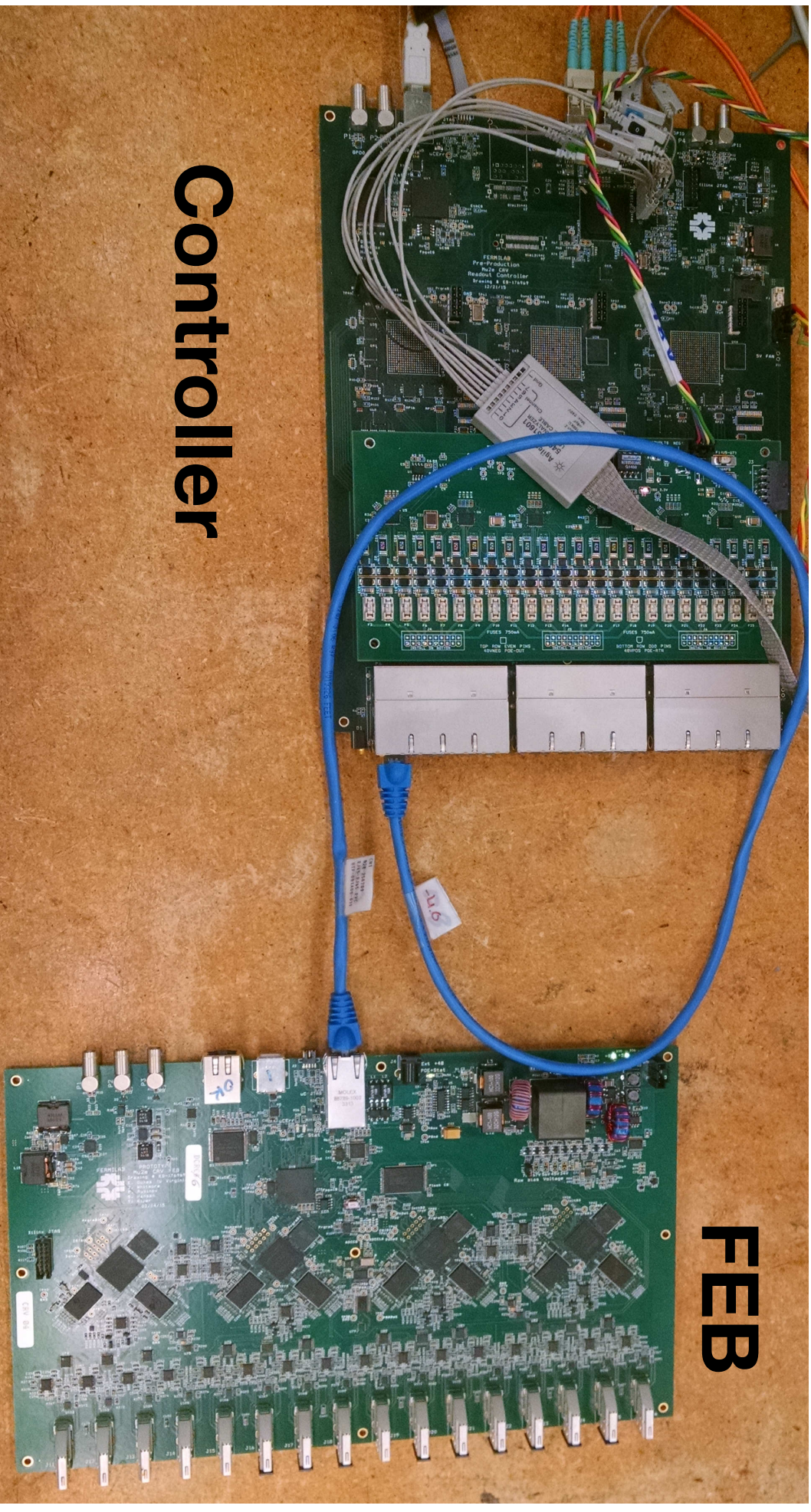
# Back view



# Front view



# Controller w/ one FEB





# Controller w/ two FEBS



**Controller**

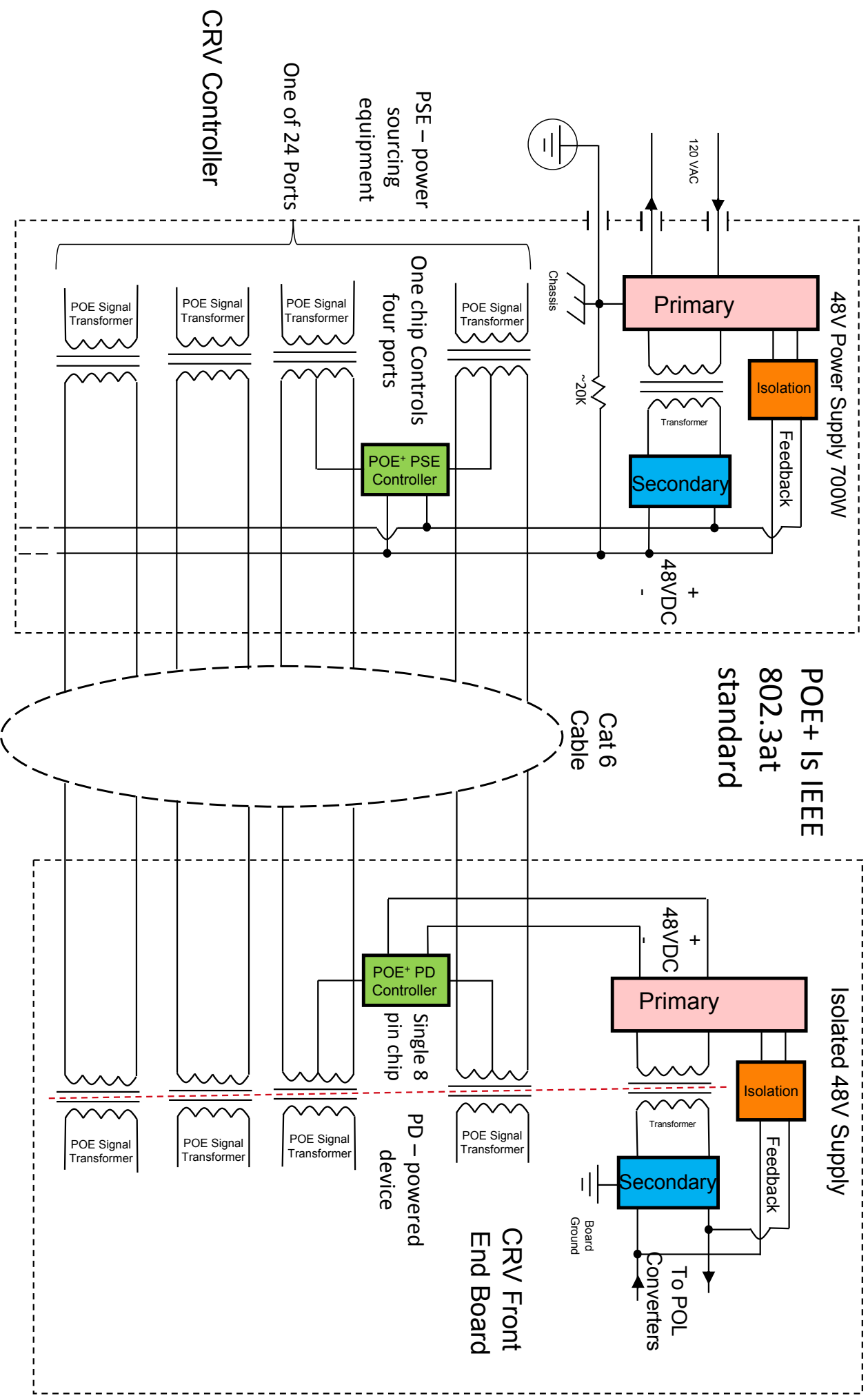
**FEBS**

**FEBS**





# Power and Data Link Arrangement



# DAQ concept

- 12 FEBS referenced to a single chassis, each FEB communicates over copper to a master controller (DC isolated on both sides).
- Each controller can take digital inputs from 24 FEBS (64 channels each-> 1536 channels, or in the case of 40 channels each->960 channels).
- Controller provides power (48 V supply) to FEBS.
- Controller connects to a DAQ PC either over fiber optic or ethernet (copper).
- Pulses (timestamp and pulse height) are sent from FEBS to controller. Controller issues global trigger to FEBS.

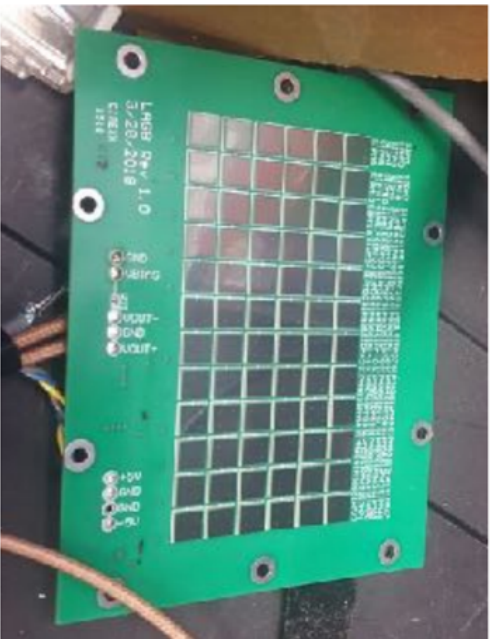
**Can the FEEB work with the  
active summing board?**

**(yes)**

# Bench-top tests

SIPM Power Supply

OpAmp Power Supply



**Gustavo's board**

(in cold)

**Bias for op-amp and MPPCs provided by external DC power supply**



**balun from Michigan**

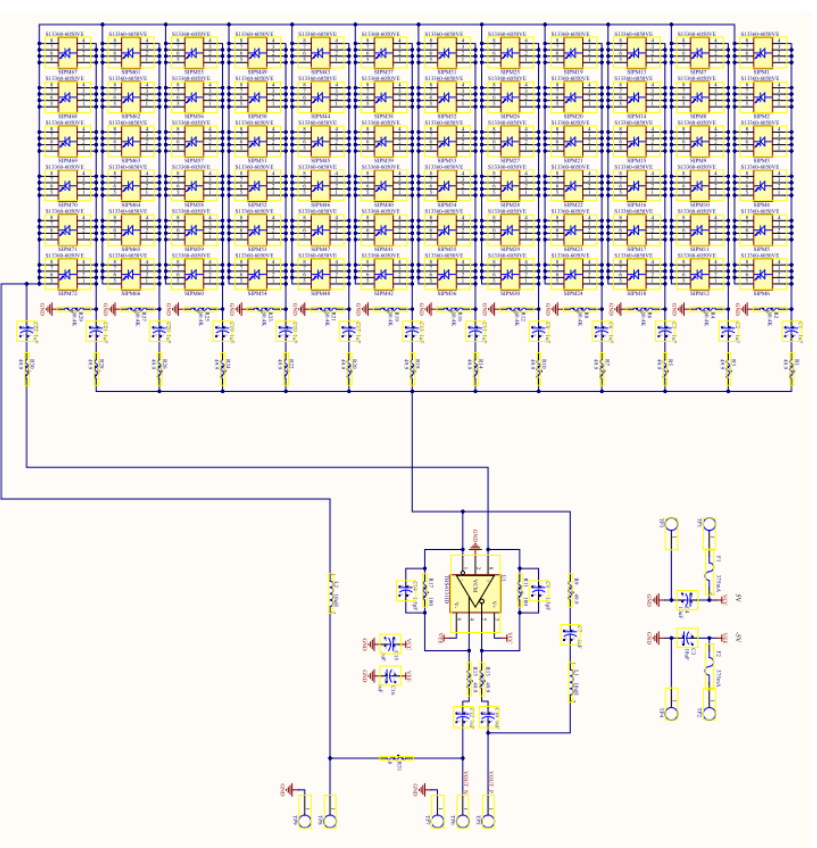
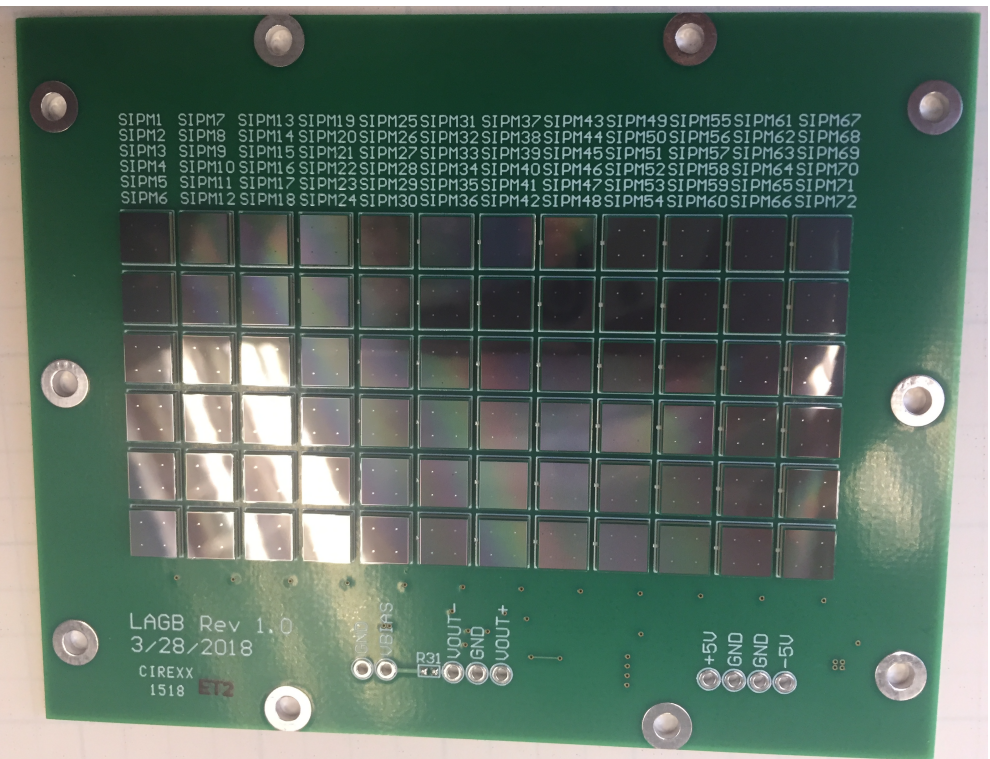


**FEB**

Laptop for DAQ

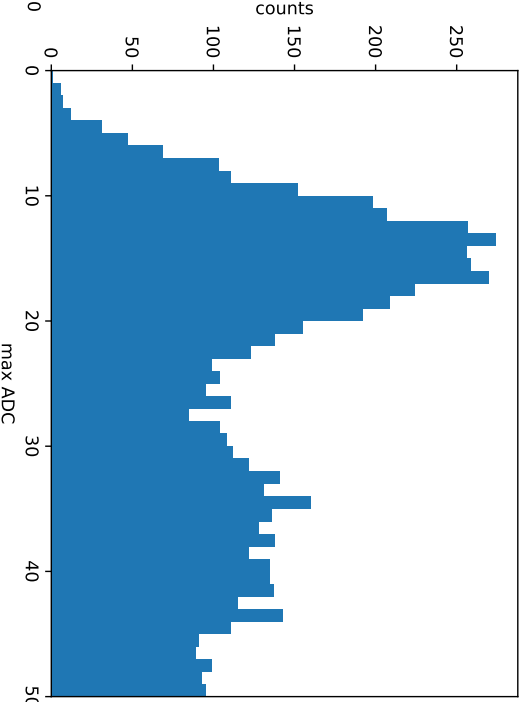
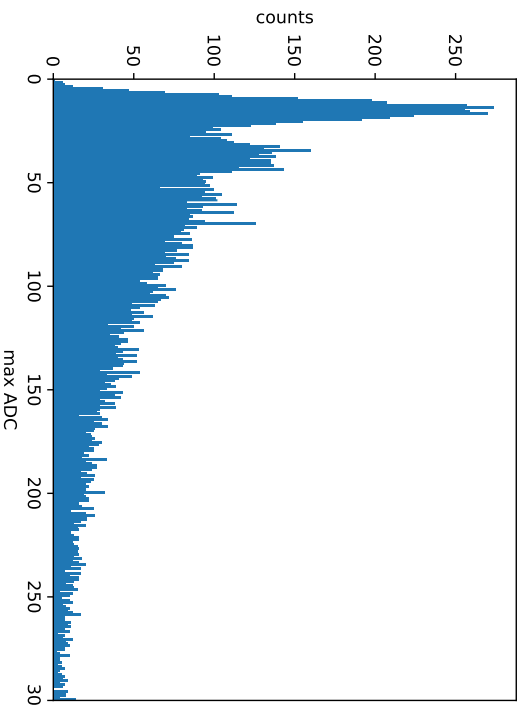
**Op-amp output is differentiated, while the FEB has a single-ended op-amp. Need to “undifferentiate” signal with balun**

# 72 MPPC array test

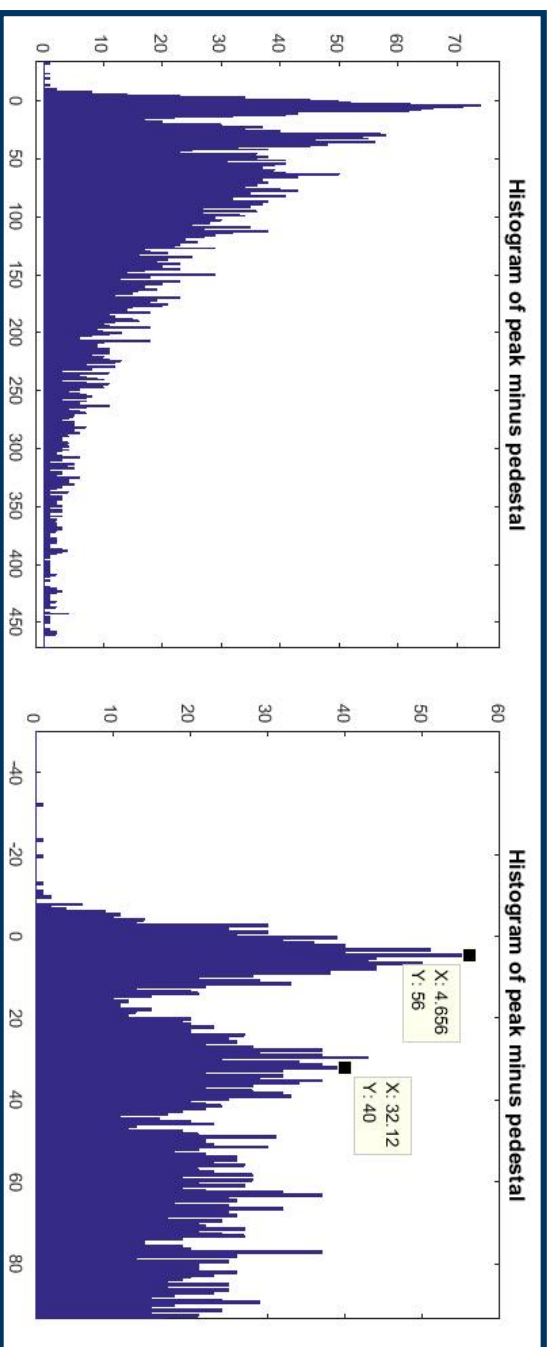


**each of 12 rows has 6 of 6mm<sup>2</sup> MPPCs in parallel**  
**total capacitance of 7.8 nF per row**

# Successfully demonstrated single photon resolution!



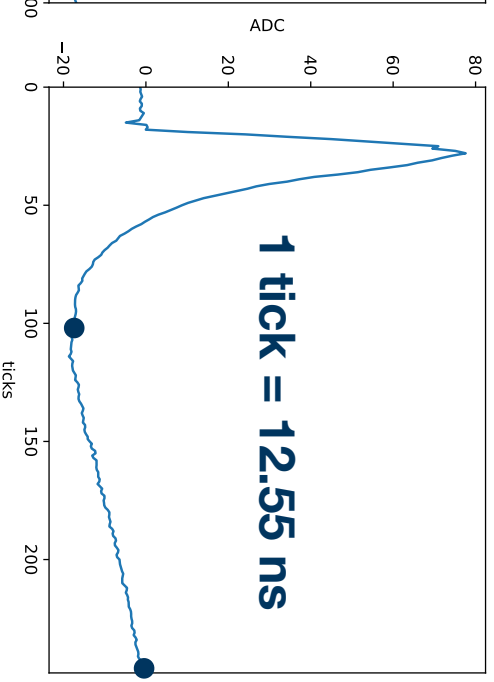
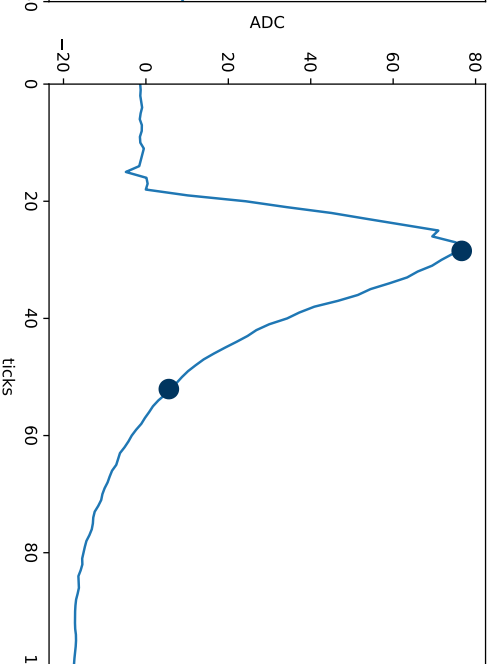
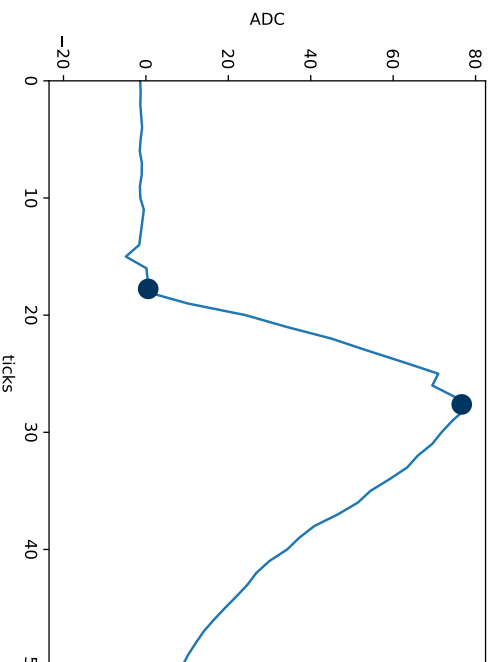
**Mu2e FEB**  
**S/N = 4**



**SSP, S/N = 5**  
courtesy of  
**Gustavo and Dante**

**Comparable resolution measured as peak-to-width ratio**

# Average waveforms



- Rise time: 125 ns
- Fall time: 350 ns
- Recovery time:  $O(2\mu s)$  — what's shown on the right is as wide a window as the FEB allows

# Zero-suppression

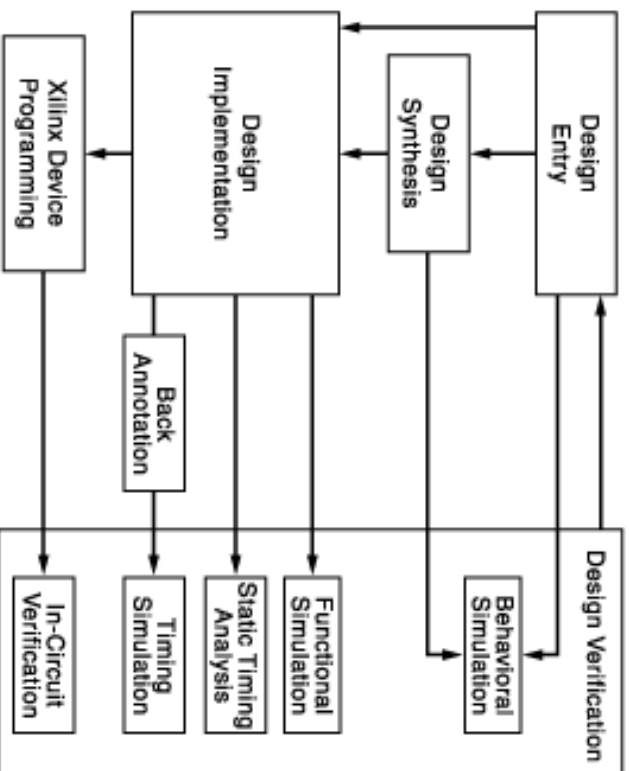
- Zero suppression: Time tick is saved to the board's RAM if the tick is above a pre-set pedestal value.
- mu2e and SBND will use the FEB+controller to take zero-suppressed data.
  - FEB+controller zero suppression interface work is ongoing.
- Work towards fully understanding the zero-suppression (suppression factor) requirements is ongoing.
  - Dependent on readout window and overall trigger rate.



# Bandwidth and rates

- Bottleneck is 10MB/s FEB to controller rate (per FEB).
  - Currently considering 40 readout channels per board.
- 80 MHz, 12 bit ADC; 5.5 us waveforms=5.3 kbit/waveform
  - Consistent with longest waveforms (including late-light) expected
- DC rate: 250 Hz/channel; 53 Mbps/APA (1 APA=40 channels)
  - 6.6 MB/s FEB to controller DC rate (compare to 10 MB/s FEB-controller bottleneck)
  - Can develop multi-channel coincidence+threshold requirement at the FEB firmware level to mitigate (study ongoing).
- DAQ interface spec: 8Gbps per connection. DAQ takes 24 FEB signals (10 Mbps each)=240 Mbps. Ok!
  - Maximum instantaneous rate: 6000 channels fire at once
    - 32 Mbits (4 MB) at once.
  - The controller can handle all 24 boards firing at once. Write speed for 24 boards is 150 MB/s and could likely be increased to 400 MB/s with some work (according to Sten Hansen).

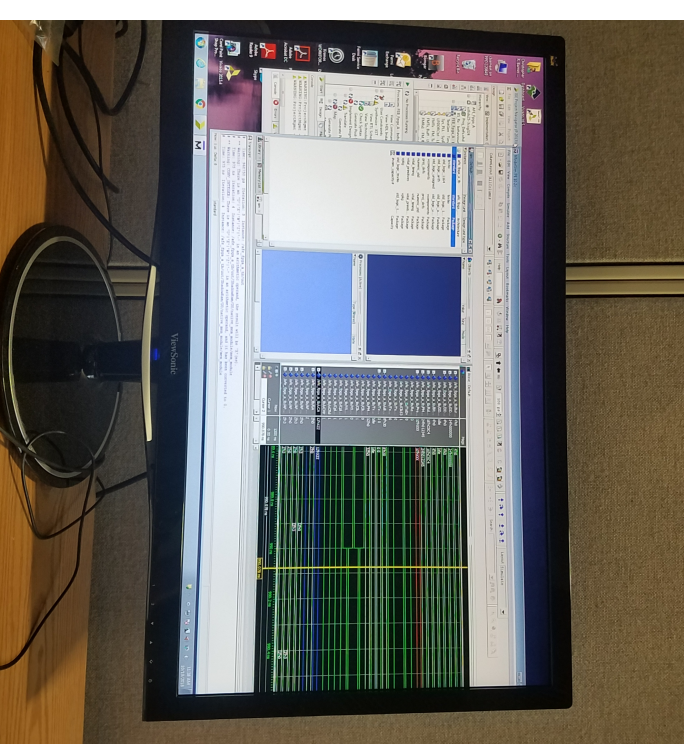
# Firmware development



Source: "FPGA Design Flow Overview", Xilinx Website.

**Xilinx ISE:** This is a design environment used to design firmware written in VHDL for use in Field-Programmable Gate Arrays (FPGAs). The ISE ("Integrated Synthesis Environment") version, 14.7, is the last available version that works with a Spartan 6 FPGA.

**ModelSim:** This is a simulation environment for VHDL and other hardware description languages, distributed by Mentor Graphics. The version, 10.2c, is the version that works with the ModelSim license at Fermilab.



# Structure of the Firmware

The firmware is written in VHDL, called “Very High Speed Integrated Circuit Hardware Description Language” .

The firmware is separated into three components:

1. **Main Firmware File (extension “vhd”):** contains the logic for piping data into the FEB and out to the controller.
2. **Test Bench (extension “tb”):** contains the timing structure for each of the signals that the logic in #1 handles.
3. **Constraints File (extension “ucf”):** contains the associations between the ports on the FEB and the signals within #1.
4. **Project Definitions File (extension “vhd”):** defines iterators and constants that are used within #1.

The remainder of the firmware consists of the functional models of components that are called within #1.

**Initially written for mu2e->adapting it for DUNE  
(ongoing work)**

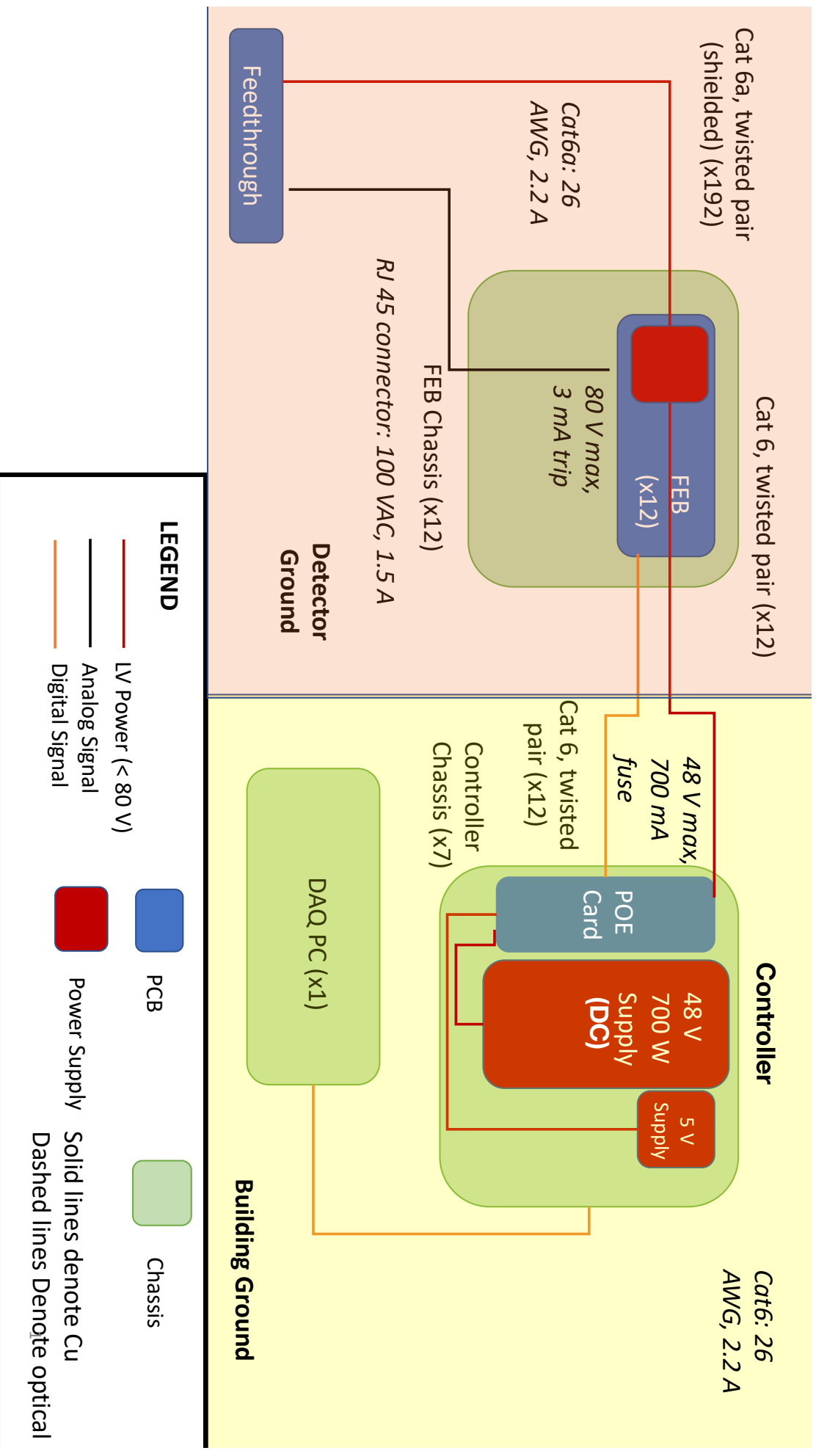
# Power considerations

- In addition to digitizing the SiPM signals, the FEB is nominally designed to bias the SiPMS.
- Can the power be used for the active summing board as well?
  - No, it does not provide a stable enough voltage. The on-board Cockroft-Walton should not be used to bias the differential amplifier of the summing board.
- How to handle this?
  - Redesign on-FEB power supply?
  - Include another cable/wire in design?
- We are working to address this.

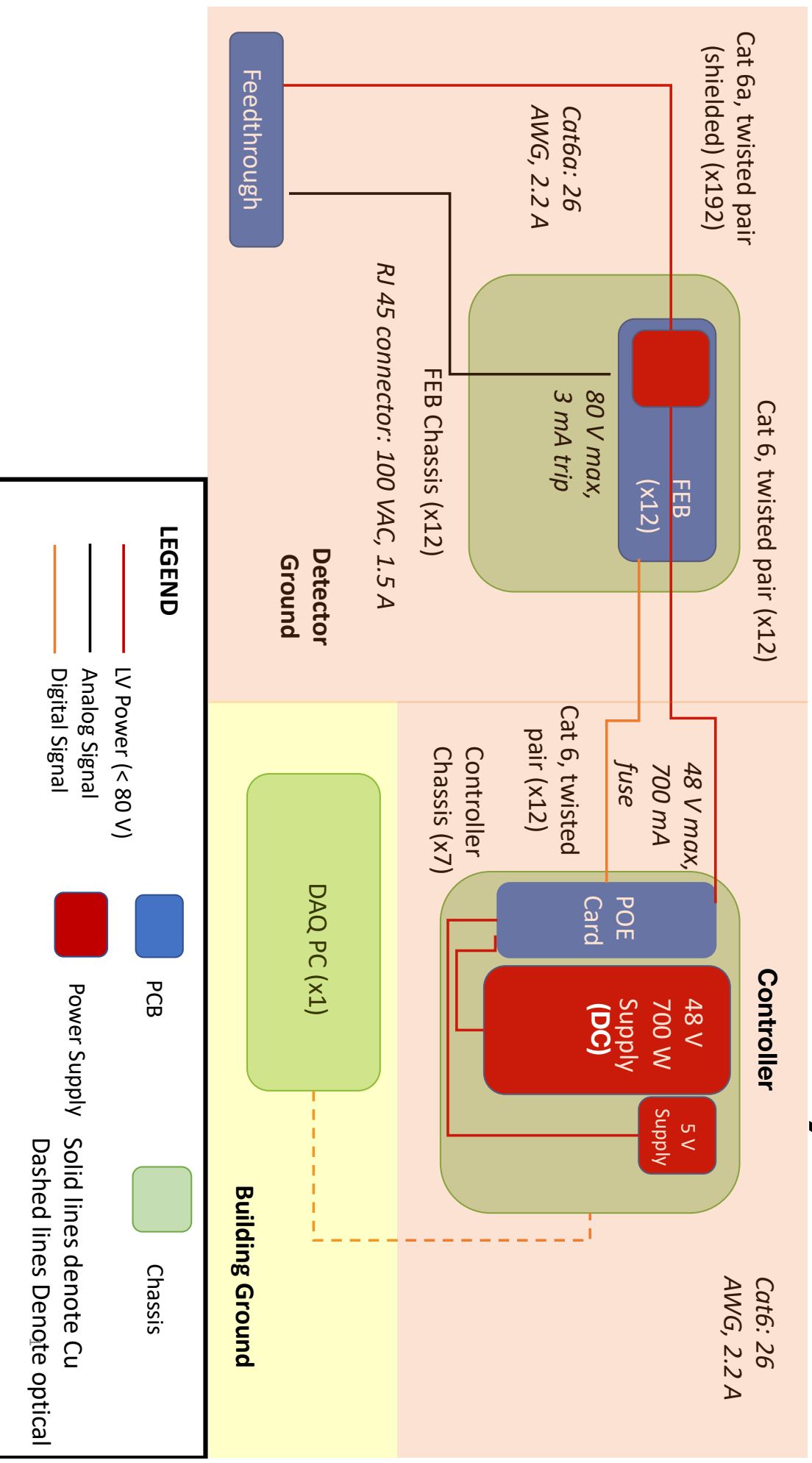
# Rack space and power consumptions

- 6000 channels total; assume 40 channels/FEB
- 12 FEB/chassis, 13 chassis (6u each) required for FEBs.
- 7 controllers (controlling 24 FEB each), 1 u each.
- ~85u required. Assuming 42u/rack, we will need just over 2 racks.
- Power supply on a controller is 700 W, each FEB takes 20 W.

# Grounding scheme



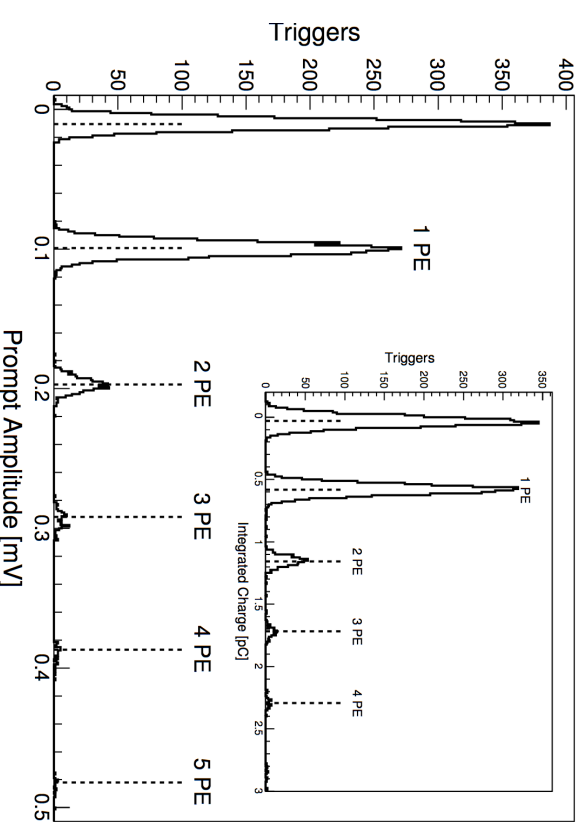
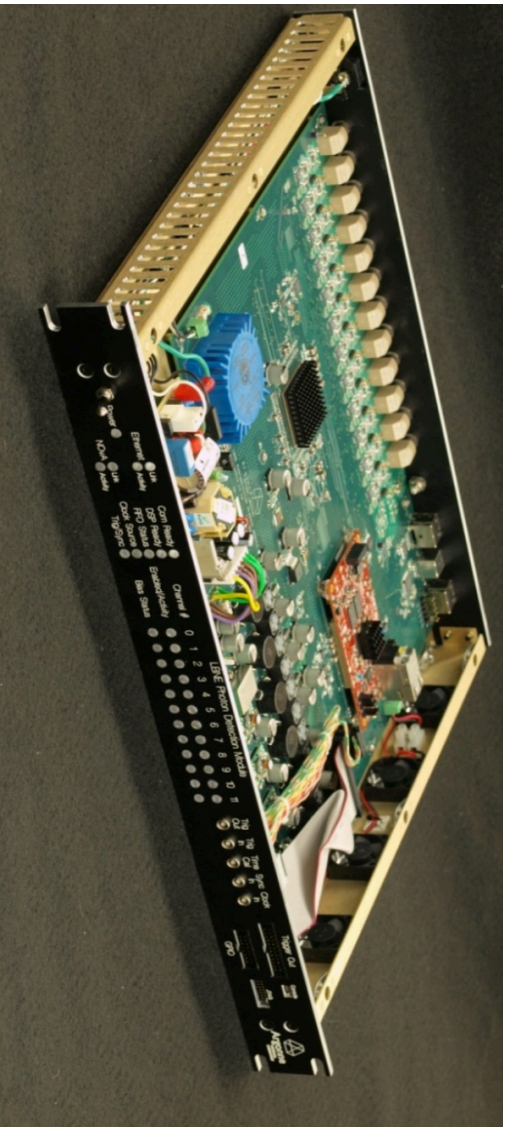
# Other option (optical from controller to DAQ)



# Alternative front-end (SSP) (in ProtodUNE)

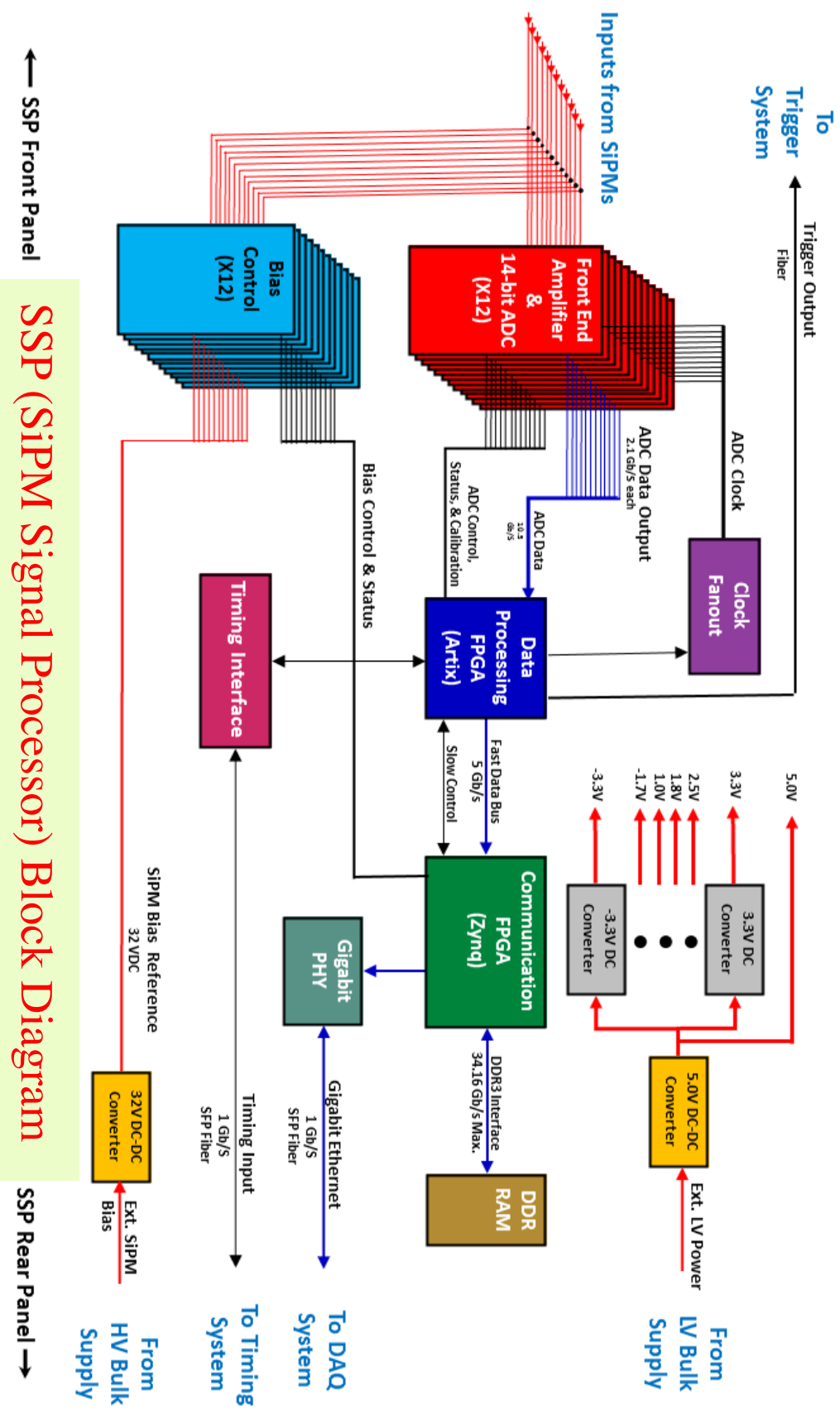
- Argonne SSPs (150 MS/s, 14 bit) [comparing to 80 MS/s, 12 bit]
- Higher cost with significantly more utility
- Multiple onboard utilities for online signal characterization
- Used in ProtodUNE (288 channels)

**JINST 11 P05016 (2016)**





# Alternative front-end (SSP)



From Zelimir Djurcic

# Main issues moving forward

- Demonstrate full FEB+controller+DAQ chain (and merging with TPC info) in ICEBERG.
- Develop solution for active summing board's power.
- Possible board re-designs
  - 48 channel board re-design (from 64 channels)?
    - 40 channels (1 APA) + 8 spare?
  - Power scheme, including both MPPC and active summing board bias?
  - Cat6 instead of HDMI?
- Explore the possibility of using DC power input to the controller (perhaps from a Weiner supply), in consideration of noise issues.
- Develop firmware and zero-suppression (including multi-channel coincidence+threshold on FEB) scheme.
  - Considerations: DC rate, radiogenics rate, maximum instantaneous rate