Cold Electronics Cable Plant in the LAr

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Fermilab

Cold Electronics Mechanical Review

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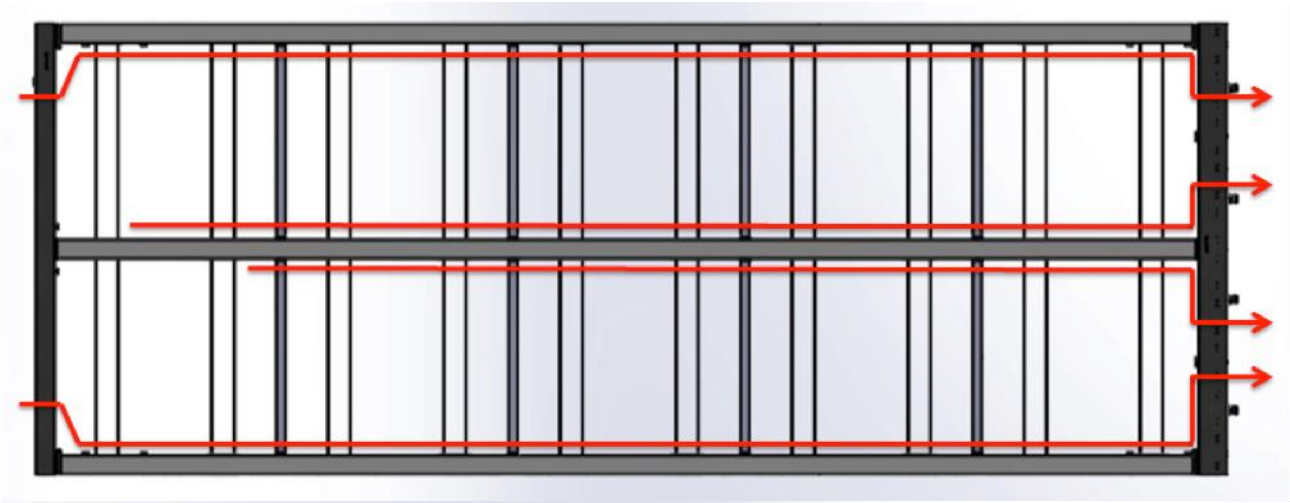
Cold Cables (i)

- Cables inside the LAr
  - PDS cables: 1 Cat 6 Ethernet cable for each photon detector bar (10 per APA)
  - APA/HV (CE responsibility): 8 RG-316 coaxial cables per APA to provide bias voltage to wire planes, field cage termination electrodes, electron diverters
  - CE: for each FEMB (20 per APA) 1 cable bundle to provide power to the FEMB and ASICs, 1 cable bundle to provide clock/controls and read out digitization of wire information
- All PDS cables for 2 APAs go to one flange on the top of cross-shaped spool piece
- The CE cables from the same 2 APAs go to the two flanges on the sides of the cross-shaped spool piece (no mixing at the flange level)

Routing of PDS cables (i)



Top APA

Bottom APA

Routing of PDS Cables (ii)

- PDS cables are segmented in 2 parts (top APA) or 3 parts (bottom APA)
- Connection of bottom/top APA takes place outside the clean room in front of the cryostat
- 4 bundles of 5 cables each:
  - 2 at the sides of the top APA
  - 2 at the center of the top APA
- Connection of cable segments going from head tube of top APA to PDS flange done inside the clean room in front of the cryostat
- In the following we are assuming that there will not be any change of the PDS cable type / connectors
  - I think that there should be a risk associated to this until design of photon bars (including FE electronics) is finalized and tested

Cold Cables (ii)

- Bias voltage cables
  - 2 bundles of RG-316 with SHV connectors
  - Connect to SHV board that is one side of the APA
    - 1 bundle on right side of APA (top APA)
    - 1 bundle on left side of APA (bottom APA, it's simply rotated, location of SHV board is the same on both APAs)

Cold Cables (iii)

- FEMB clock/control/readout for ProtoDUNE-SP
- SAMTEC cable with custom printed circuit board as male part of the connector
- 12 low-skew twin-axial cables
  - Four 1.28 Gbps data lines
  - One 100 MHz clock line
  - One MHz clock line
  - Two lines for I2C
  - Four lines for JTAG (only 1 used)

Cold Cables (iv)

- FEMB power cables bundle for ProtoDUNE-SP
  - Nine AWG20 twisted-pair cables with single connector on the CE flange side, two connectors on the FEMB side
    - Analog motherboard, 4 twisted-pair cables
      - 3 pairs for 2.5V (1.1A total) – power to FE ASICs and ADCs
      - 1 pair for 5V (0.01 A) – bootstrap the low voltage converters
    - FPGA mezzanine, 5 twisted-pair cables
      - 1 pair for 3V (0.4A)
      - 1 pair for 1.5V (0.47A)
      - 1 pair for 4.2V (0.06A)
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Insertion Tests

- The size of the side tubes for the APA frames has been increased to 4” x 4” to accommodate the CE cable plant
- To ensure smooth insertion using a conduit with 2.5” outer diameter
- Still we cannot fit a full ProtoDUNE cable bundle for bottom APA inside the conduit
  - 8 RG-316 bias voltage cables
  - Power cables for FEMBs (10 times 9 twisted-pair cables, i.e. 90 twisted-pairs)
  - Clock/control and readout cables for FEMBs (10 times 12 low skew twinax cables, i.e. 120 twinax cables)
- Cables for bottom APA are staggered by 23 cm
  - Use this to spread connectors along the cable

What are the DUNE needs ?

- We have not yet chosen the ASIC set to be used for building the ProtoDUNE FEMBs
  - We do not know how much power the ASICs will consume
    - Have the information for LArASIC, will have it soon for ColdADC and CRYO, in July for COLDATA
    - We cannot design today the cable plant for power distribution
  - We have a better understanding of the clock/control and data readout paths
- Insertion tests that have taken place at PSL and at Ash River (next presentation by Manhong) have been made under certain assumptions

Assumptions made for the tests

- We are still using the “same” ProtoDUNE cable (see comment later): we are stuck with bundles of 12 twinax / 9 twisted-pair wires
- Reduce number of clock/control + readout links from 12 to 10 and instead of using 10 bundles of cables with 10 twinax (100 twinax total), use 9 bundles of cables with 12 twinax (108 winax used in the test)
- Reduce the number of power lines from 9 to 8 and instead of using 10 bundles of cables with 8 twisted pairs (80 twisted pairs) use 9 bundles of cables with 9 twisted pairs (81 twisted pairs used in the test)
- Include the bias cables in the test (in DUNE happens only for one side of the APA)

Does this make sense ? (i)

- Preliminary assignment of clock/control + readout cables for DUNE (LArASIC, ColdADC, COLDATA solution)
  - Four 1.28 Gbps data lines
  - One 62.5 MHz clock line
  - One Fast Command line
  - Three lines for I2C (single ended signals, require more connections)
  - One spare line
- This assumes that the clock and the fast command are shared between the two COLDATA chips
  - No redundancy, will be tested in new FEMB (timescale September)
  - Will also investigate data transmission at 2.56 Gbps for 2nd version of COLDATA (backup plan)

Does this make sense ? (ii)

- Preliminary assignment of clock/control + readout cables for DUNE (CRYO solution)
  - Four 1.28 Gbps data lines
  - Two lines with copies of 56 MHz clock (one for each CRYO chip)
  - Three shared SACI protocol lines
  - Two lines with individual SACI protocol lines (one for each CRYO chip)
  - One spare line
- Reduce to 10 lines by sharing the 56 MHz clock between the two CRYO ASICs, remove spare line
  - No redundancy
  - Could also investigate data transmission at 2.56 Gbps for 2nd version of CRYO (backup plan)

Does this make sense ? (iii)

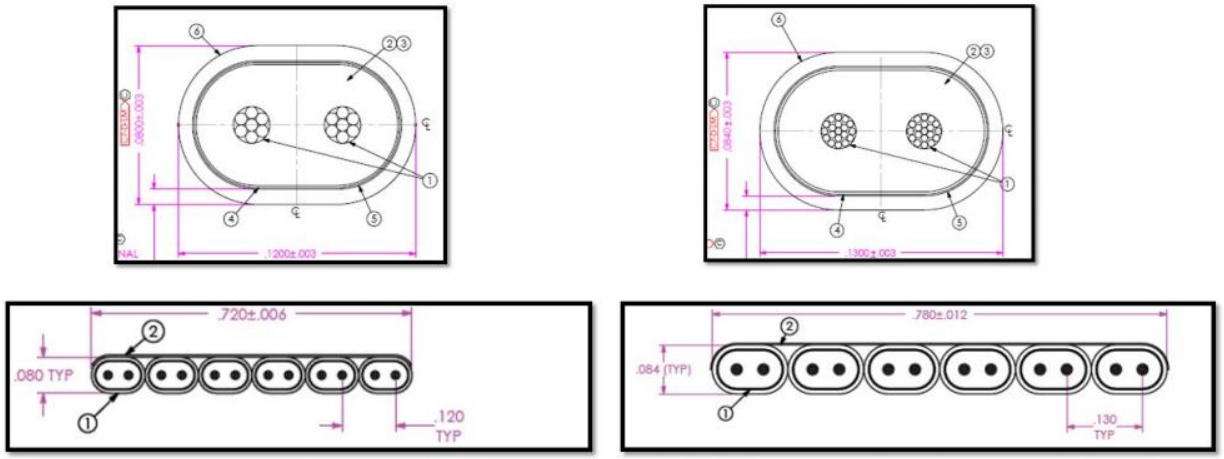
- For control/clock + data readout lines it seems reasonable to assume that we will have only 10 twinax (100 twinax total for APA tube). Test performed with 108 twinax
- For power wires test performed with 81 twisted-pairs wires per APA tube
  - This corresponds to removing only the pair foreseen for test pulses
  - Can probably remove also one of the two 5V lines (very low current, if we need a mezzanine we could route this through the connector between the two boards, not needed if there isn't any mezzanine)
- Removal of FPGA should result in lower power requirements, may lead to further reduction of number of wires.

The “same” Cables as ProtoDUNE ?

- The clock/control and data readout cables we used for the insertion tests are actually bulkyer than the ProtoDUNE ones

Communication with Samtec

- Difference between CCS-192589 and CCS-199713



- ProtoDUNE design **CCS-192589** used a standard 26awg 7 stranded conductor and a thinner Cu Foil shield tape
- ICEBERG design **CCS-199713** uses a larger 26awg 19 stranded conductor and a thicker Cu Foil shield tape to ***improve SI for acceptable conditions***

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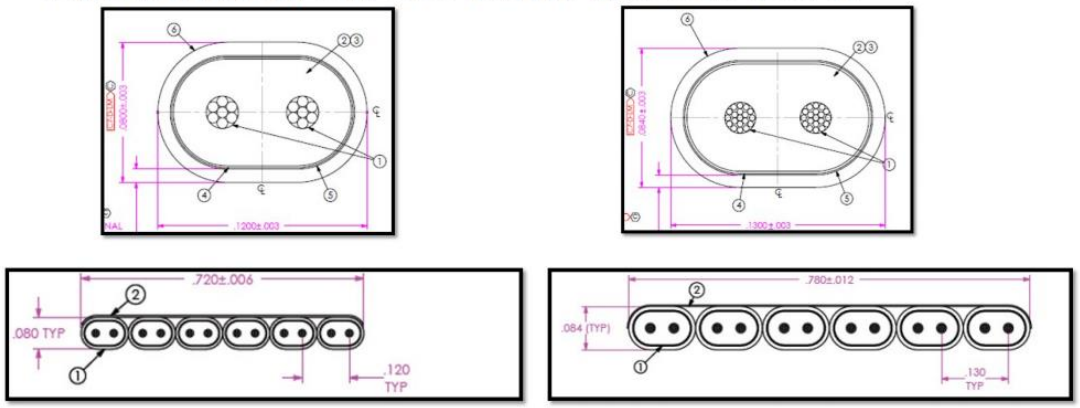
The “same” Cables as ProtoDUNE ?

- The clock/control and data readout cables we used for the insertion tests are actually bulkyer than the ProtoDUNE ones:
  - ProtoDUNE cable: 18.29 mm x 4.19 mm
  - Tests: 19.81 mm x 4.45 mm

- Difference between CCS-192589 and CCS-199713



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Overall Message

- The cable insertion tests performed at PSL and at Ash River are valid
  - We can route the cables through the APA frames using the 2.5” conduit
  - The cross section of the cable plant in DUNE should be smaller

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  - We can route the cables through the APA frames using the 2.5” conduit
  - The cross section of the cable plant in DUNE should be smaller
- For future tests in 2019 we will continue to use the same cables
- Transition to final set of cables will not happen before 2020, with design of FEMBs using 2nd generation of ASICs

Future Insertion Tests (i)

- Spring - Summer 2019
  - Perform tests with DUNE APA frames (as compare to just APA tube) at Ash River
  - Mockup (see Manhong's presentation later) of cryostat penetration and top of APA with cable trays (at BNL)
- Summer – Fall 2019
  - Study what happens when we route cables through APA frame and then go cold (do we pull the cable slack into the APA frame to compensate the shrinkage of the cables ? Are the cables damaged in the cooldown ?)
    - Test to be performed at CERN using the cold box (not exactly LAr temperature but close) using an APA frame tube (and a weight to simulate the rest of the cables ?)

Future Insertion Tests (ii)

- 2nd half 2020
  - Finalize cable plant and purchase prototypes of final cables
  - Repeat insertion test at Ash River with APA pair
  - Repeat test in cold box at CERN and check that cable is not damaged when cooled down (cable slack slides easily inside the conduit in the APA frame tube)
  - Repeat cable insertion tests through cryostat penetrations
- Later
  - Mockup of integration and installation activities at Ash River