ADC Calibration for LArTPC Electronics

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Outline

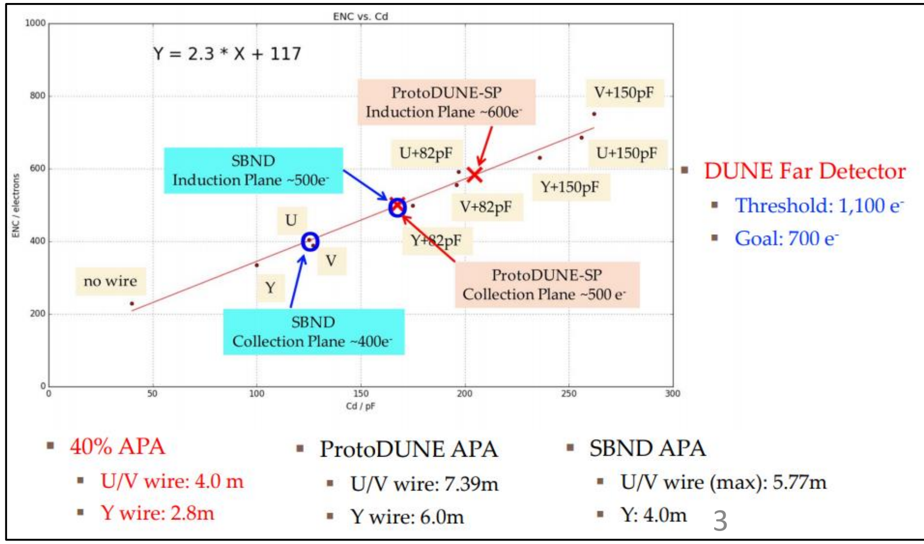
- Cold electronics for the LArTPC
- Sticky code mitigation
- ADC nonlinearity (NL) calibration
- Summary

V. Radeka et al., **Cold electronics for 'Giant' Liquid Argon Time Projection Chambers**
J. Phys. Conf. Ser. 308 (2011) 012021

Cold electronics for the LArTPC era

- Cold electronics (CE) is crucial for reducing noise in LArTPC (at ~89K)
- MicroBooNE first achieved excellent noise performance (ENC ~400 *e*⁻) with the preamplifier installed in LAr → 5-6 times improvement
- ProtoDUNE-SP has a design of 600 *e*⁻ ENC in the induction plane (~7.4m wires)
- SBND and DUNE (far) would be at similar level

	Preamp	**ADC**
MicroBooNE	Cold	Warm
SBND	Cold	Cold (COTS)
ProtoDUNE-SP	Cold	Cold
DUNE Far Detector	Cold	Cold

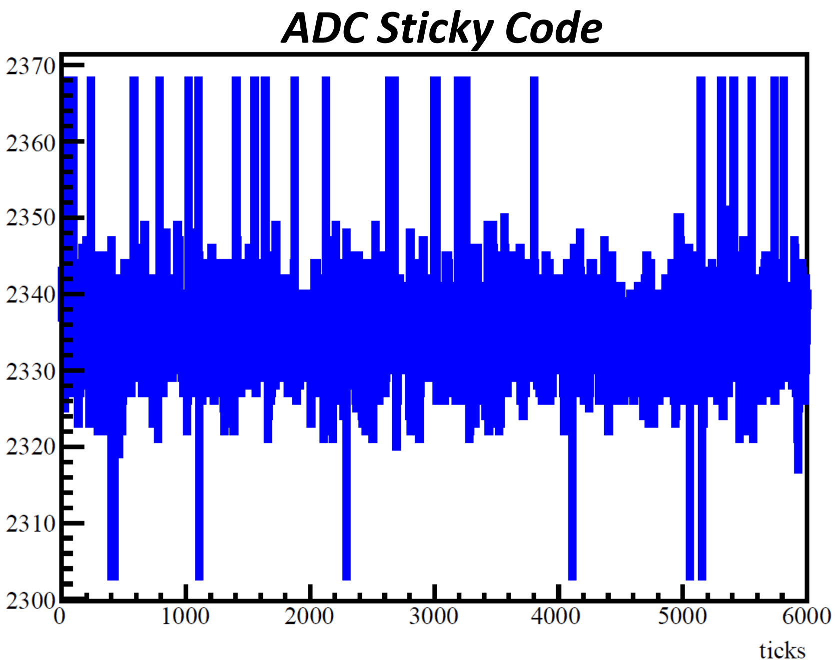


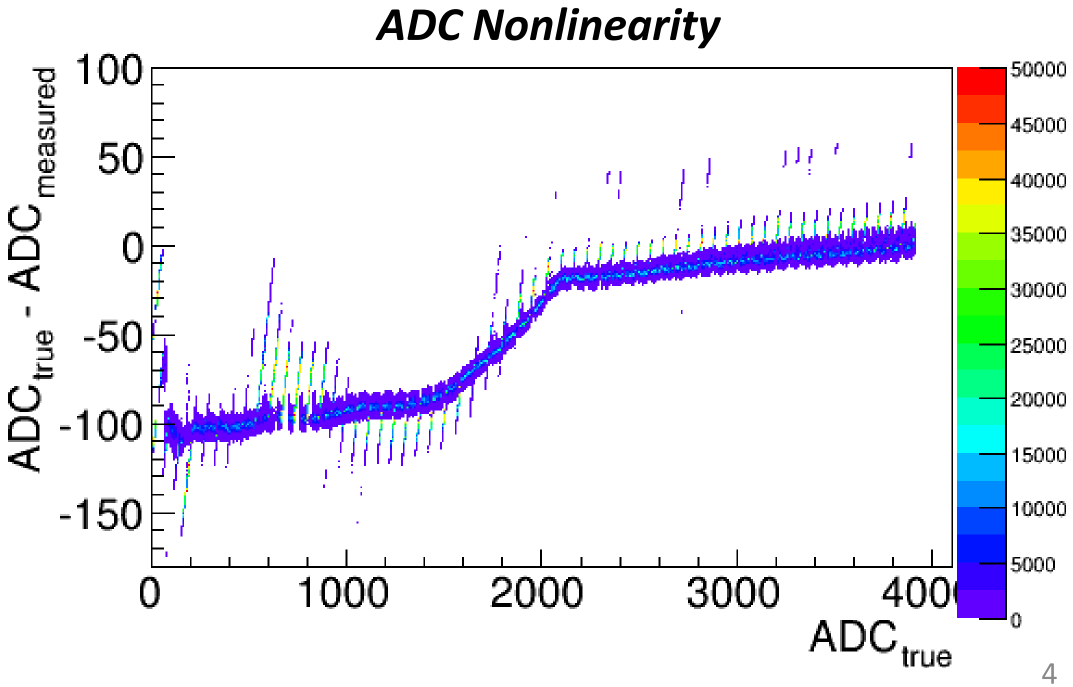
- DUNE Far Detector
  - Threshold: 1,100 e⁻
  - Goal: 700 e⁻

- 40% APA
  - U/V wire: 4.0 m
  - Y wire: 2.8m
- ProtoDUNE APA
  - U/V wire: 7.39m
  - Y wire: 6.0m
- SBND APA
  - U/V wire (max): 5.77m
  - Y: 4.0m

Precise ADC determination in protoDUNE

- However, given the cold environment in LAr, two problems occur for the precise determination of ADC





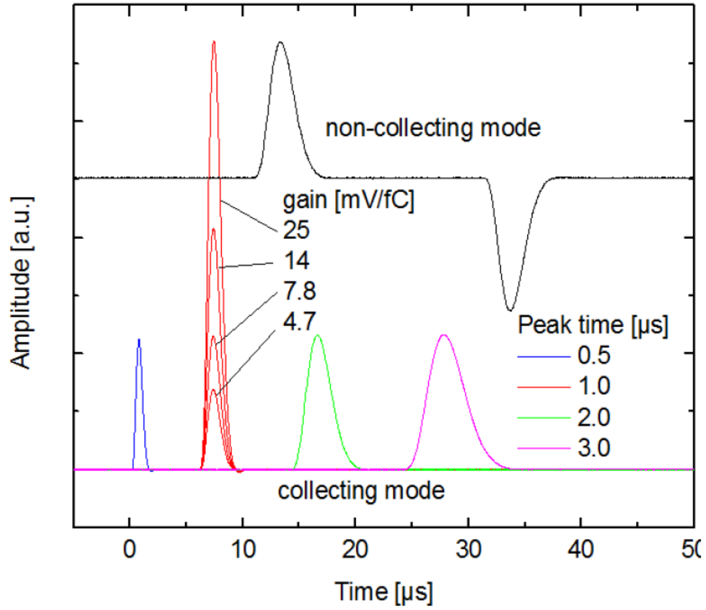
ProtoDUNE TPC readout electronics

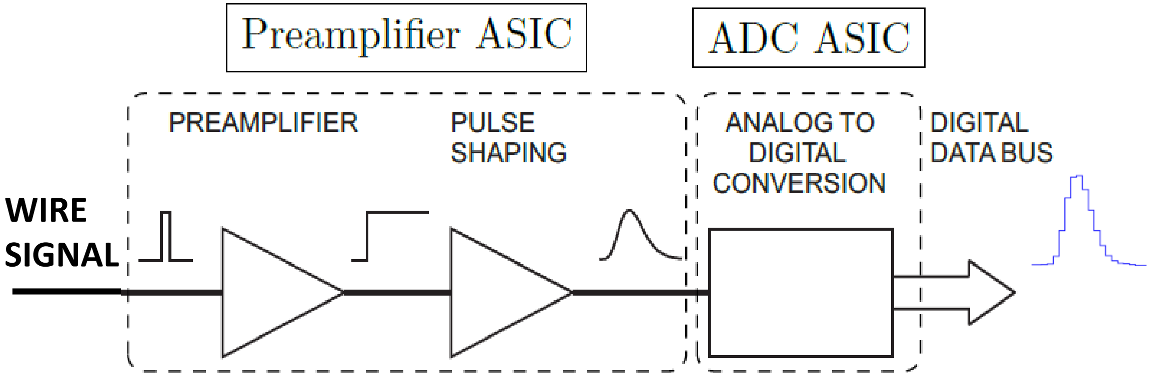
ProtoDUNE TPC readout electronics

- Cold preamplifier
  - Gain: 4.7, 7.8, 14, or 25 mV/fC
  - Shaping time: 0.5, 1.0, 2.0, or 3.0 µs

- Cold ADC (Analog to Digital Converter)
  - 12 bits: 4096 minimum steps in full range (0.2V ~ 1.6V)
  - 2 MHz sampling rate

protoDUNE: 14 mv/fC + 2.0 µs





V. Radeka et al. *Cold electronics for 'Giant' Liquid Argon Time Projection Chambers*, *J. Phys. Conf. Ser.* **308** (2011) 012021.

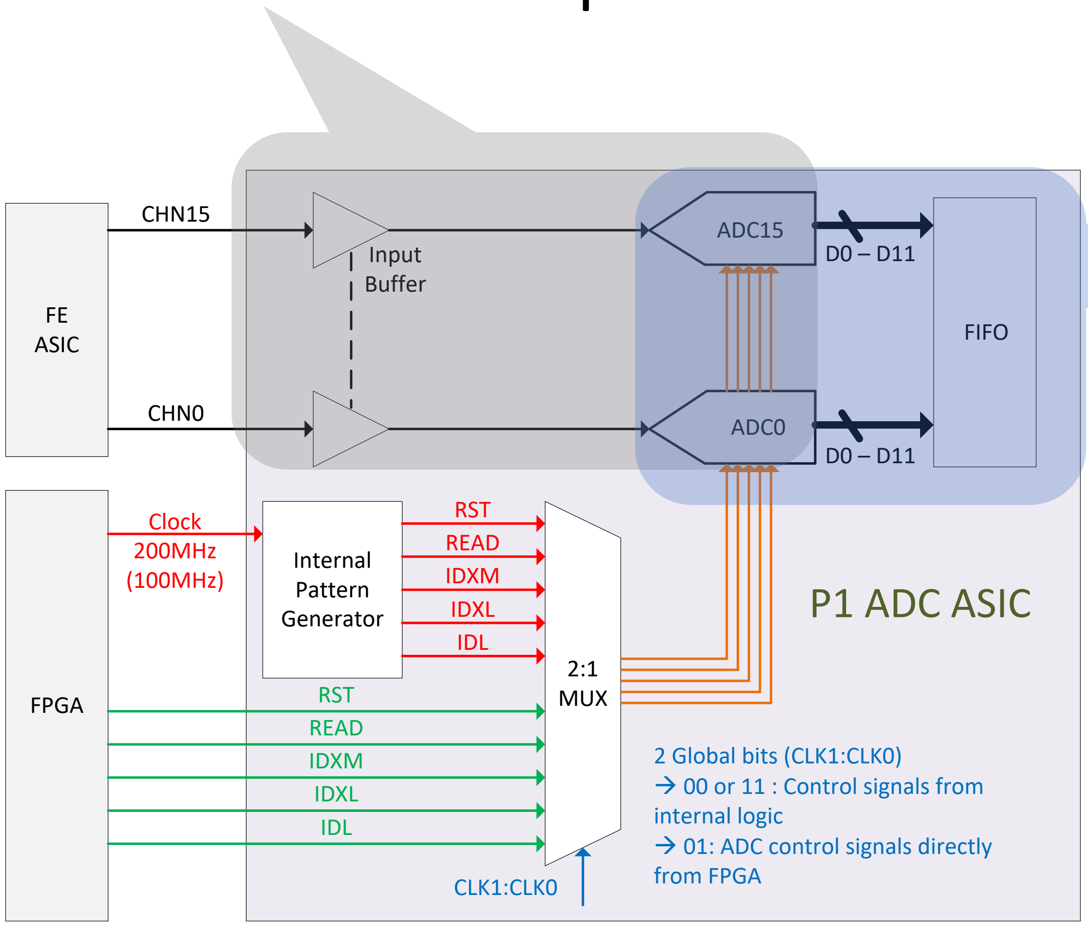
Readout scheme of ADC circuit

- 16 channels per ADC circuit

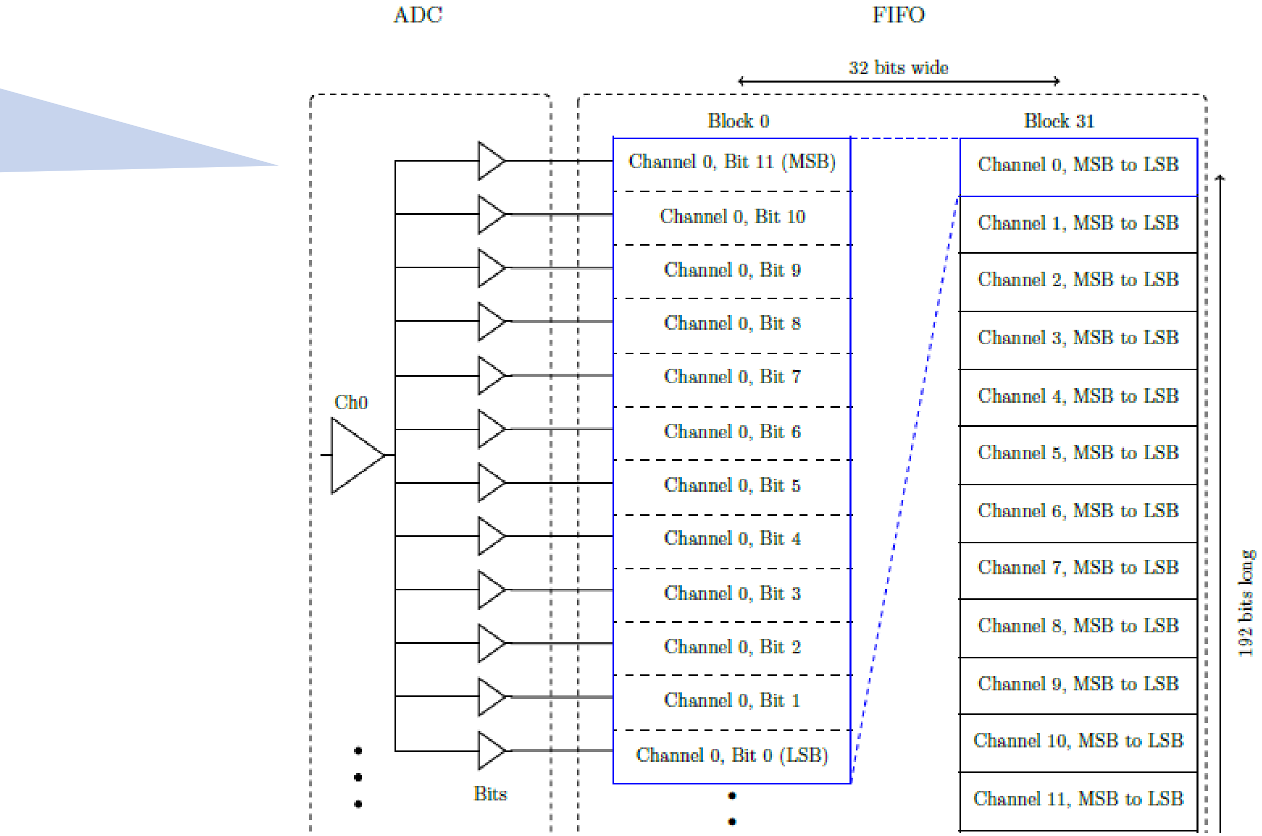
- 12 bits per channel **saved** in a FIFO buffer

e.g. 2048 = 100,000,000,000

Most significant bits (MSB) *Least significant bits (LSB)*

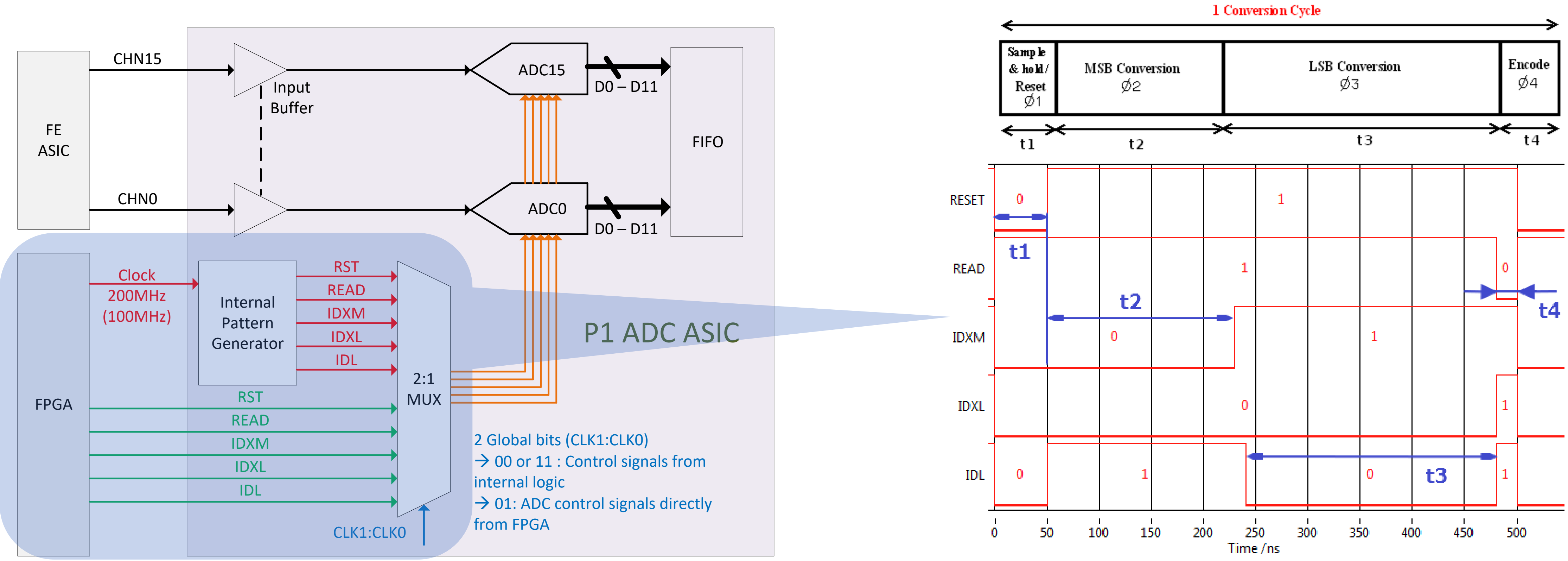


2 Global bits (CLK1:CLK0)
→ 00 or 11 : Control signals from internal logic
→ 01: ADC control signals directly from FPGA



Readout scheme of ADC circuit

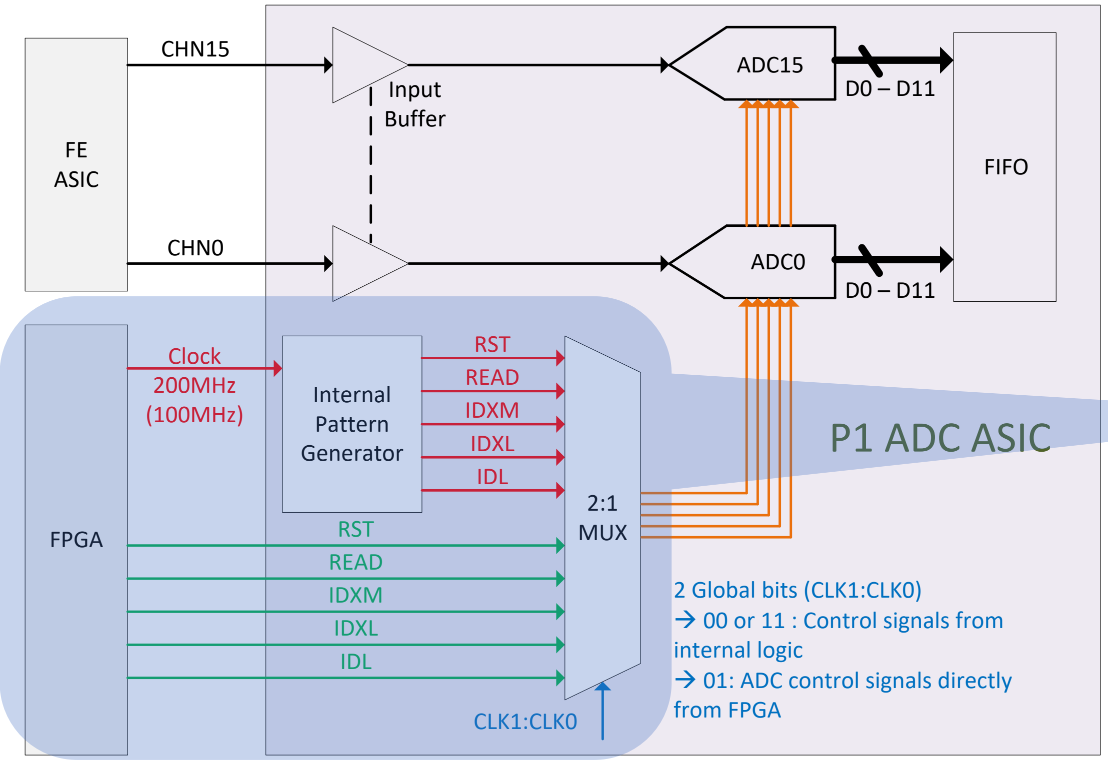
- The read/write logic must be synchronized through five control signals



2 Global bits (CLK1:CLK0)
→ 00 or 11 : Control signals from internal logic
→ 01: ADC control signals directly from FPGA

Readout scheme of ADC circuit

- These five signals can be generated **internally** inside the ADC by a 200 MHz clock (2 MHz digitization) or taken **externally**



2 Global bits (CLK1:CLK0)
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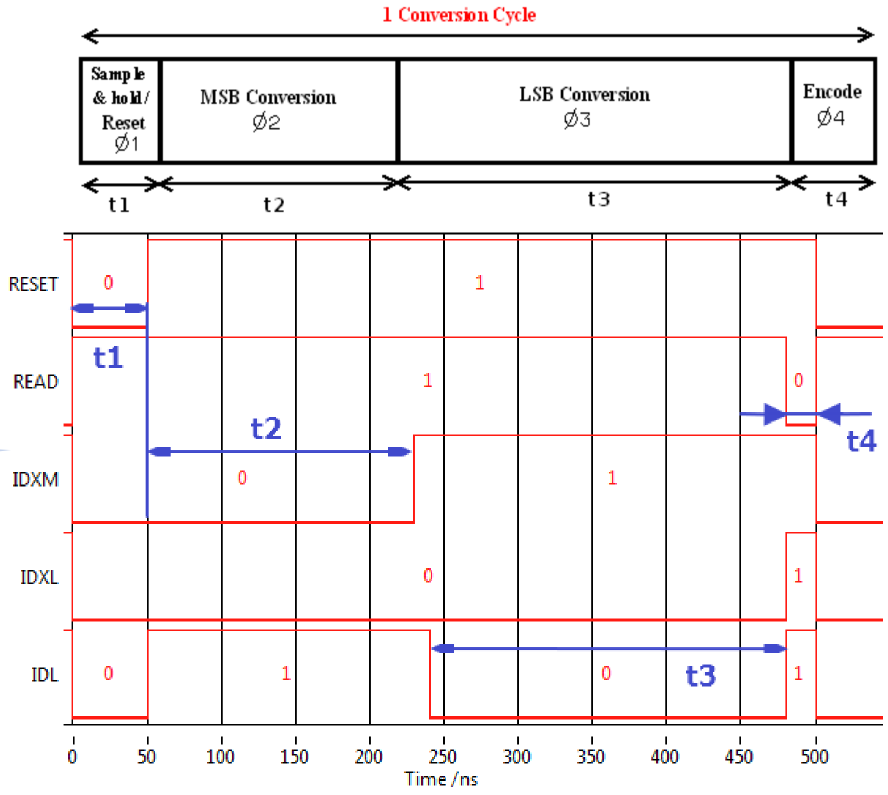
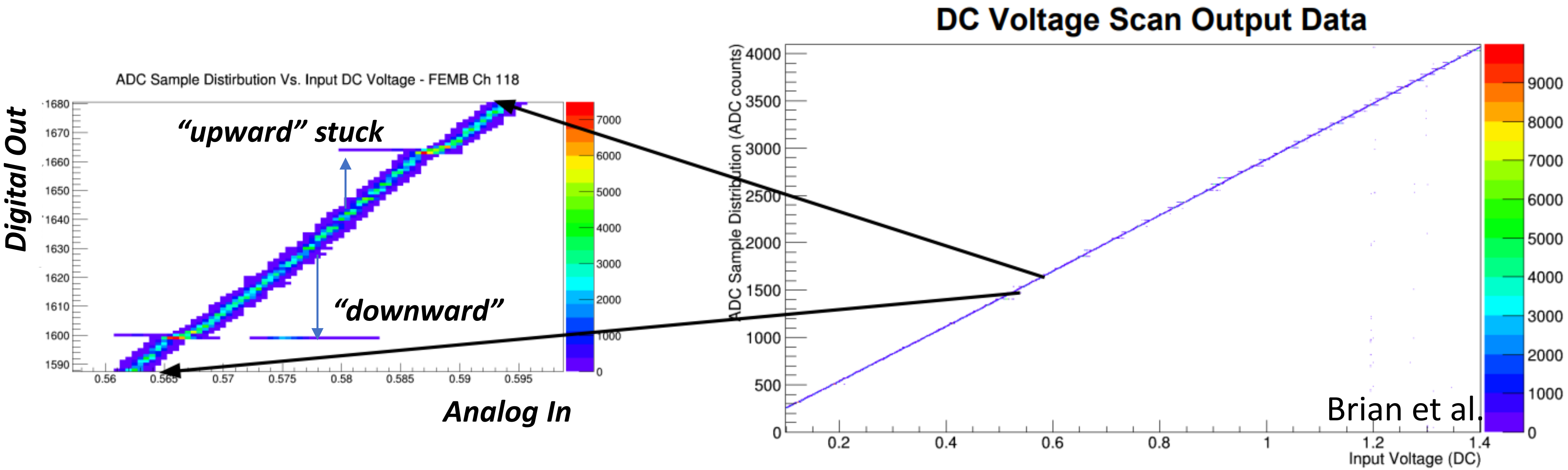


Sticky code mitigation

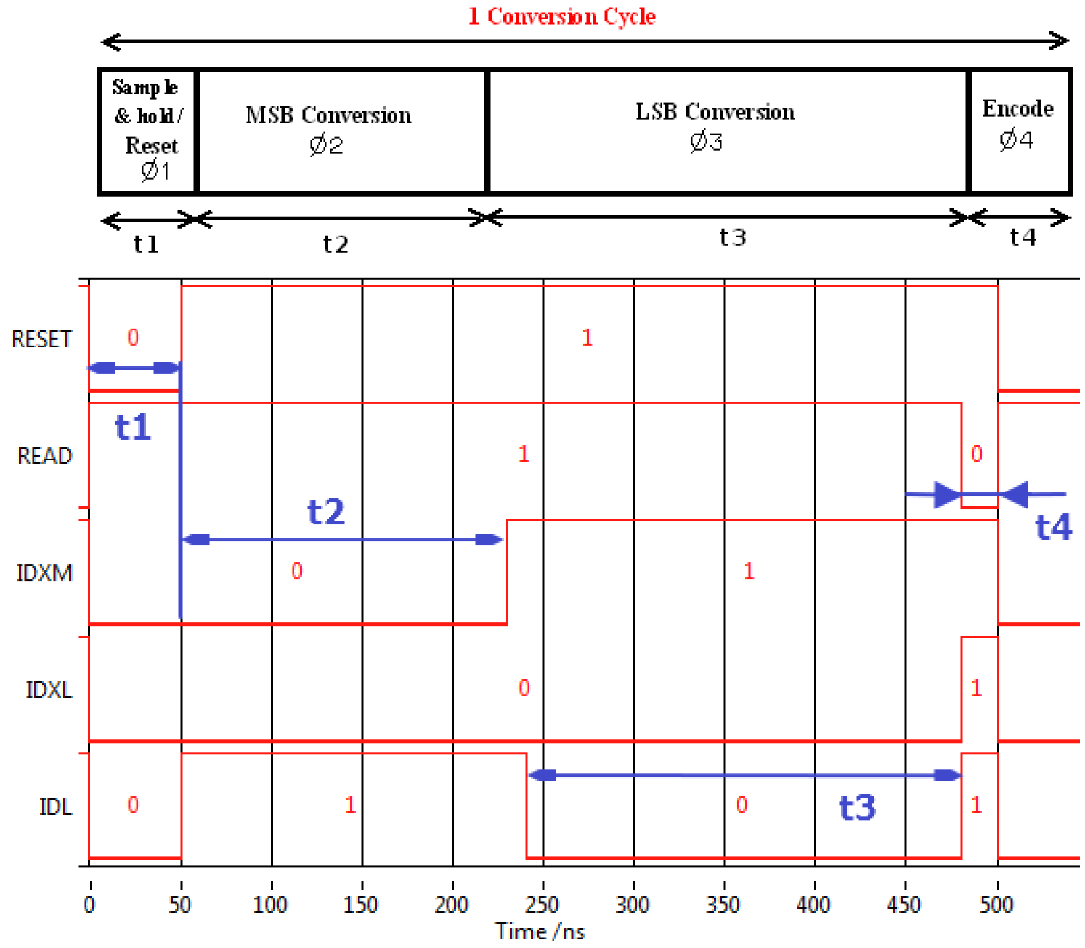
Sticky Code

- The 6 LSBs in ADC ASIC was found to be “sticky” around 000000 (0x00) or 111111 (0x3F)
- So called sticky code, or stuck bit



ADC Digitization and Sticky Code

- Two stages of a 12-bit digitization
  - 6 MSBs (most significant bits)
  - 6 LSBs (least significant bits)
- The 6 LSBs are held until the MSBs are converted to binaries
- An instability during the MSB and LSB phases results in either all LSB codes 0, or all LSB codes 1



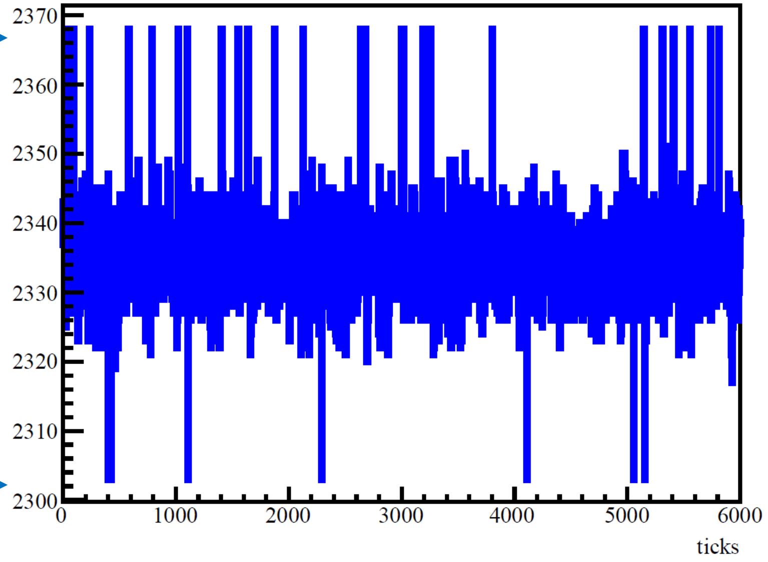
Identification of sticky code

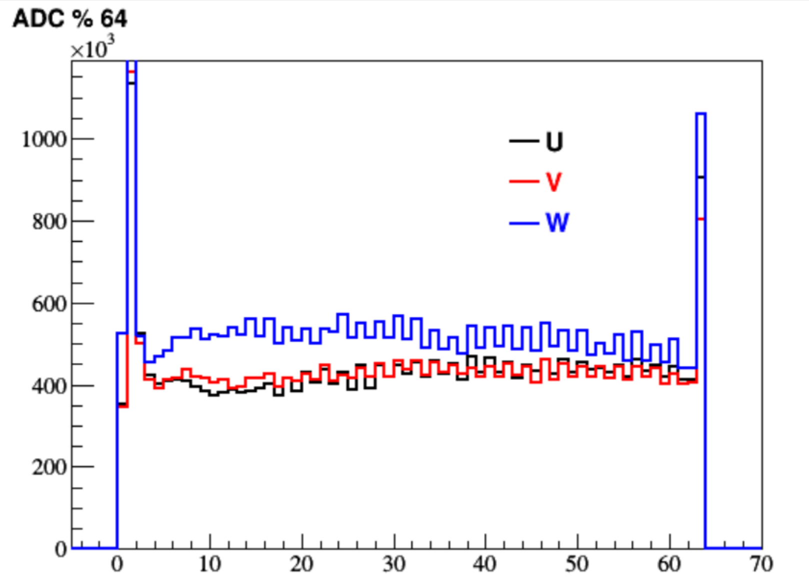
- By taking modulo of 64 (LSBs=111111), 0, 1, 63 usually indicates sticky codes
- A waveform correction will be applied in each “sticky” channel

An example of pedestal waveform

$2368 = (100101000000)_2$

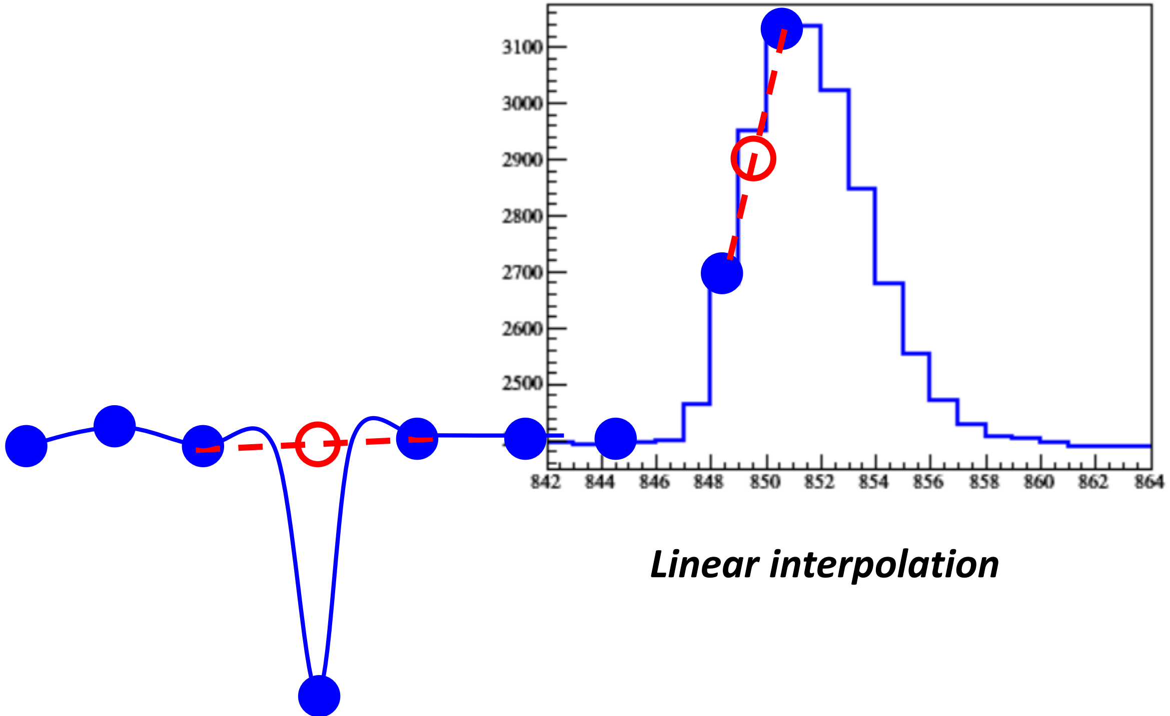
$2303 = (100011111111)_2$



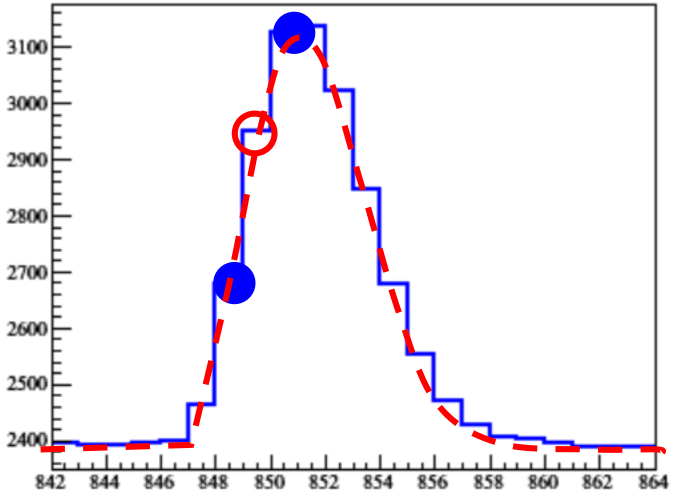


Sticky Code Mitigation

- Linear interpolation between “un-sticky” codes is a good first step
- However, linear interpolation may not be sufficient for signal region
- A correction w.r.t. the electronics response function would be better



Linear interpolation



W.r.t response function

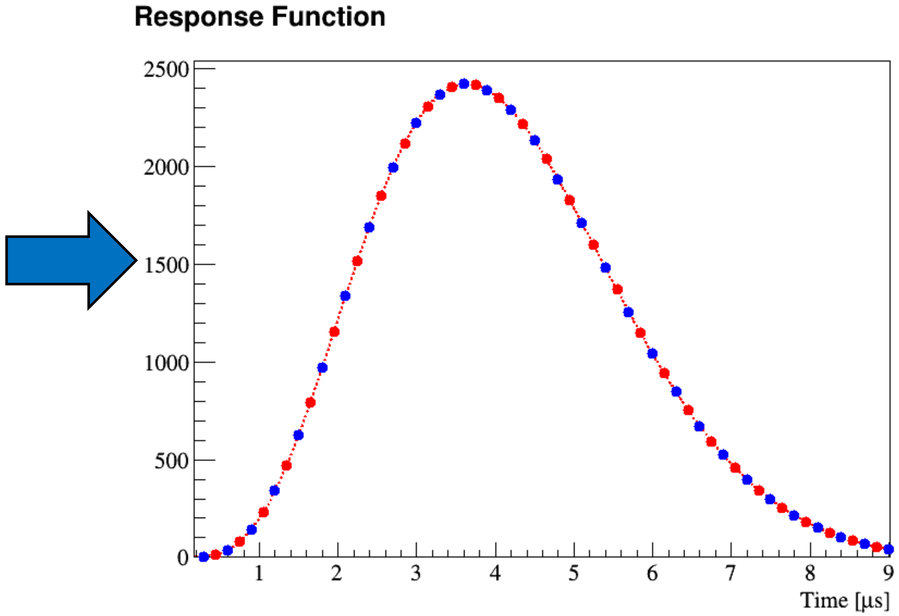
FFT interpolation w.r.t electronics response

- However, some facts makes it difficult for using the response function
  - A few percent channel-to-channel variation in response function
  - Changes due to the cold environment
  - Coupled with ADC nonlinearity (discussed shortly)
- Instead, a FFT interpolation is proposed by

  i) Linear interpolation as a base correction

  ii) Once a "sticky" code found in an even-binned tick, apply phase shift to odd-binned ticks to cover even-binned ticks, and *vice versa*

FT property	Time domain	Frequency domain
	$f(t)$	$F(\omega)$
Phase shift	$f(t-t_0)$	$F(\omega)e^{-j\omega t_0}$

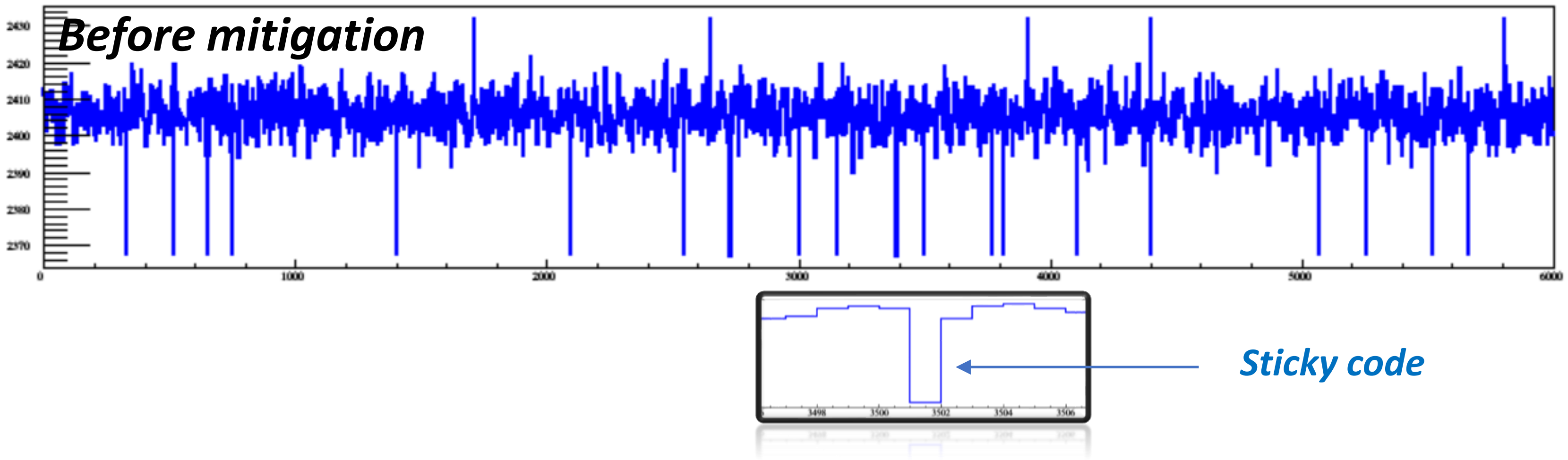


Advantages of such FT interpolation

- Only the phase changed, while no changes of the magnitude in the frequency domain
  - Still respect the shape of the electronics response function

- Sometimes, good code tagged as “sticky”, the FT interpolation presumably minimize the biases
  - Balance of efficiency and accuracy for sticky code tagging

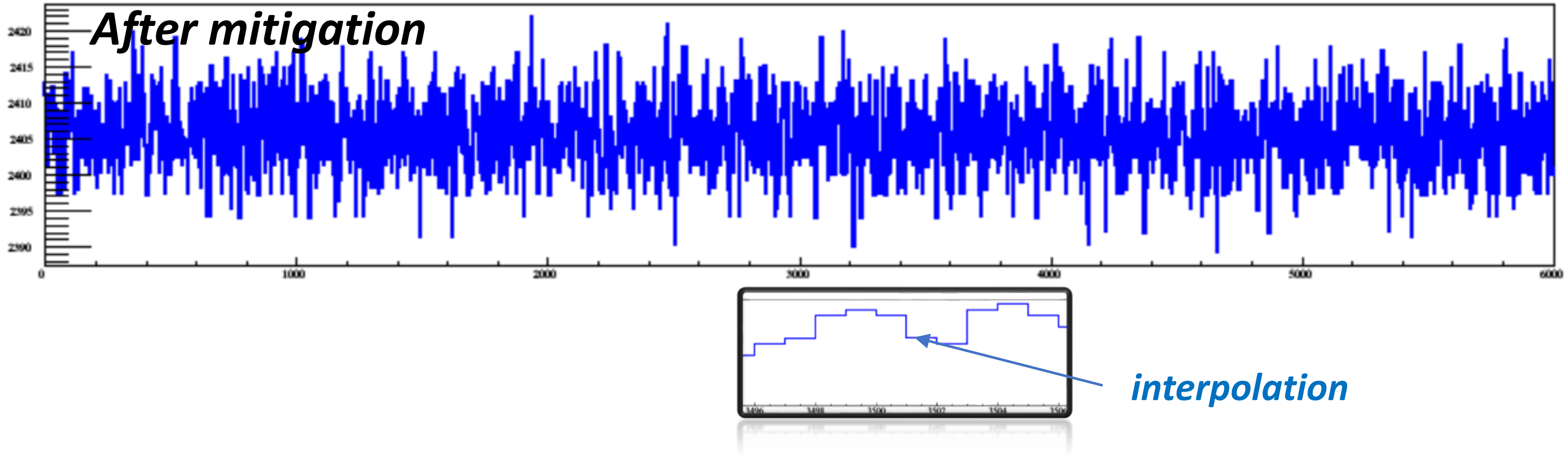
Performance of ADC mitigation



Channel 7699

Before mitigation

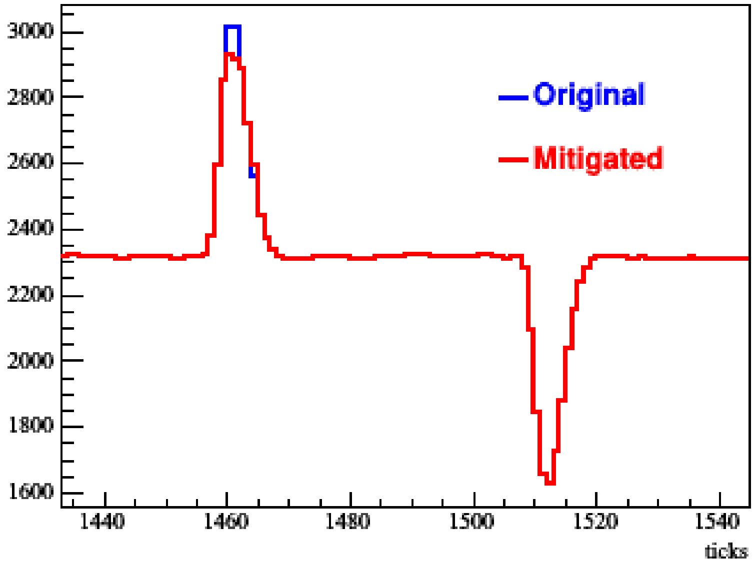
Sticky code



After mitigation

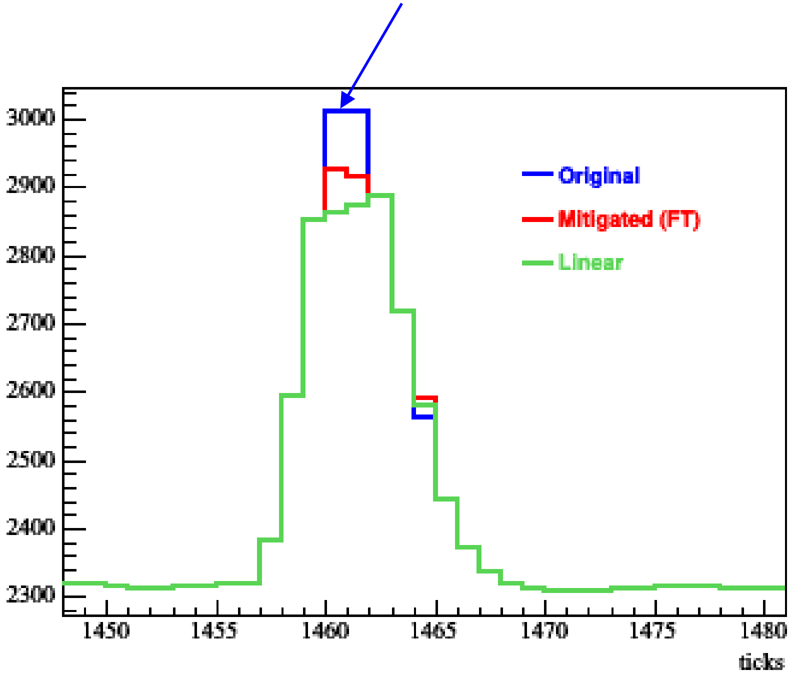
interpolation

Preamp pulser data



Zoom-in

Sticky at 3008 = $(101111000000)_2$



- However, when two adjacent sticky codes happens on the peak region, the mitigation does not work well
- Need to improve this special case
    - Maybe ignore the base correction from linear interpolation

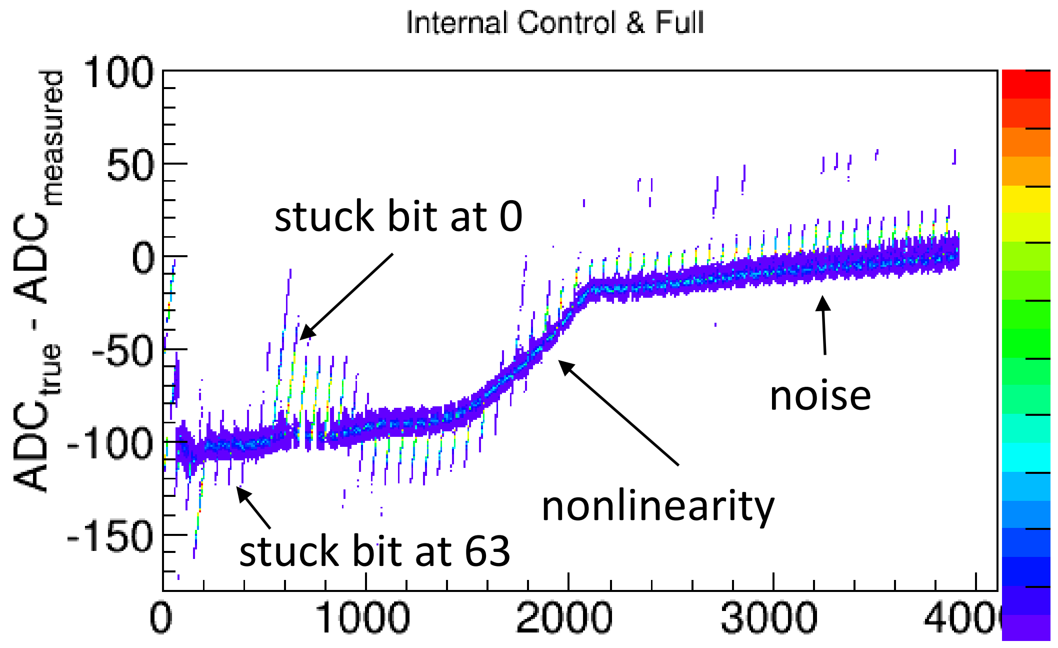
Short summary on sticky code

- Sticky code is caused by the electronics instability during the MSB and LSB conversion phase
- Sticky code mitigation was preliminarily studied with protoDUNE data
- A linear interpolation and a FT interpolation was applied, some special cases needs to be improved

ADC nonlinearity calibration

ADC nonlinearity

- ADC nonlinearity (NL) is a common issue even for warm electronics
- However, low temperature degrades the electronics and read/write logics
- External clock eases NL as well as sticky code
- NL is sensitive to clock settings

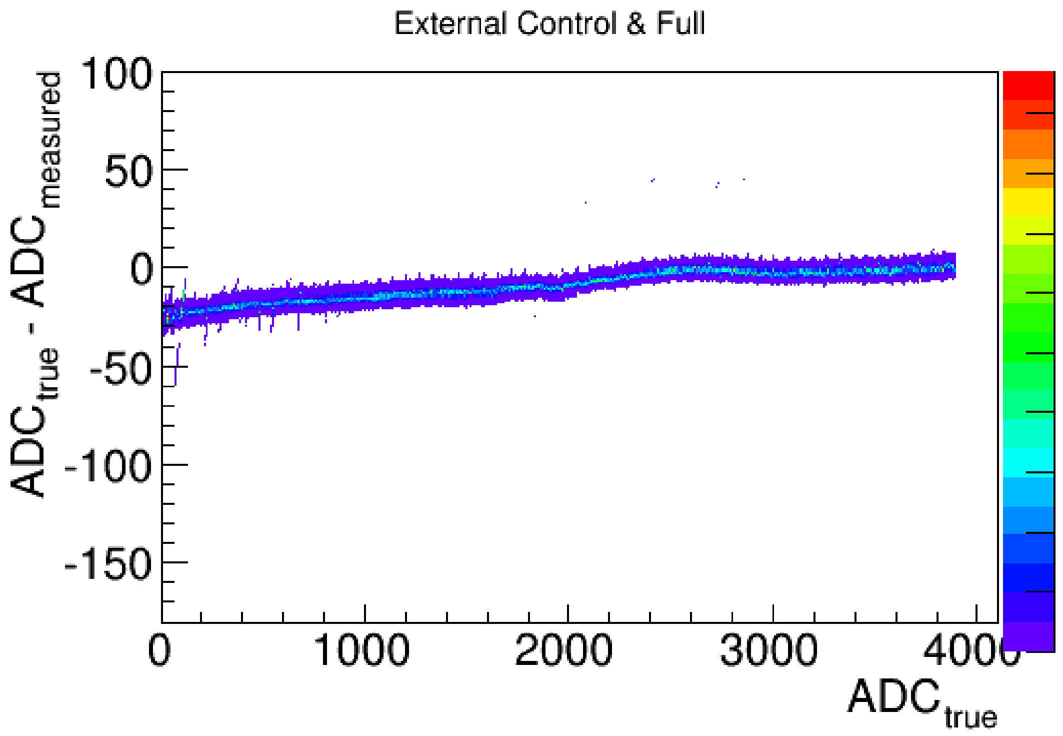


stuck bit at 0

stuck bit at 63

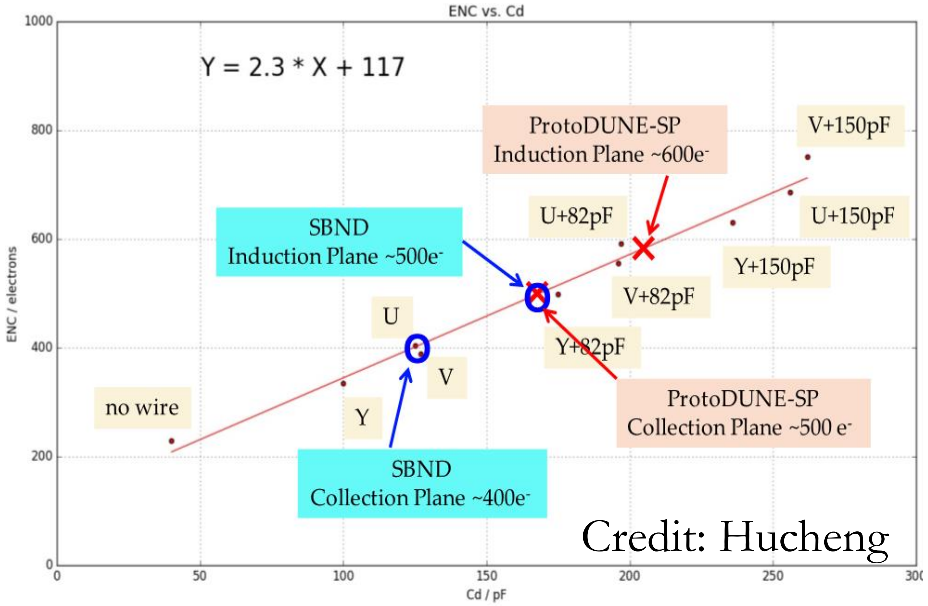
nonlinearity

noise

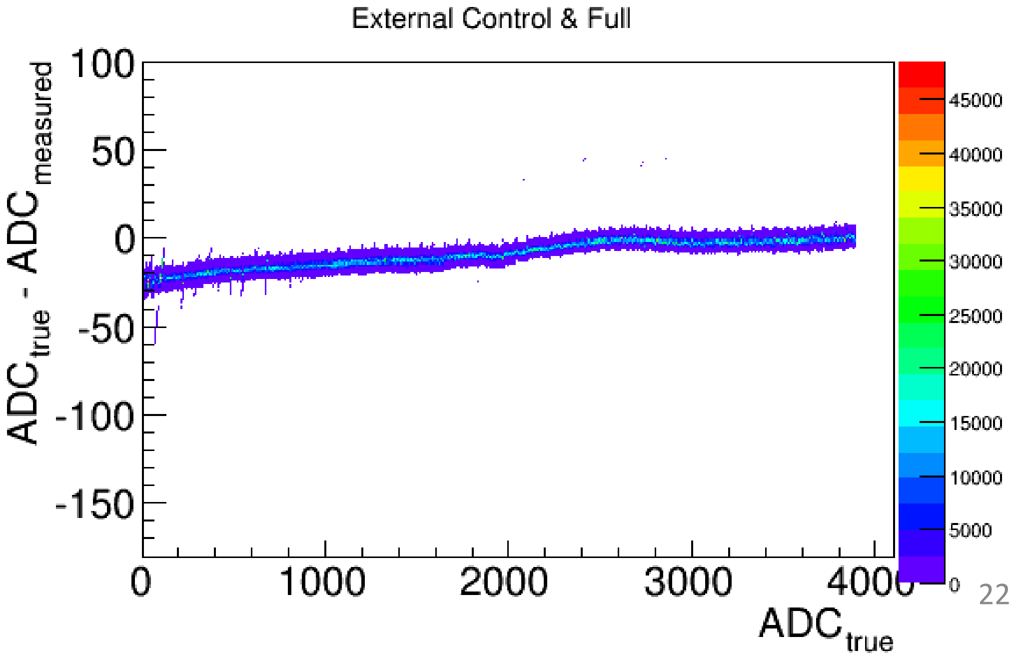


Motivation of the NL calibration

- 600 e^- ENC at ProtoDUNE (≈ 4 ADCs)
- Would like to control the NL below 4 ADC in the useful range
- A precise determination of ADC would be very important for the extraction of ionized electrons and PID analysis

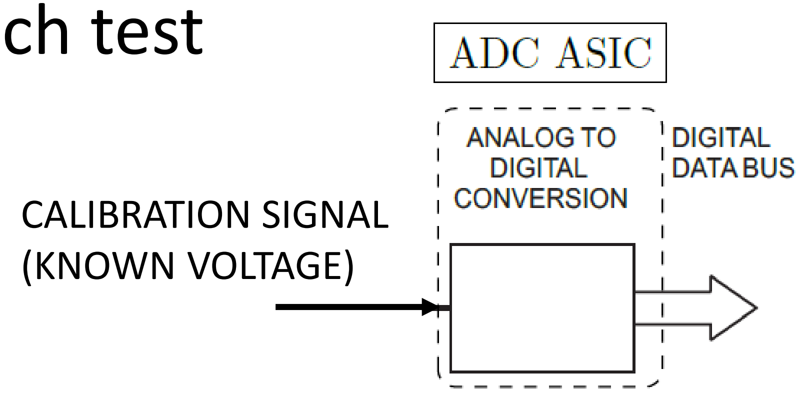


Credit: Hucheng



Difficulties from a bench test to protoDUNE

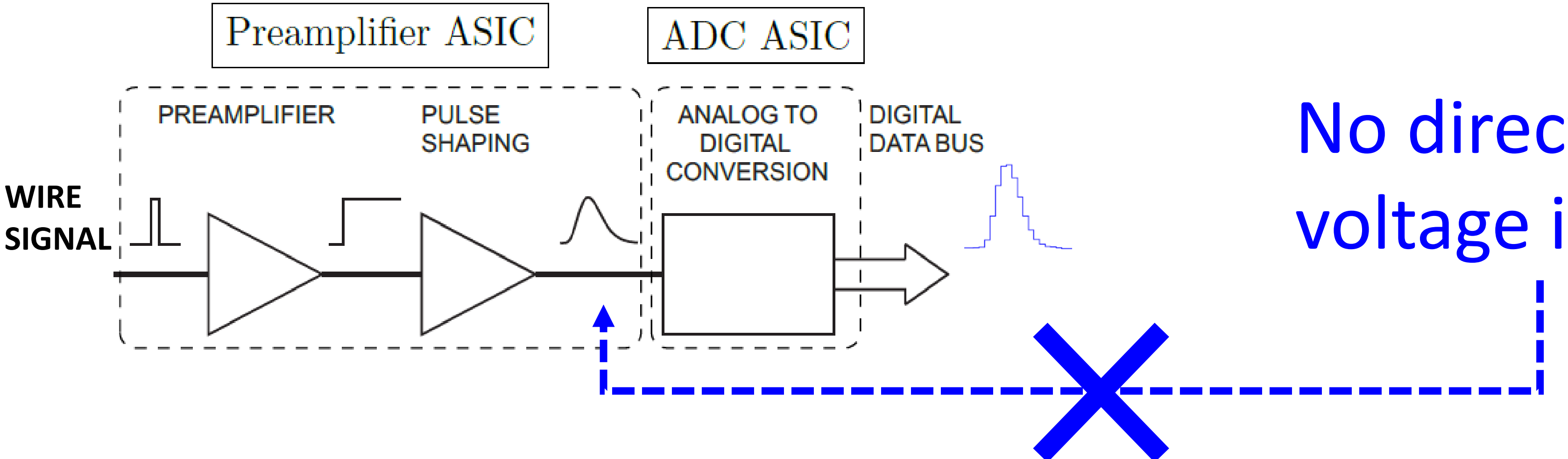
- Bench test



NL is sensitive to clock settings

- (bench test) clock is tuned for each ADC
- (protoDUNE) one clock shared by four ADC curcuits

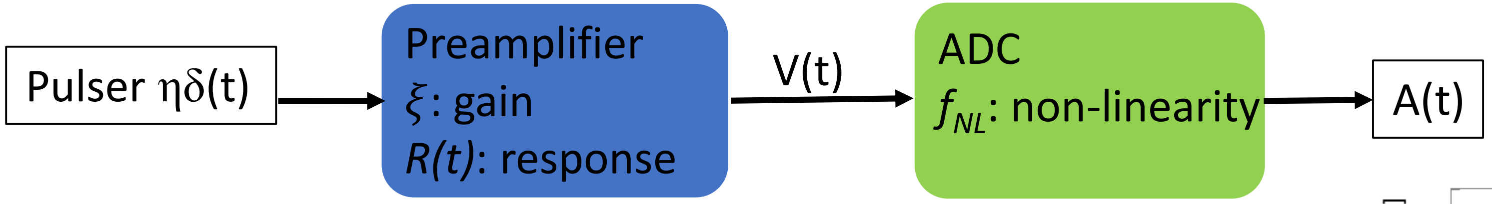
- ProtoDUNE



No direct voltage input!

C. Adams et al., *Ionization Electron Signal Processing in Single Phase LArTPCs II. Data/Simulation Comparison and Performance in MicroBooNE*
arXiv:1804.02583

Idea of the NL calibration setup

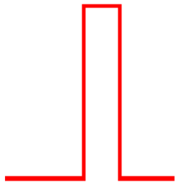

Pulser ηδ(t)

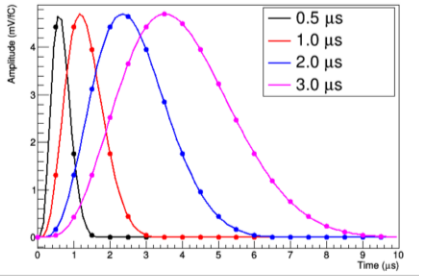
Preamplifier
ξ: gain
R(t): response

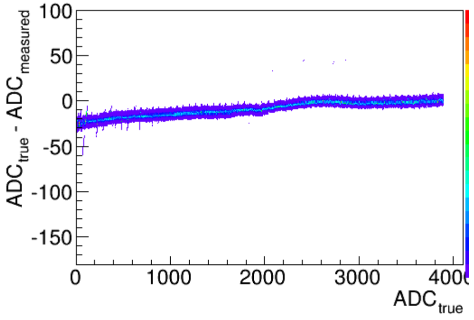
V(t)

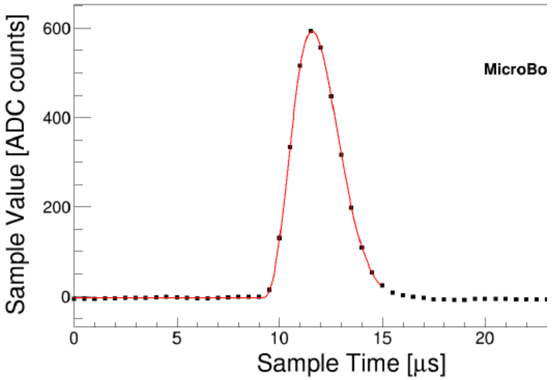
ADC
f_{NL}: non-linearity

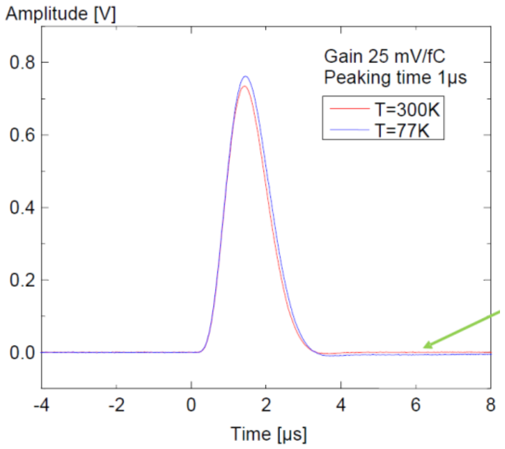
A(t)







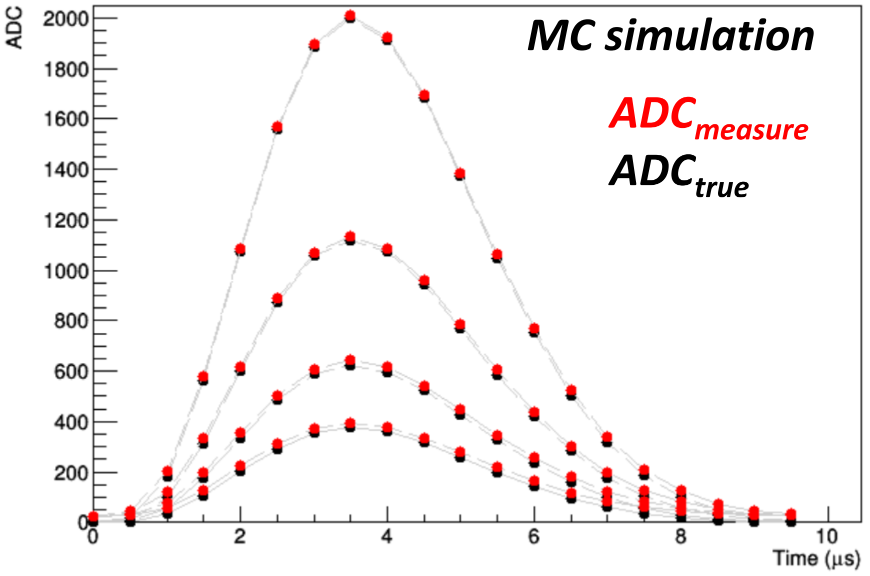


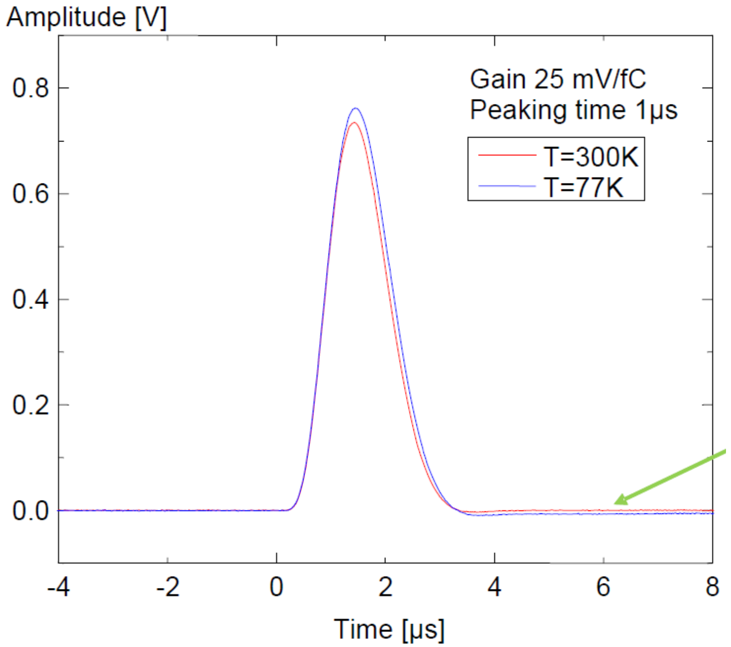


Caveat: cold environment also changes the response

- Similar setup as in MicroBooNE electronics calibration
  - 6 bit pulser, i.e. 64 programmable amplitudes (<1.4V)
  - four adjustable gains of preamplifier

Direct measurement of NL?

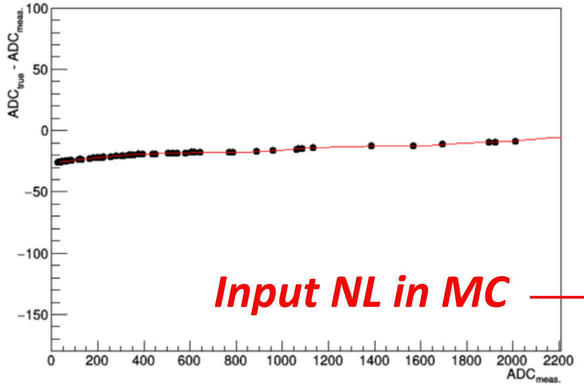


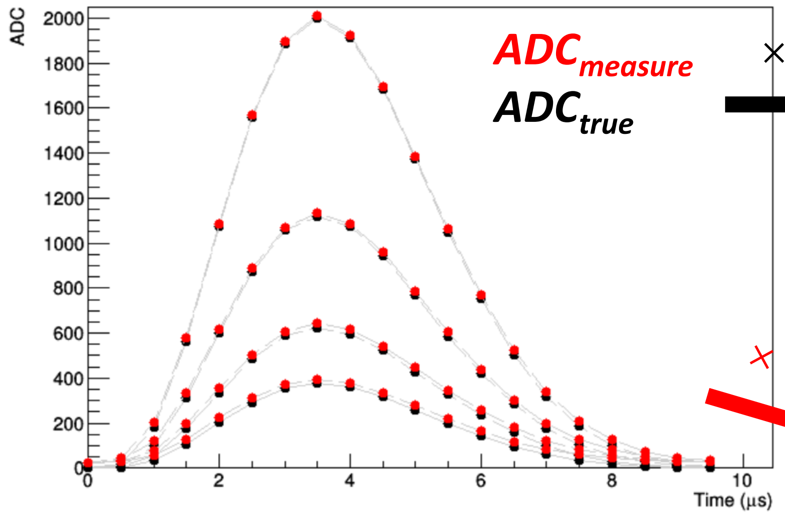


- Given a precise response function of the preamp, a NL measurement can be obtained
- However, low temperature change the response significantly

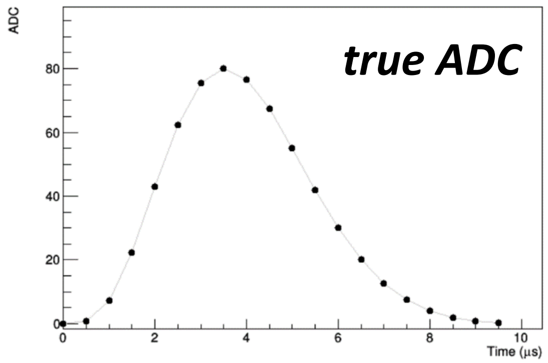
From a response function respective

- Assume pulse voltage (η) and preamp gain (G) do not change the shape of electronics response
- NL distorts the shape differently for high ADC and low ADC



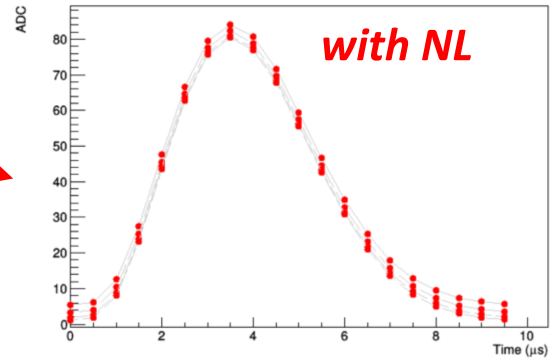


$\times\ 1/\ \eta G$



Waveforms match perfectly in shape

$\times\ 1/\ \eta G$



A spread in shapes

Calibration strategy

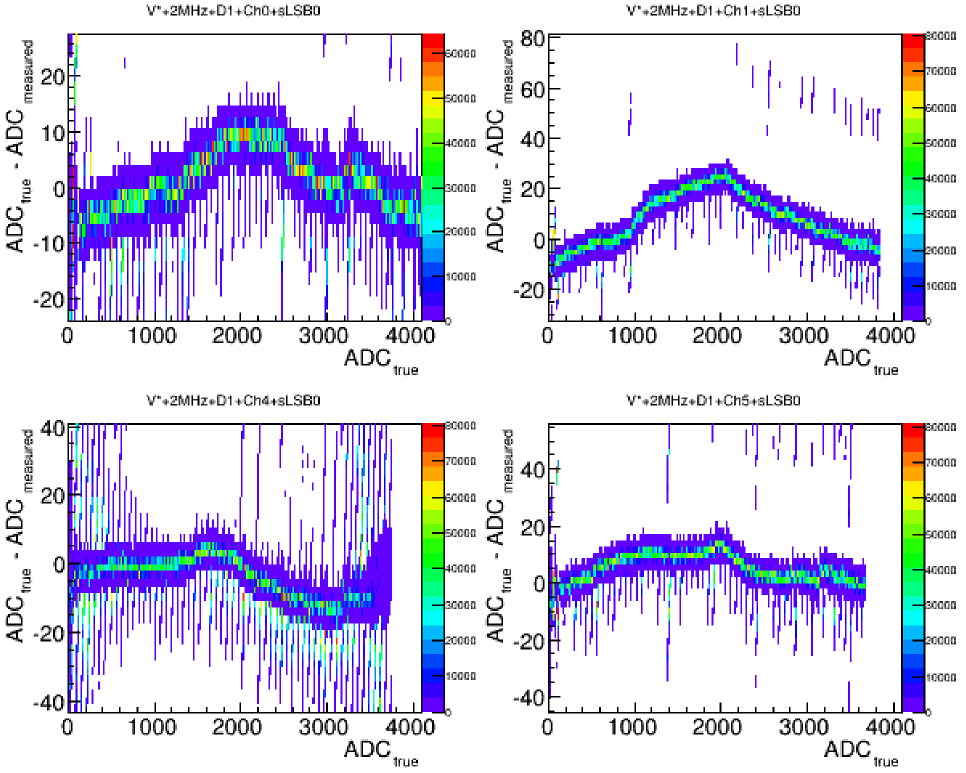
- Assume a function of nonlinearity correction
  - a piecewise function
  - a polynomial function
  - a function build from a 12-bit ADC model

- Minimize the variance in A(t)/ηG
  - i.e. the effective response function

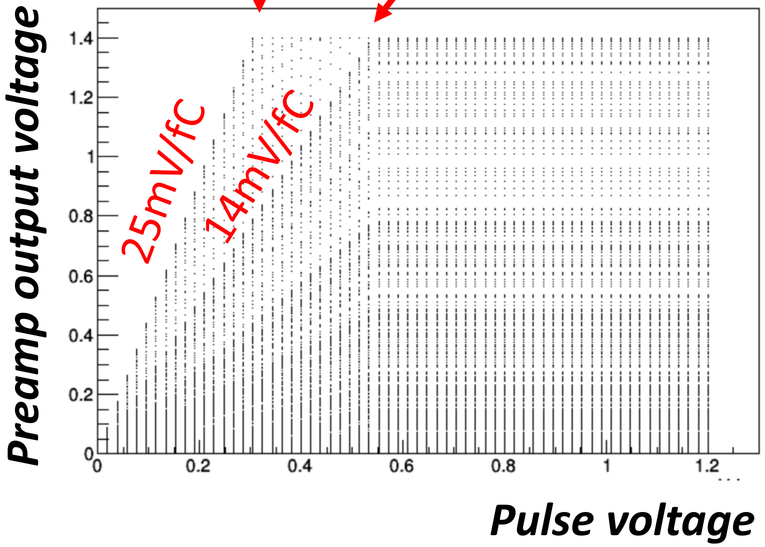
- ~O(10k) data points & ~O(10) unknowns
  → should be a solvable problem

- A channel by channel calibration plan

NL varies from channel to channel in the bench test

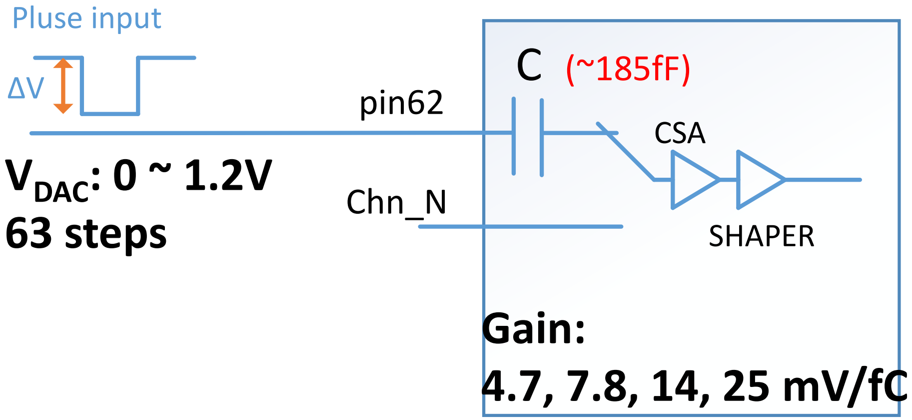


Proof of principle with a MC simulation



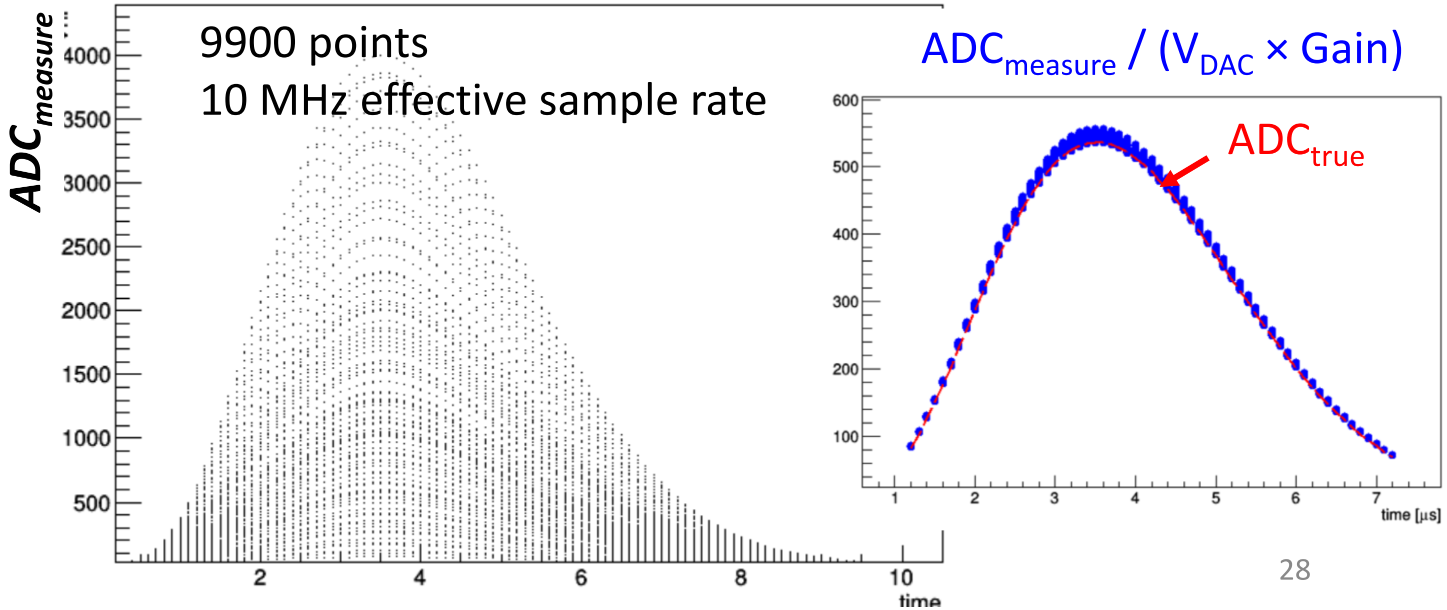
preamp output saturation

preamp input saturation



V_{DAC}: 0 ~ 1.2V
63 steps

Gain:
4.7, 7.8, 14, 25 mV/fC

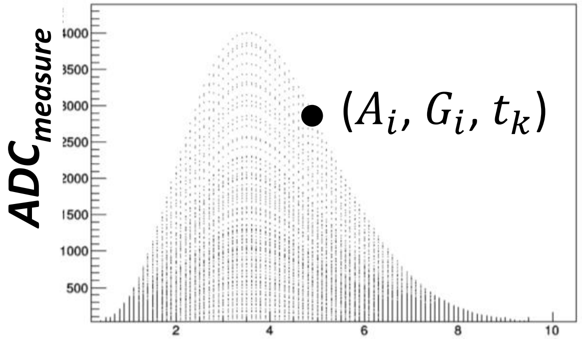


9900 points
10 MHz effective sample rate

$ADC_{measure} / (V_{DAC} \times Gain)$

- By ignoring some saturations in preamp, a 10k data set is possible

χ^2 minimization



$$\chi^{2(\alpha)} = \sum_i \left(A_i + f^{(\alpha)}(A_i) - R^{(\alpha-1)}(t_k)G_i\right)^2$$

index of the α-th iteration

G_i = pulse voltage × preamp gain
(A normalization of charge input)

Time tick for A_i

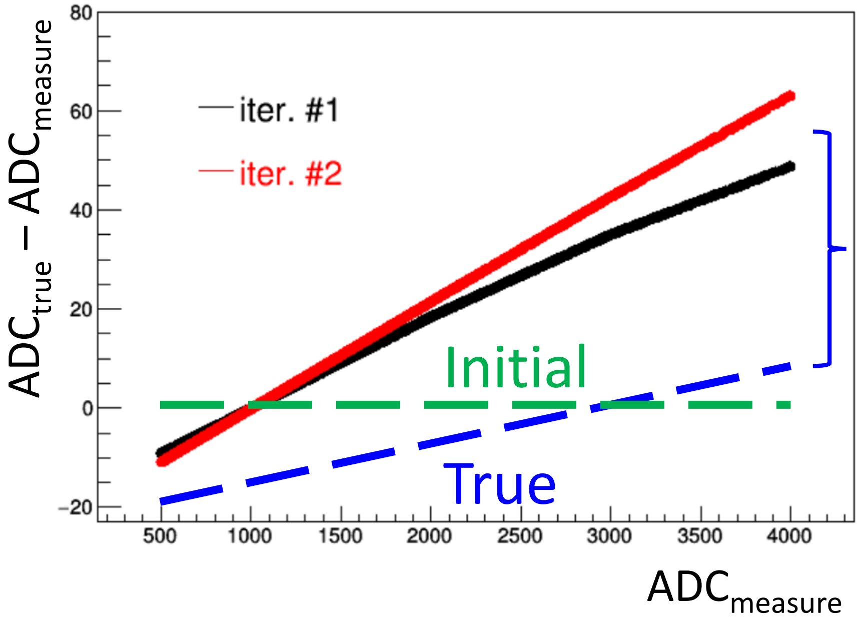
i-th data point

NL correction function
(To be fitted out)

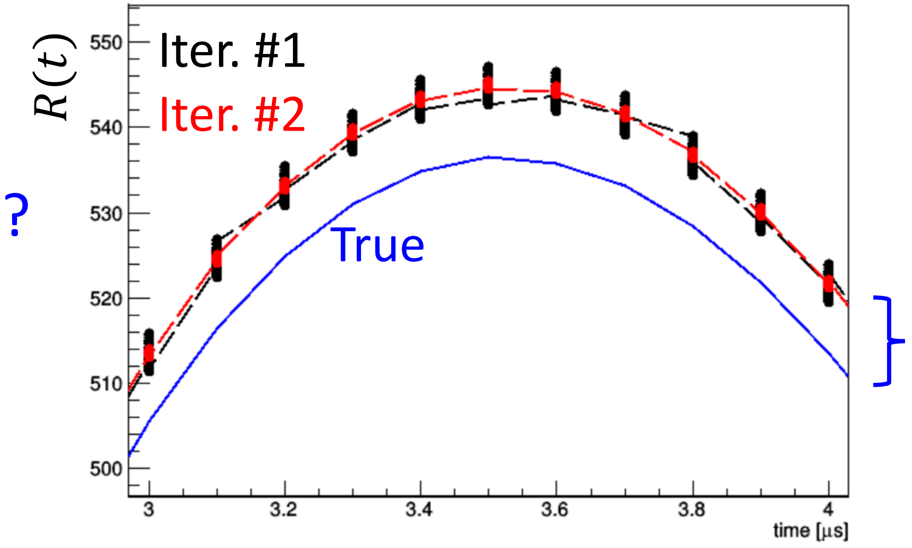
$R^{(\alpha-1)}(t_k) = \frac{1}{N}\sum \frac{A_i + f^{(\alpha-1)}(A_i)}{G_i}$ is the **effective response function**
(Calculated with the NL function from best fit of previous iteration)

“Best-fit” $f(A_i)$ and $R(t)$

- Given an initial value of NL correction function $f(A_i)$
- After a few iterations, “best-fit” NL $f(A_i)$ and effective response $R(t)$ tends to be stable
- The spread in $R(t)$ significantly shrinks after minimization



NL bias?



Electronics response bias ≈ 9

Degeneracy in NL and response function

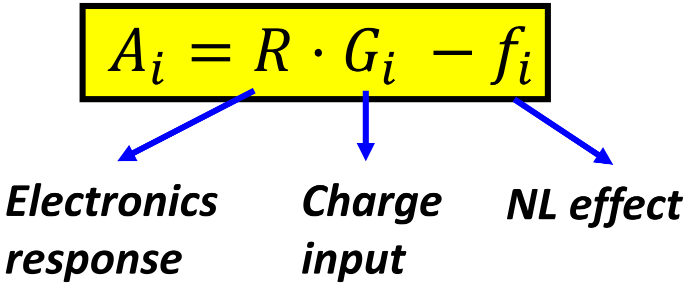
- Given different initial values, χ^2 minimization do not always converge to the true value
- Assume two sets of “best-fit” NL correction ***f(A)*** and ***F(A)***

best fit

Dataset	$\{A_i, G_i\}$	$\{A_i, G_i\}$
NL correction function f_i	$\boldsymbol{f}(\boldsymbol{A_i})$	$\boldsymbol{F}(\boldsymbol{A_i})$
Effective response function R(t)	$\frac{A_i + \boldsymbol{f}(\boldsymbol{A_i})}{G_i}$	$\frac{A_i + \boldsymbol{F}(\boldsymbol{A_i})}{G_i}$
ADC formation	$R \cdot G_i - f_i$	
ADC for charge G_i	A_i	A_i

- Two sets of NL & response function are equivalent in signal prediction and deconvolution

Signal formation



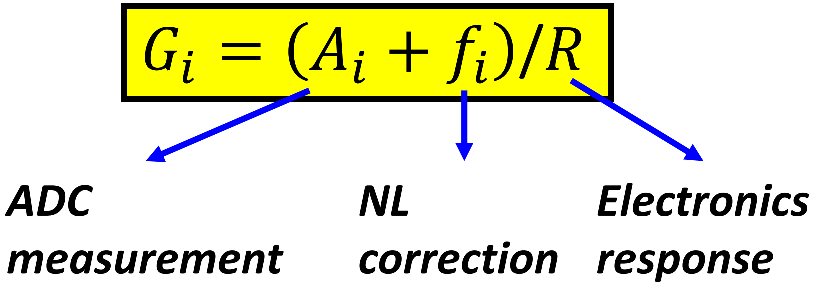
$$A_i = R \cdot G_i - f_i$$

Electronics response

Charge input

NL effect

Signal deconvolution



$$G_i = (A_i + f_i)/R$$

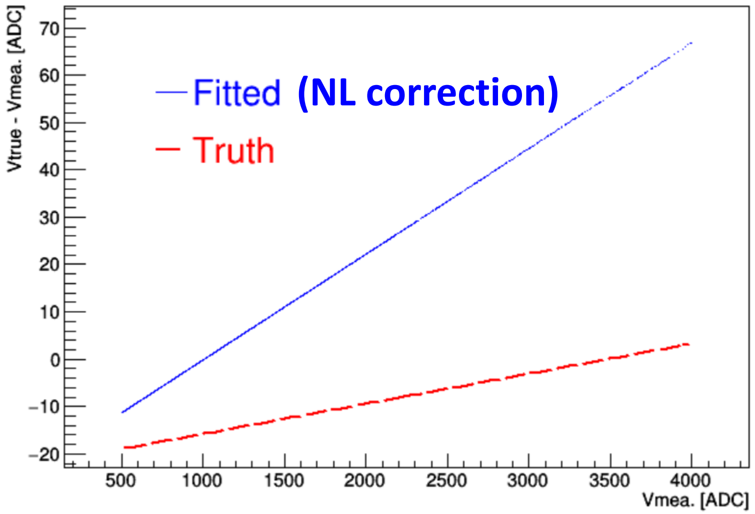
ADC measurement

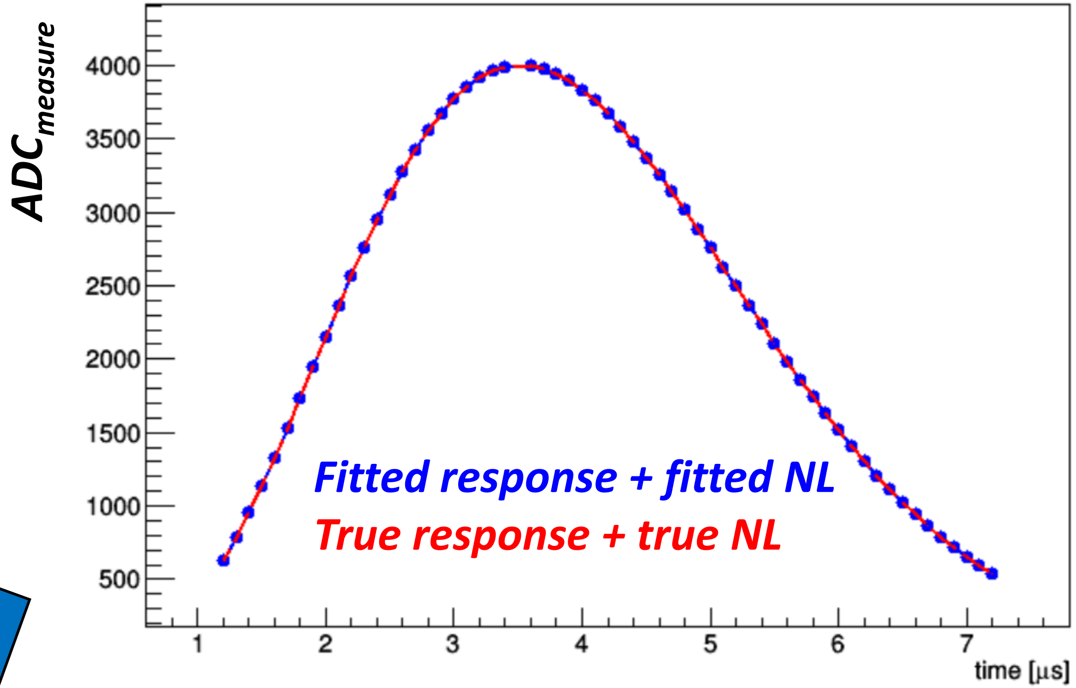
NL correction

Electronics response

MC validation of the degeneracy

- Given a same charge input, the waveform predictions are close (<1 ADC) for
  - True response and NL
  - A "best-fit" effective response and NL





NL bias in "best-fit" is not a problem!

Interim summary

- Principle of ADC nonlinearity (NL) calibration for protoDUNE was studied through a simplified Monte Carlo study
- With a series of well controlled pulses to the charge preamplifier, an **effective ADC NL** and an **effective electronics response** function of the preamplifier can be obtained
- The ionization charge can be accurately extracted given these two effective functions

Summary

- Cold electronics is crucial for LArTPC experiments

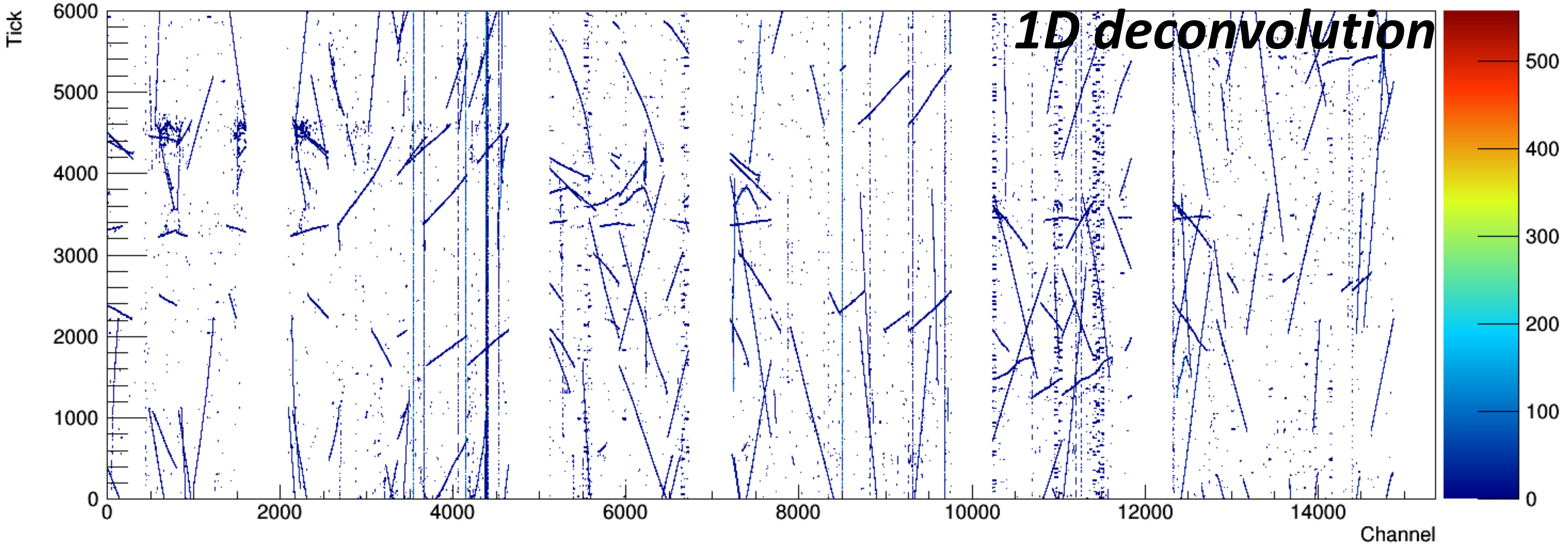
- The sticky code mitigation and ADC nonlinearity calibration are essential for a precise determination of TPC readout
  - Sticky code mitigation was preliminarily studied with protoDUNE data
  - ADC nonlinearity calibration was studied with a MC simulation

- For any downstream analysis that requires a precise extraction of ionized electrons (e.g., PID), such ADC calibration would be meaningful

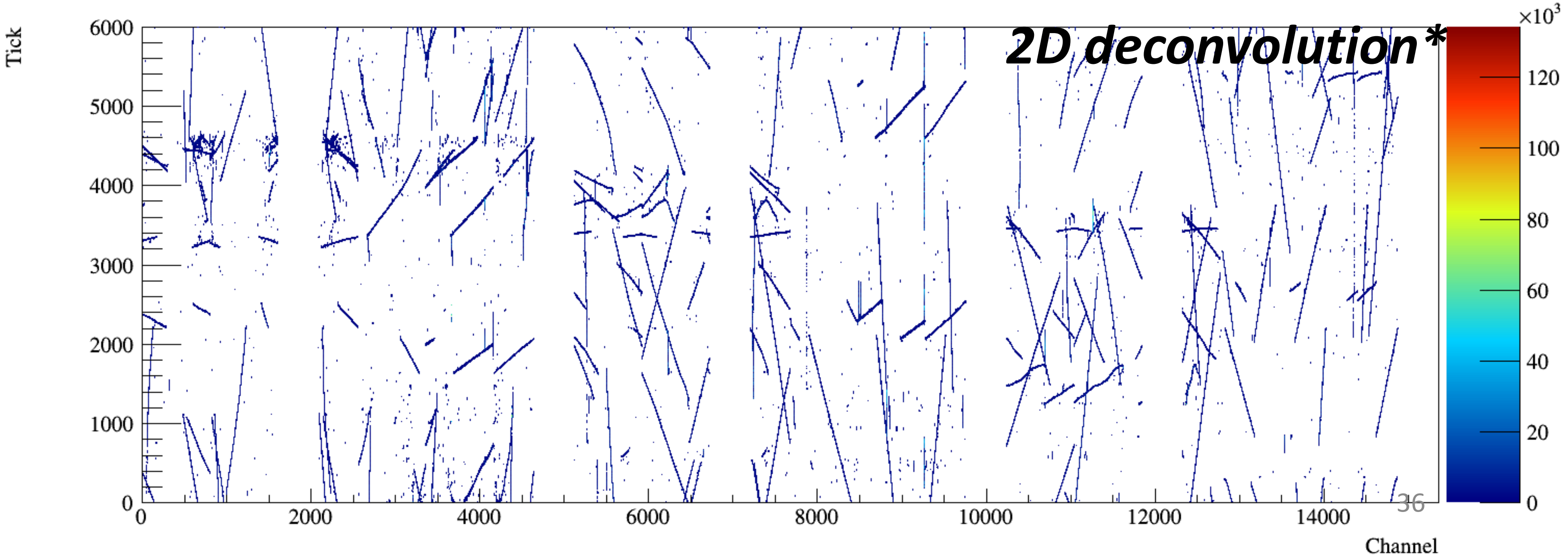
Wire-Cell signal processing in protoDUNE

(Figures to be included in Hanyu’s Wire-Cell signal processing talk)

SP Performance in protoDUNE beam data



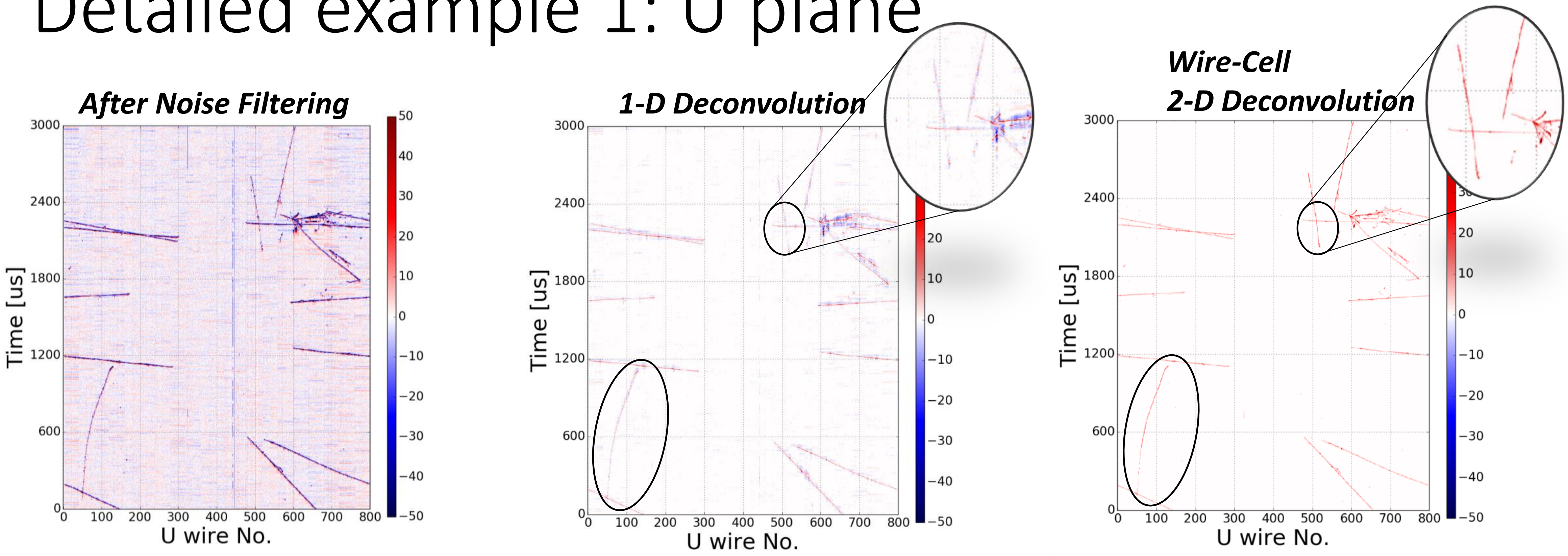
Run 5141, Event 23865
Threshold: 5
From the offline reco chain
(protoDUNE_reco_data.fcl)



Run 5141, Event 23865
Threshold: 3σ noise
Unit: # of electrons
From Wire-Cell toolkit

**: There is still room for improving the software filter and some thresholds, etc.*
***: Noise filtering has not been applied here for both 1D & 2D.*

Detailed example 1: U plane


After Noise Filtering

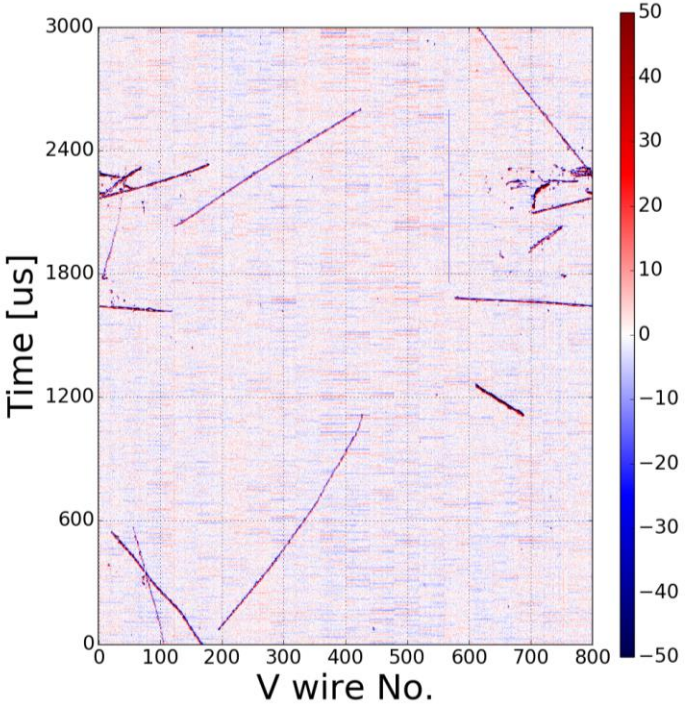
1-D Deconvolution

Wire-Cell 2-D Deconvolution

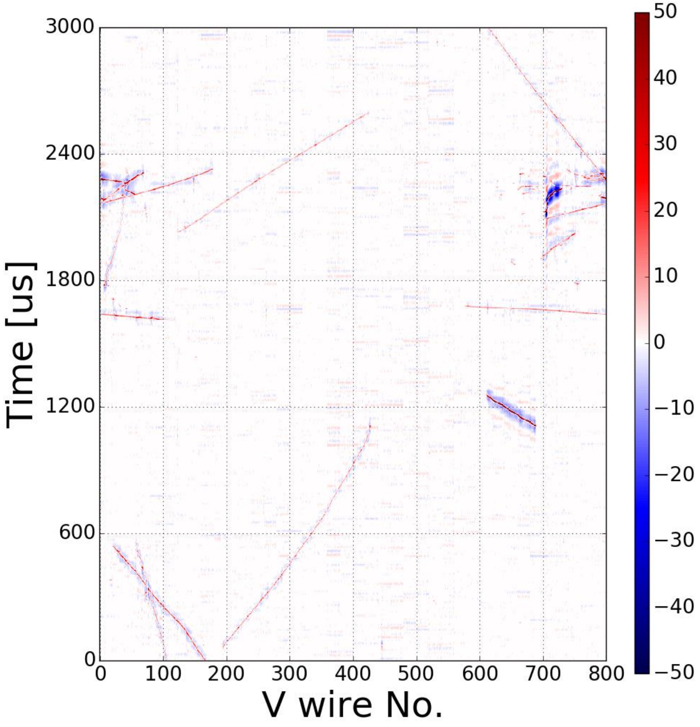
- Re-normalize 1D & 2D to the same scale
- No significant negative component after 2D deconvolution
- Long tracks (in time) are more visible in the 2D deconvolution

Example 2: V plane

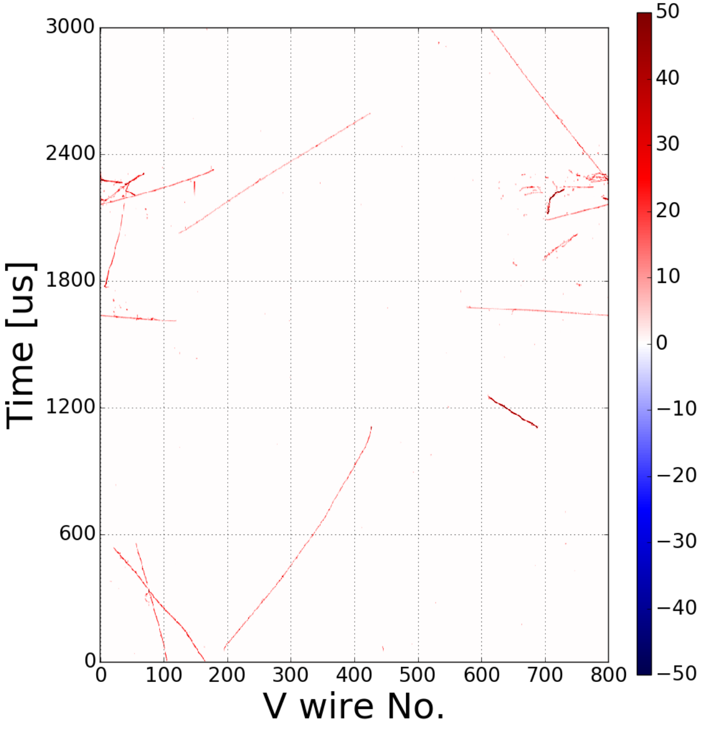
After Noise Filtering



1-D Deconvolution

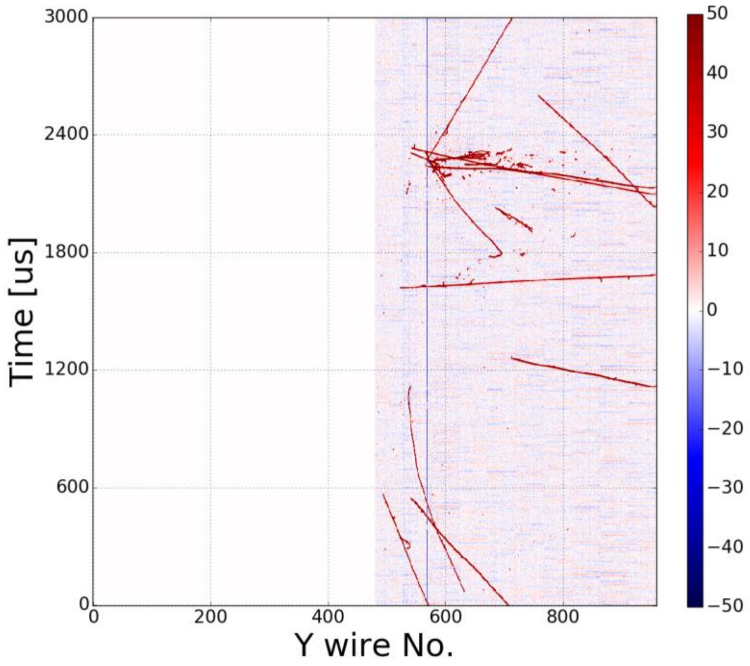


2-D Deconvolution

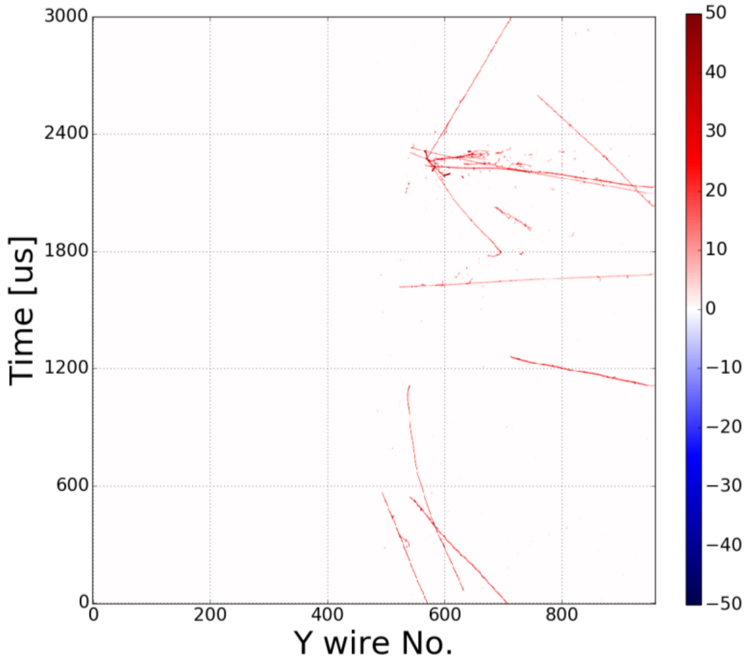


Example 3: W plane

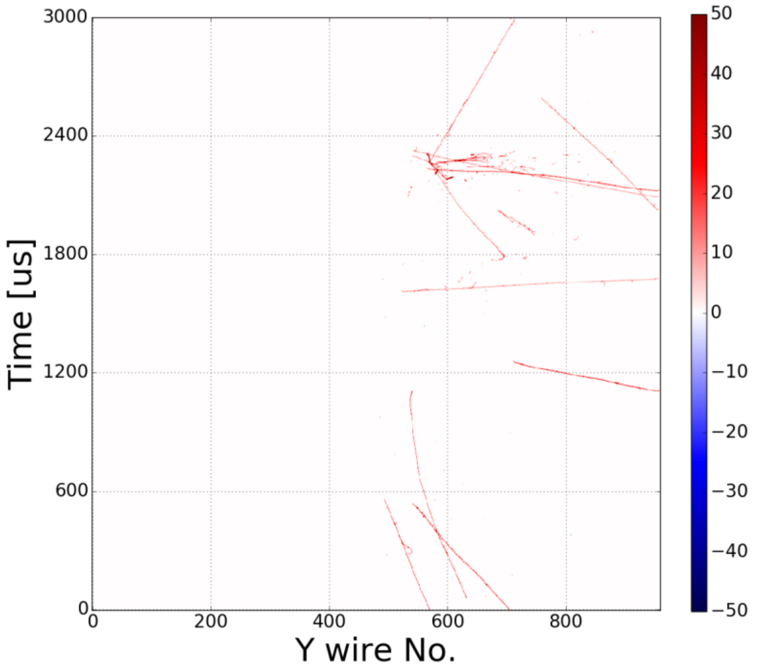
After Noise Filtering



1-D Deconvolution



2-D Deconvolution



- 1D & 2D deconvolution are consistent in collection plane