ECON ASICs

Jim Hirschauer

ASICs PMG

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Recent/Current activities

- May 14 : ECON mini-review with focus on transmitter choice (10G or 1.28G)

- June 19-21 : HGCAL workshop
    - Decide on ECON-T and ECON-D architectures (numbers of I/O)
    - FE/TPG working group presents full summary of TRG algo results to HGCAL

- Sep 2019 : Fully specific ECON-T trigger and ECON-D zero suppression algorithms

- Oct 22-24, 2019: DOE CD-1

May 14 review

- We presented proposal for "decentralized" system design that has **several benefits**:
  - isolates system complexity into single small "ECON board" and "transmitter board"; large multiplicity of board versions remains for passive motherboard.
  - uniform footprint/architecture for ECON-D and ECON-T
  - simpler and less expensive QFP package (instead of BGA package)
  - uses simpler 1.28G transmitters (instead of 10G)
- and **one disadvantage** : more 10-25% more links
- Report is here :
  https://indico.cern.ch/event/808629/attachments/1853690/3044864/ECON_Design_Review_Recommendations_Summary.pdf

- Report highlights:

Removing 10G outputs and replacing multiple 1.28G outputs: This is fully supported and recommended by all reviewers.

Decentralized architecture : This is considered another important simplification step from an engineering perspective. It remains to be accepted by the collaboration as it impacts other areas of the project.

Verification : It is essential to achieve "first time silicon success". The verification process is key to achieving this and can dominate the overall design time. It must not be underestimated.

Schedule: The new schedule [**Submit MPWs in Mar/Apr 2020, final chips in Jan 2021**] respects the HGCal project overall schedule. However, the ECON ASIC remains critical path. It is very important to maintain momentum and human resource allocation to the ECON design and verification process.

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ECON status, progress, schedule

- Ralph and Gregory have developed matrix of activities with estimate of effort for each:
  - 144 person-weeks for ECON-T + 46 person-weeks for ECON-D
- 62 person-weeks of verification is only 33% of effort - much lower than 70% "rule of thumb"
  - Doubling verification would make it 50% of 250 person-week effort

	Definition of architecture	Study architecture and concensus	Block specification done 90%	Block RTL Implemented	Block testbench 90% implemented	Block Simulation 90% done, self checking	Block synthesis done	DFT method defined	DFT method implemented and tested	Triplication Method defined	Triplication in RTL complete	RTL Integration with Econ_t 90% done	Pinout List Complete / Interface compatability	Analog block layout complete	Block level Spice and SDF simulation	Block Formal Verification netlist to RTL done	Block PD 70% done	Top level UVM DV plan for block done	Top level UVM testbench 90% implemented	Top level UVM DV plan execution	Block level PD 100%	Pinout Layout Complete	Floorplan 100%	Top level PD 100% done	
Eport Rx	0	0		0	0	1	0.5			0.5	1	0.5		1	1	0.1	2	3	4	2	3	0.5	1	0	21.1
Aligner								1	1	0.5	1					0.3	0.5	2	2	1	1	0.2	0.2	0	10.7
Data Mux										0.5	0.5	1			0.1	0.1	0.2	1	1	1	0.2		0.2	0	5.8
Fast Command							0.2			0.1	0.5					0.1	0.2	1	1	1	0.2	0.1		0	4.4
Error Handling	1	2	0.5	1	2	1	0.2			0.2	0.5	0.2	0.1		0.1	0.1	0.5	2	4	1	0.2	0.1		0	16.7
I2C				1	2	1	0.2			0.5	1	0.2			0.1	0.1	1	2	1	1	0.2	0.1	0.5	0	11.9
Efuse	0.5	0.5	0.5		2	1						1	0.5		0.5	0.1	1	1	1	1	0.2	0.1	0.5	0	11.4
PLL Calibration / EPortRX training	0.2	0.2	0.1													1			1	0.2				0	2.7
1.28 Tx Gbps digital, scrambler / transmission encoding	1	1										0.5			0.5	0.5	0.5	0.1	0.1	1	0.2	0.1	0.5	0	6
1.28 Tx Gbps analog	1	1	1											1	1	0.1	0.5	0.1		1	0.1	0.1	0.5	0	7.4
Trigger Buffer Management SM	unk	unk	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Latency Control Management SM	unk	unk	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Trigger Algorithm	unk	unk	1	2	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	11.2
Top Level	unk	unk					2	2	3	1	2					2	2				2		0.2	1	17.2
	3.7	4.7	3.5	5	10.5	7	3.7	3	4	3.3	6.5	4	0.6	2	3.3	4.8	9.9	16.7	19.6	13.2	8.8	1.3	4.2	1	144

ECON effort

- Four scenarios based on required and available effort:
  A. 190 person-weeks required / 4.2 person-years available : OK
  B. 190/3.5 : Tight but feasible
  C. 250/4.2 : ECON delays system test and production
  D. 250/3.5 : ECON delays system test and production

- Scenario A presented on May 14, and deemed barely feasible.
  - Recommendation to accelerate w.r.t. Scenario A

	Worse Case	Best Case
Ralph	1	1
Mike (ANL)	0.6	0.6
Gregory	0.4	0.4
Alpana	0.4	0.4
Sandeep	0.5	0.8
Jim Hoff	0.5	1
Total	3.4	4.2
ECON duration (190 p-wks)	56 weeks	45 weeks
ECON duration (250 p-wks)	74 weeks	60 weeks