ECON ASICs

Jim Hirschauer

ASICs PMG

8 July 2019

Recent/Current activities

- May 14 ECON mini-review : removed 10G link from ECON

- June 19-21 : HGCAL workshop
    - Discussed all aspects of ECON-T and ECON-D architectures (numbers of I/O)
    - FE/TPG working group presented full summary of TRG algo results

- July 9 : Final meeting on ECON architecture
    - Will show final latency and link count with optimized data format and use of 16-bit words
    - Expecting selection of decentralized architecture with NO extra 640 Mbps transmitter.

- Sep 2019 : fully specify ECON TRG algorithm(s):
    - Gregory/JH discussed plan to make programmable choice between
        - variable-format / variable-size "threshold" algorithm
        - fixed-format / fixed-size "super trigger cell" algorithm
    - Design team should proceed assuming programmable choice with "threshold" algorithm as priority.

- Oct 22-24, 2019: DOE CD-1

Jonathan Lewis's June 12 minutes following June 11 ASICs PMG:

1 **Dune** Work is proceeding on debugging the auto-calibration section of the ColdADC. This is occupying a most of Jim Hoff's time currently. We expected to have him transitioned to ECON by now. Given the problems with the chip, the project wants another turn in the fall in order to have chips for an integration test of a motherboard prototype. The amplifier rail voltage issue prevents the current prototype from being used. Fixing the other issues would clearly be advantageous. Carl Grace from LBNL will be at Fermilab next week. It is expected that working together, Carl and Jim should be able to debug the calibration issue. Approximately 6 person-weeks of Jim and Sandeep will be required in the fall for the submission of the next chip. The other task for Jim to complete is writing documentation. Dave is going to review the current documentation and work with Jim to insure that docs are completed in a timely way with a goal of making them just good enough to design motherboards.

2 **ECON** was substantially replanned at the CERN workshop. The ECON-T and ECON-D will have similar footprints with only 12 inputs and 12 outputs. All will be 1.28 Gbps. Jim showed the updated work plan. It requires 144 FTE-weeks for ECON-T and 46 weeks for ECON-D. That includes an integrated 62 weeks for verification. That total is seen as low. Jim's best-case scenario using the available staff would barely make it to the March 2020 submission date required by the CMS schedule. That assumes no distractions or pitfalls. Verification is an OO coding task, so it is a ripe area for adding other support.

It was clear to all, that ECON cannot succeed without an infusion of labor. Therefore, the following actions will be taken

1 Jim Hoff will complete ColdADC as outlined above in 2 weeks and transition to ECON full time. Along with other work, he will start to setup the verification framework.
2 Within ~2 weeks, Davide will move to share time between ECON and QIS, with at least 50% of time going to ECON. Work on his LDRD may need to be postponed.
3 Jim Hirschauer will talk to Liz S-K and Jim Amundson about possible OO programming from SCD help for verification. (Using postdocs was discussed and deemed not to be advisable given the aggressive schedule.)
4 Gregory and Terri will work to integrate engineers from the front-end group wherever possible (e.g. C. Gingu) to write Verilog and perform related tasks.
5 Gregory and Gary will work to re-integrate Farah into the revamped project
6 We will continue to look for outside partners. However, that is increasingly looking like a dry hole.
7 We will bring in a UVM consultant for training. Verification for the Dune chips is thought to have been overkill. A consultant will help better target work for ECON.

The DUNE and ECON chips are the highest priorities for the department. If necessary other activities, e.g. QIS will be scaled back to free staff to work on them.

The labor needed for the submission of the revised ColdADC clearly will interfere with ECON progress. The timing of that is sufficiently uncertain, that we agreed to defer discussion of that schedule and its impacts to a later date (after August 5).

Please let me know if you have any questions on or corrections to these minutes.

JH homework

- Arrange **meeting with SCD** for bringing software expert into ASIC verification effort.
  - Made initial contact
  - Liz/JimA have a person in mind.
  - JH was at CERN, then Liz away (still) -- will try to hold meeting week of Jul 22-26 when it's feasible for all.

- ECON-T **working document**:
  - Gregory and JH made good progress last week finalizing data format and latency control
  - First draft will be released this week

ECON status, progress, schedule

- Ralph and Gregory have developed matrix of activities with estimate of effort for each:
  - 144 person-weeks for ECON-T + 46 person-weeks for ECON-D
- 62 person-weeks of verification is only 33% of effort - much lower than 70% "rule of thumb"
  - Doubling verification would make it 50% of 250 person-week effort

	Definition of architecture	Study architecture and concensus	Block specification done 90%	Block RTL Implemented	Block testbench 90% implemented	Block Simulation 90% done, self checking	Block synthesis done	DFT method defined	DFT method implemented and tested	Triplication Method defined	Triplication in RTL complete	RTL Integration with Econ_t 90% done	Pinout List Complete / Interface compatability	Analog block layout complete	Block level Spice and SDF simulation	Block Formal Verification netlist to RTL done	Block PD 70% done	Top level UVM DV plan for block done	Top level UVM testbench 90% implemented	Top level UVM DV plan execution	Block level PD 100%	Pinout Layout Complete	Floorplan 100%	Top level PD 100% done	
Eport Rx	0	0		0	0	1	0.5			0.5	1	0.5		1	1	0.1	2	3	4	2	3	0.5	1	0	21.1
Aligner								1	1	0.5	1					0.3	0.5	2	2	1	1	0.2	0.2	0	10.7
Data Mux										0.5	0.5	1			0.1	0.1	0.2	1	1	1	0.2		0.2	0	5.8
Fast Command							0.2			0.1	0.5					0.1	0.2	1	1	1	0.2	0.1		0	4.4
Error Handling	1	2	0.5	1	2	1	0.2			0.2	0.5	0.2	0.1		0.1	0.1	0.5	2	4	1	0.2	0.1		0	16.7
I2C				1	2	1	0.2			0.5	1	0.2			0.1	0.1	1	2	1	1	0.2	0.1	0.5	0	11.9
Efuse	0.5	0.5	0.5		2	1						1	0.5		0.5	0.1	1	1	1	1	0.2	0.1	0.5	0	11.4
PLL Calibration / EPortRX training	0.2	0.2	0.1													1			1	0.2				0	2.7
1.28 Tx Gbps digital, scrambler / transmission encoding	1	1										0.5			0.5	0.5	0.5	0.1	0.1	1	0.2	0.1	0.5	0	6
1.28 Tx Gbps analog	1	1	1											1	1	0.1	0.5	0.1		1	0.1	0.1	0.5	0	7.4
Trigger Buffer Management SM	unk	unk	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Latency Control Management SM	unk	unk	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Trigger Algorithm	unk	unk	1	2	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	11.2
Top Level	unk	unk					2	2	3	1	2					2	2				2		0.2	1	17.2
	3.7	4.7	3.5	5	10.5	7	3.7	3	4	3.3	6.5	4	0.6	2	3.3	4.8	9.9	16.7	19.6	13.2	8.8	1.3	4.2	1	144

Reference info

ECON status, progress, schedule

- No update on status matrix for this meeting, but will have one next meeting:

	Definition of architecture	Study architecture and concensus	Block specification done 90%	Block RTL Implemented	Block testbench 90% implemented	Block Simulation 90% done, self checking	Block synthesis done	DFT method defined	DFT method implemented and tested	Triplication Method defined	Triplication in RTL complete	RTL Integration with Econ_t 90% done	Pinout List Complete / Interface compatability	Analog block layout complete	Block level Spice and SDF simulation	Block Formal Verification netlist to RTL done	Block PD 70% done	Top level UVM DV plan for block done	Top level UVM testbench 90% implemented	Top level UVM DV plan execution	Block level PD 100%	Pinout Layout Complete	Floorplan 100%	Top level PD 100% done	
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Aligner								1	1	0.5	1					0.3	0.5	2	2	1	1	0.2	0.2	0	10.7
Data Mux										0.5	0.5	1			0.1	0.1	0.2	1	1	1	0.2		0.2	0	5.8
Fast Command							0.2			0.1	0.5					0.1	0.2	1	1	1	0.2	0.1		0	4.4
Error Handling	1	2	0.5	1	2	1	0.2			0.2	0.5	0.2	0.1		0.1	0.1	0.5	2	4	1	0.2	0.1		0	16.7
I2C				1	2	1	0.2			0.5	1	0.2			0.1	0.1	1	2	1	1	0.2	0.1	0.5	0	11.9
Efuse	0.5	0.5	0.5		2	1						1	0.5		0.5	0.1	1	1	1	1	0.2	0.1	0.5	0	11.4
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1.28 Tx Gbps digital, scrambler / transmission encoding	1	1										0.5			0.5	0.5	0.5	0.1	0.1	1	0.2	0.1	0.5	0	6
1.28 Tx Gbps analog	1	1	1											1	1	0.1	0.5	0.1		1	0.1	0.1	0.5	0	7.4
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Top Level	unk	unk					2	2	3	1	2					2	2				2		0.2	1	17.2
	3.7	4.7	3.5	5	10.5	7	3.7	3	4	3.3	6.5	4	0.6	2	3.3	4.8	9.9	16.7	19.6	13.2	8.8	1.3	4.2	1	144

ECON effort update based on JDL minutes

	JH Worse Case [FTE]	JH Best Case [FTE]	JDL plan [FTE]	JDL [FTE-yr in FY20]
Ralph	1	1	1	0.75
Mike (ANL)	0.6	0.6	0.6	0.45
Gregory	0.4	0.4	0.4	0.3
Alpana	0.4	0.4	0.4	0.3
Sandeep	0.5	0.8	0.8	0.6
Jim Hoff	0.5	1	1	0.75
Davide	0	0	0.5	0.38
Farah	0	0	0.5	0.38
Total	3.4	4.2	5.2	3.9
ECON duration (190 p-wks)	56 weeks	45 weeks	37 weeks	
ECON duration (250 p-wks)	74 weeks	60 weeks	48 weeks	

ECON effort

- Four scenarios based on required and available effort:
  A. 190 person-weeks required / 4.2 person-years available : OK
  B. 190/3.5 : Tight but feasible
  C. 250/4.2 : ECON delays system test and production
  D. 250/3.5 : ECON delays system test and production

- Scenario A presented on May 14, and deemed barely feasible.
  - Recommendation to accelerate w.r.t. Scenario A

	Worse Case	Best Case
Ralph	1	1
Mike (ANL)	0.6	0.6
Gregory	0.4	0.4
Alpana	0.4	0.4
Sandeep	0.5	0.8
Jim Hoff	0.5	1
Total	3.4	4.2
ECON duration (190 p-wks)	56 weeks	45 weeks
ECON duration (250 p-wks)	74 weeks	60 weeks