ECON ASICs

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ASICs PMG

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JH/CMS homework

- July 9 CMS meeting on **ECON architecture : CMS finalized choices** of
  - Uniform simplified architecture for ECON-T and ECON-D
    - 12x 1.28 Gbps, 14x 1.28 Gbps output, 0x 640 Mbps outputs
  - Threshold algorithm as default ECON-T configuration
    - ECON-T will also be programmable to allow fixed format / latency TRG algo, which will be fully specified at CMS week Sep 23-27.

- Arrange **meeting with SCD** for bringing software expert into ASIC verification effort.
  - Hirschauer, Deptuch, Hoff met with Liz+JimA on July 25
    - Hoff gave nice presentation on System Verilog, UVM, Fermilab ASIC group, ECON ASIC, etc. -- made it clear that UVM skills would be useful for foreseeable future.
    - Liz+JimA are understanding how to reorganize to free 50-100% of one person.

- ECON-T **working document**:
  - Hirschauer released first draft on July 12 to CMS and ECON team
    - ECON-T data format finalized
    - Latency control finalized

Output data format from working doc

- Full specification of ECON-T output data format
  - based on iterative process with design team
  - Uses "1/2 word" special optimization to minimize latency for jets in low occupancy regions
  - latency determined with full CMSSW simulation

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8. Output data format

The data format for the threshold algorithm depends on the number of TC selected as described below. The packet from each BX is padded to make 16-bit words.

Table 1 — Data common to all data types.

	Description	Bits	Use
1	Header	5	Incrementing 0-31, send 31 at BC0 and restart increment
2	Data type	2-3	0 TC, 1-7 TC, 8-48 TC, truncated 1-word, truncated 2-word
3	Module sum	8	Sum of charge in all channels
4	Extra bit	0-1	Extra bit available only for data types 00, 01, 10.

Table 2 — Data types. Truncated data types beginning with "11" have additional bit to indicate level of truncation.

Code	Description
00	0 TC
01	Low occupancy : [1, 7] TC
10	High occupancy : [8,48] TC
110	Truncated 1-word (module sum)
111	Truncated 2-word (3x 1/3-module sum)

Table 3 — data sent for low occupancy data type

	Description	Bits	Comments
1	Number of channels sent	3	
2	Addresses	6b * NTC	
3	Charge data	7b * NTC	

Number of TC	Data type	Header	Data type	Module sum	Extra bit	Number of channels	Address or Map	Charge data	Padding	Total bits	16b words
0	Trunc 1w	5	3	8	0	0	0	0	0	16	1
0	Trunc 2w	5	3	24	0	0	0	0	0	32	2
0	0 TC	5	2	8	1	0	0	0	0	16	1
1	Low occ	5	2	8	1	3	6	7	0	32	2
2	Low occ	5	2	8	1	3	12	14	3	48	3
3	Low occ	5	2	8	1	3	18	21	6	64	4
4	Low occ	5	2	8	1	3	24	28	9	80	5
5	Low occ	5	2	8	1	3	30	35	12	96	6
6	Low occ	5	2	8	1	3	36	42	15	112	7
7	Low occ	5	2	8	1	3	42	49	2	112	7
8	High occ	5	2	8	1	0	48	56	8	128	8
9	High occ	5	2	8	1	0	48	63	1	128	8
10	High occ	5	2	8	1	0	48	70	10	144	9
11	High occ	5	2	8	1	0	48	77	3	144	9
12	High occ	5	2	8	1	0	48	84	12	160	10
13	High occ	5	2	8	1	0	48	91	5	160	10
14	High occ	5	2	8	1	0	48	98	14	176	11
15	High occ	5	2	8	1	0	48	105	7	176	11
16	High occ	5	2	8	1	0	48	112	0	176	11
17	High occ	5	2	8	1	0	48	119	9	192	12
18	High occ	5	2	8	1	0	48	126	2	192	12
19	High occ	5	2	8	1	0	48	133	11	208	13
20	High occ	5	2	8	1	0	48	140	4	208	13
21	High occ	5	2	8	1	0	48	147	13	224	14
22	High occ	5	2	8	1	0	48	154	6	224	14
23	High occ	5	2	8	1	0	48	161	15	240	15
24	High occ	5	2	8	1	0	48	168	8	240	15
25	High occ	5	2	8	1	0	48	175	1	240	15
26	High occ	5	2	8	1	0	48	182	10	256	16
27	High occ	5	2	8	1	0	48	189	3	256	16
28	High occ	5	2	8	1	0	48	196	12	272	17
29	High occ	5	2	8	1	0	48	203	5	272	17
30	High occ	5	2	8	1	0	48	210	14	288	18
31	High occ	5	2	8	1	0	48	217	7	288	18
32	High occ	5	2	8	1	0	48	224	0	288	18
33	High occ	5	2	8	1	0	48	231	9	304	19
34	High occ	5	2	8	1	0	48	238	2	304	19
35	High occ	5	2	8	1	0	48	245	11	320	20
36	High occ	5	2	8	1	0	48	252	4	320	20
37	High occ	5	2	8	1	0	48	259	13	336	21
38	High occ	5	2	8	1	0	48	266	6	336	21
39	High occ	5	2	8	1	0	48	273	15	352	22
40	High occ	5	2	8	1	0	48	280	8	352	22
41	High occ	5	2	8	1	0	48	287	1	352	22
42	High occ	5	2	8	1	0	48	294	10	368	23
43	High occ	5	2	8	1	0	48	301	3	368	23
44	High occ	5	2	8	1	0	48	308	12	384	24
45	High occ	5	2	8	1	0	48	315	5	384	24
46	High occ	5	2	8	1	0	48	322	14	400	25
47	High occ	5	2	8	1	0	48	329	7	400	25
48	High occ	5	2	8	1	0	48	336	0	400	25

Latency control from working doc

- Concise but precise (beyond narrative) summary based on iterative process with design team and CMS

7. Output buffer and readout latency control

ECON manages its output buffer to provide well defined maximum readout latency. The maximum readout latency is programmable.

Output buffer depth is 840 words deep, and each word is 16b wide. The number 840 is the product of the maximum possible readout latency (30 BX), the maximum number of elinks (14), and the number of 16b words per BX per elink: 840 words = (30 BX) * (14 max elinks) * (2 words / BX / elink). With two output elinks active and programmed for 12 BX max latency, ECON would use only 24 words of this this 840-word buffer.

For each BX, ECON computes three data types:

- **Module Sum :** 5b header + 3b data type + 8b sum of charge from TCs in entire module
- **1/3-Module Sums :** 5b header + 3b data type + 3x (8b sum of charge from TCs in 1/3 of the module)
- **Full data :** nominal format described below

ECON buffer state machine monitors

- **Nbuf** = number of 16b words in buffer
- **NBX0** = number of 16b words in "full data" packet for current BX

State machine selects 1 of 3 data types for transmission for each BX depending on which of three exclusive conditions is satisfied. Conditions depend on programmable parameters T1 and T2 (both in units of numbers of 16b words). The data type associated with each condition is programmable. The conditions are:

- **Condition 1 :** (Nbuf + NBX0) > T2
- **Condition 2 :** [(Nbuf + NBX0) <= T2] and [Nbuf > T1]
- **Condition 3 :** [(Nbuf + NBX0) <= T2] and [Nbuf <= T1]

The first condition is the primary method of latency control. We expect to operate with T2 set such that the maximum readout latency is 12 BX; the T2 value therefore depends on the number of active elinks. The truncated packets are 1 or 2 16b words, so they always fit into the buffer which drains at a minimum rate of 32bits/BX for a single elink.

Recent activities

- ~Twice weekly technical design team meetings since last PMG
  - Hirschauer presented ECON-T working doc
  - DFT / scan chain methodology
  - triplication method
  - Plan and progress on taking Word Aligner block through the full RTL ➔ physical design chain to test tools.

- Independent review/consultation on Universal Verification Methodology / System Verilog
  - Aug 5-9 : final report from consultant this afternoon.

July 8 ECON status

	Definition of architecture	Study architecture and consensus	Block specification done 90%	Block RTL Implemented	Block testbench 90% implemented	Block Simulation 90% done, self checking	Block synthesis done	DFT method defined	DFT method implemented and tested	Triplication Method defined	Triplication in RTL complete	RTL Integration with Econ_t 90% done	Pinout List Complete / Interface compatability	Analog block layout complete	Block level Spice and SDF simulation	Block Formal Verification netlist to RTL done	Block PD 70% done	Top level UVM DV plan for block done	Top level UVM testbench 90% implemented	Top level UVM DV plan execution	Block level PD 100%	Pinout Layout Complete	Floorplan 100%	Top level PD 100% done	
Eport Rx							0.5			0.5	1	0.5		1	1	0.1	2	3	4	2	3	0.5	1	0	20.1
Aligner								1	1	0.5	1					0.3	0.5	2	2	1	1	0.2	0.2	0	10.7
Data Mux										0.5	0.5	1			0.1	0.1	0.2	1	1	1	0.2		0.2	0	5.8
Fast Command							0.2			0.1	0.5					0.1	0.2	1	1	1	0.2	0.1		0	4.4
Error Handling	1	2	0.5	1	2	1	0.2			0.2	0.5	0.2	0.1		0.1	0.1	0.5	2	4	1	0.2	0.1		0	16.7
I2C				1	2	1	0.2			0.5	1	0.2			0.1	0.1	1	2	1	1	0.2	0.1	0.5	0	11.9
Efuse	0.5	0.5	0.5		2	1						1	0.5		0.5	0.1	1	1	1	1	0.2	0.1	0.5	0	11.4
PLL Calibration / EPortRX training	0.2	0.2	0.1													1			1	0.2				0	2.7
1.28 Tx Gbps digital	1	1										0.5			0.5	0.5	0.5	0.1	0.1	1	0.2	0.1	0.5	0	6
1.28 Tx Gbps analog / full custom	1	1	1											1	1	0.1	0.5	0.1		1	0.1	0.1	0.5	0	7.4
Latency Control Management	0	0	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Trigger Algorithm	0	0	1	2	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	11.2
Top Level	0	0					2	2	3	1	2					2	2				2		0.2	1	17.2
System Level	0	0																							0
	3.7	4.7	3.3	4.5	9	5	3.5	3	4	3.3	6.5	3.8	0.6	2	3.3	4.7	9.4	15.2	18.1	12.2	8.3	1.3	4	1	134

Aug 9 ECON status

	Definition of architecture	Study architecture and consensus	Block specification done 90%	Block RTL Implemented	Block testbench 90% implemented	Block Simulation 90% done, self checking	Block synthesis done	DFT method defined	DFT method implemented and tested	Triplication Method defined	Triplication in RTL complete	RTL Integration with Econ_t 90% done	Pinout List Complete / Interface compatability	Analog block layout complete	Block level Spice and SDF simulation	Block Formal Verification netlist to RTL done	Block PD 70% done	Top level UVM DV plan for block done	Top level UVM testbench 90% implemented	Top level UVM DV plan execution	Block level PD 100%	Pinout Layout Complete	Floorplan 100%	Top level PD 100% done	
Eport Rx							0.5			0.5	1	0.5		1	1	0.1	2	3	4	2	3	0.5	1	0	20.1
Aligner								1	1	0.5	1					0.3	0.5	2	2	1	1	0.2	0.2	0	10.7
Data Mux										0.5	0.5	1			0.1	0.1	0.2	1	1	1	0.2		0.2	0	5.8
Fast Command							0.2			0.1	0.5					0.1	0.2	1	1	1	0.2	0.1		0	4.4
Error Handling	1	2	0.5	1	2	1	0.2			0.2	0.5	0.2	0.1		0.1	0.1	0.5	2	4	1	0.2	0.1		0	16.7
I2C				1	2	1	0.2			0.5	1	0.2			0.1	0.1	1	2	1	1	0.2	0.1	0.5	0	11.9
Efuse	0.5	0.5	0.5		2	1						1	0.5		0.5	0.1	1	1	1	1	0.2	0.1	0.5	0	11.4
PLL Calibration / EPortRX training	0.2	0.2	0.1													1			1	0.2				0	2.7
1.28 Tx Gbps digital	1	1										0.5			0.5	0.5	0.5	0.1	0.1	1	0.2	0.1	0.5	0	6
1.28 Tx Gbps analog / full custom	1	1	1											1	1	0.1	0.5	0.1		1	0.1	0.1	0.5	0	7.4
Latency Control Management	0	0	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Trigger Algorithm	0	0	1	2	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	11.2
Top Level	0	0					2	2	3	1	2					2	2				2		0.2	1	17.2
System Level	0	0																							0
	3.7	4.7	3.3	4.5	9	5	3.5	3	4	3.3	6.5	3.8	0.6	2	3.3	4.7	9.4	15.2	18.1	12.2	8.3	1.3	4	1	134

- Design team completed ~12 person-weeks of ECON work in 4 weeks since July 8 PMG.**
- Physicists + design team specified critical "blue" blocks.
- Realistic milestones for tracking progress provided at next ASICs PMG

**Assuming yellow is 20% complete, green is 100% complete

Additional material

ECON effort update based on JDL minutes

	JH Worse Case [FTE]	JH Best Case [FTE]	JDL plan [FTE]	JDL [FTE-yr in FY20]
Ralph	1	1	1	0.75
Mike (ANL)	0.6	0.6	0.6	0.45
Gregory	0.4	0.4	0.4	0.3
Alpana	0.4	0.4	0.4	0.3
Sandeep	0.5	0.8	0.8	0.6
Jim Hoff	0.5	1	1	0.75
Davide	0	0	0.5	0.38
Farah	0	0	0.5	0.38
Total	3.4	4.2	5.2	3.9
ECON duration (190 p-wks)	56 weeks	45 weeks	37 weeks	
ECON duration (250 p-wks)	74 weeks	60 weeks	48 weeks	

ECON effort

- Four scenarios based on required and available effort:
  A. 190 person-weeks required / 4.2 person-years available : OK
  B. 190/3.5 : Tight but feasible
  C. 250/4.2 : ECON delays system test and production
  D. 250/3.5 : ECON delays system test and production

- Scenario A presented on May 14, and deemed barely feasible.
  - Recommendation to accelerate w.r.t. Scenario A

	Worse Case	Best Case
Ralph	1	1
Mike (ANL)	0.6	0.6
Gregory	0.4	0.4
Alpana	0.4	0.4
Sandeep	0.5	0.8
Jim Hoff	0.5	1
Total	3.4	4.2
ECON duration (190 p-wks)	56 weeks	45 weeks
ECON duration (250 p-wks)	74 weeks	60 weeks