ECON ASICs

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Pam Klabbers, Ralph Wickwire

ASICs PMG

9 Sep 2019

JH/CMS homework

- **Meeting with SCD** for bringing software expert into ASIC verification effort.
  - Hirschauer followed up with Liz + JimA; they proposed a few names (with associated skill sets) and received Hirschauer's feedback.
  - Next step is to plan meeting(s) with Hoff and two candidates.

Recent activities

- Initiated new weekly "**ECON One-hour Round Table**" (Tuesday, 3pm) to try to organize effort of large team more efficiently
    - Each team member gives 4-minute report on
        - recent progress
        - what input/decisions they need
    - Final 20 minutes devoted to listing Action Items that came up, identifying most critical inputs/decisions, arranging small-group topical meetings during the week

- **Jim Hoff and Christian Gingu** have made excellent progress setting up the **UVM framework**
    - Their progress is in turn driving Ralph's efforts to have a fully integrated top-level design (with dummy blocks in places)
    - Already have near term milestone that the basic test bench should be passing data by late September.

- **Mike and Sandeep** are making progress on modifying Mike's **ePortRx + Word Aligner block** to work with methods decided last month for TMR and scan chains.
    - Sandeep has completed library characterization for new radiation models.

- **Wickwire and Hirschauer** made good progress on adding Fast Command, Registers aking progress on modifying Mike's **ePortRx + Word Aligner block** to work with methods decided last month for TMR and scan chains.
    - Sandeep has completed library characterization for new radiation models.

Milestones (1)

Hoff
Gingu
Wickwire
Miryala
Hammer
Unknown
Deptuch
Hirschauer/ Noonan **
Noy ***
All

	1-Aug	15-Aug	1-Sep	15-Sep	1-Oct	15-Oct	1-Nov	15-Nov	1-Dec	15-Dec	1-Jan
UVM track		Start building UVM Test bench			Basic TB passing data	UVM test plan document complete	Physics data prepared for simulation **				
Verilog / Design track				Start extracting PLL from full custom block	EportTx design Start			Finish extracting PLL from full custom block		EportTx design Done	Start Latency Management Verilog
Integration track	Integrate Word Aiigner, Fast Command, I2C into ECON-T top					All blocks (some empty) instantiated in EConT top and data flowing.	Start review/ modification of lpGBT RTL for EConT specific use		Complete review and correct functionality in EConT top (from top lpGBT laid out)	PLL integrated	ePortTx integrated
Physical design track	Complete library characterization for radiation corners		Start Full Implementation of ePortRx digital		Complete full Implementation of ePortRx digital	Start review of ePortRx analog functionality and layout		Complete review of ePortRx analog functionality and layout		ePortRx analog + digital layout complete	
Algorithm track	Preliminary Algo plan **				Final algorithm choice **		Algo spec complete **			Algo Verilog complete	
Review and Sign-off Track				EConT & specification reviewed with CERN.				EConT & specification reviewed with CERN.			

Milestones (2)

Hoff
Gingu
Wickwire
Miryala
Hammer
Unknown
Deptuch
Hirschauer/ Noonan **
Noy ***
All

	15-Jan	1-Feb	15-Feb	1-Mar	15-Mar	1-Apr	15-Apr	1-May	15-May	1-Jun	15-Jun
UVM track	Algo tested standalone with physics data		LM tested		System sim initiated with CERN team ***				UVM final signoff		
Verilog / Design track		Latency Management implemented in Verilog									
Integration track	Algo integrated		LM integrated								
Physical design track	Initial Floor plan complete	Start buffer PD		Complete buffer PD	Start Algo + LM PD		Finish Algo + LM PD		Top level PD done		
Algorithm track											
Review and Sign-off Track		EConT & specification reviewed with CERN.				EConT & specification reviewed with CERN.			System sim passing data & interfaces understood.***	Signoff review done	Submit

- Sandeep has completed library characterization for new radiation models.

Sep 9 ECON status

Color map	Definition of architecture	Study architecture and consensus	Block specification done 90%	Block RTL Implemented	Block testbench 90% implemented	Block Simulation 90% done, self checking	Block synthesis done	DFT method defined	DFT method implemented and tested	Triplication Method defined	Triplication in RTL complete	RTL Integration with Econ_t 90% done	Pinout List Complete / Interface compatability	Analog block layout complete	Block level Spice and SDF simulation	Block Formal Verification netlist to RTL done	Block PD 70% done	Top level UVM DV plan for block done	Top level UVM testbench 90% implemented	Top level UVM DV plan execution	Block level PD 100%	Pinout Layout Complete	Floorplan 100%	Top level PD 100% done	
Eport Rx							0.5			0.5	1	0.5		1	1	0.1	2	3	4	2	3	0.5	1	0	20.1
Aligner								1	1	0.5	1					0.3	0.5	2	2	1	1	0.2	0.2	0	10.7
Data Mux										0.5	0.5	1			0.1	0.1	0.2	1	1	1	0.2		0.2	0	5.8
Fast Command							0.2			0.1	0.5					0.1	0.2	1	1	1	0.2	0.1		0	4.4
Error Handling	1	2	0.5	1	2	1	0.2			0.2	0.5	0.2	0.1		0.1	0.1	0.5	2	4	1	0.2	0.1		0	16.7
I2C				1	2	1	0.2			0.5	1	0.2			0.1	0.1	1	2	1	1	0.2	0.1	0.5	0	11.9
Efuse	0.5	0.5	0.5		2	1						1	0.5		0.5	0.1	1	1	1	1	0.2	0.1	0.5	0	11.4
PLL Calibration / EPortRX training	0.2	0.2	0.1													1			1	0.2				0	2.7
1.28 Tx Gbps digital	1	1										0.5			0.5	0.5	0.5	0.1	0.1	1	0.2	0.1	0.5	0	6
1.28 Tx Gbps analog / full custom	1	1	1											1	1	0.1	0.5	0.1		1	0.1	0.1	0.5	0	7.4
Latency Control Management	0	0	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Trigger Algorithm	0	0	1	2	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	11.2
Top Level	0	0					2	2	3	1	2					2	2				2		0.2	1	17.2
System Level	0	0																							0
	3.7	4.7	3.3	4.5	9	5	3.5	3	4	3.3	6.5	3.8	0.6	2	3.3	4.7	9.4	15.2	18.1	12.2	8.3	1.3	4	1	134

- For next PMG : will adjust Status Matrix to improve consistency with Milestones
- Yellow = 20% complete, green = 100%

Aug 9 ECON status

	Definition of architecture	Study architecture and consensus	Block specification done 90%	Block RTL Implemented	Block testbench 90% implemented	Block Simulation 90% done, self checking	Block synthesis done	DFT method defined	DFT method implemented and tested	Triplication Method defined	Triplication in RTL complete	RTL Integration with Econ_t 90% done	Pinout List Complete / Interface compatability	Analog block layout complete	Block level Spice and SDF simulation	Block Formal Verification netlist to RTL done	Block PD 70% done	Top level UVM DV plan for block done	Top level UVM testbench 90% implemented	Top level UVM DV plan execution	Block level PD 100%	Pinout Layout Complete	Floorplan 100%	Top level PD 100% done	
Eport Rx							0.5			0.5	1	0.5		1	1	0.1	2	3	4	2	3	0.5	1	0	20.1
Aligner								1	1	0.5	1					0.3	0.5	2	2	1	1	0.2	0.2	0	10.7
Data Mux										0.5	0.5	1			0.1	0.1	0.2	1	1	1	0.2		0.2	0	5.8
Fast Command							0.2			0.1	0.5					0.1	0.2	1	1	1	0.2	0.1		0	4.4
Error Handling	1	2	0.5	1	2	1	0.2			0.2	0.5	0.2	0.1		0.1	0.1	0.5	2	4	1	0.2	0.1		0	16.7
I2C				1	2	1	0.2			0.5	1	0.2			0.1	0.1	1	2	1	1	0.2	0.1	0.5	0	11.9
Efuse	0.5	0.5	0.5		2	1						1	0.5		0.5	0.1	1	1	1	1	0.2	0.1	0.5	0	11.4
PLL Calibration / EPortRX training	0.2	0.2	0.1													1			1	0.2				0	2.7
1.28 Tx Gbps digital	1	1										0.5			0.5	0.5	0.5	0.1	0.1	1	0.2	0.1	0.5	0	6
1.28 Tx Gbps analog / full custom	1	1	1											1	1	0.1	0.5	0.1		1	0.1	0.1	0.5	0	7.4
Latency Control Management	0	0	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Trigger Algorithm	0	0	1	2	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	11.2
Top Level	0	0					2	2	3	1	2					2	2				2		0.2	1	17.2
System Level	0	0																							0
	3.7	4.7	3.3	4.5	9	5	3.5	3	4	3.3	6.5	3.8	0.6	2	3.3	4.7	9.4	15.2	18.1	12.2	8.3	1.3	4	1	134

- Design team completed ~12 person-weeks of ECON work in 4 weeks since July 8 PMG.**
- Physicists + design team specified critical "blue" blocks.
- Realistic milestones for tracking progress provided at next ASICs PMG

**Assuming yellow is 20% complete, green is 100% complete

Additional material

July 8 ECON status

	Definition of architecture	Study architecture and consensus	Block specification done 90%	Block RTL Implemented	Block testbench 90% implemented	Block Simulation 90% done, self checking	Block synthesis done	DFT method defined	DFT method implemented and tested	Triplication Method defined	Triplication in RTL complete	RTL Integration with Econ_t 90% done	Pinout List Complete / Interface compatability	Analog block layout complete	Block level Spice and SDF simulation	Block Formal Verification netlist to RTL done	Block PD 70% done	Top level UVM DV plan for block done	Top level UVM testbench 90% implemented	Top level UVM DV plan execution	Block level PD 100%	Pinout Layout Complete	Floorplan 100%	Top level PD 100% done	
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Data Mux										0.5	0.5	1			0.1	0.1	0.2	1	1	1	0.2		0.2	0	5.8
Fast Command							0.2			0.1	0.5					0.1	0.2	1	1	1	0.2	0.1		0	4.4
Error Handling	1	2	0.5	1	2	1	0.2			0.2	0.5	0.2	0.1		0.1	0.1	0.5	2	4	1	0.2	0.1		0	16.7
I2C				1	2	1	0.2			0.5	1	0.2			0.1	0.1	1	2	1	1	0.2	0.1	0.5	0	11.9
Efuse	0.5	0.5	0.5		2	1						1	0.5		0.5	0.1	1	1	1	1	0.2	0.1	0.5	0	11.4
PLL Calibration / EPortRX training	0.2	0.2	0.1													1			1	0.2				0	2.7
1.28 Tx Gbps digital	1	1										0.5			0.5	0.5	0.5	0.1	0.1	1	0.2	0.1	0.5	0	6
1.28 Tx Gbps analog / full custom	1	1	1											1	1	0.1	0.5	0.1		1	0.1	0.1	0.5	0	7.4
Latency Control Management	0	0	0.2	0.5	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	8.9
Trigger Algorithm	0	0	1	2	1.5	1	0.2					0.2				0.1	0.5	1.5	1.5	1	0.5		0.2	0	11.2
Top Level	0	0					2	2	3	1	2					2	2				2		0.2	1	17.2
System Level	0	0																							0
	3.7	4.7	3.3	4.5	9	5	3.5	3	4	3.3	6.5	3.8	0.6	2	3.3	4.7	9.4	15.2	18.1	12.2	8.3	1.3	4	1	134