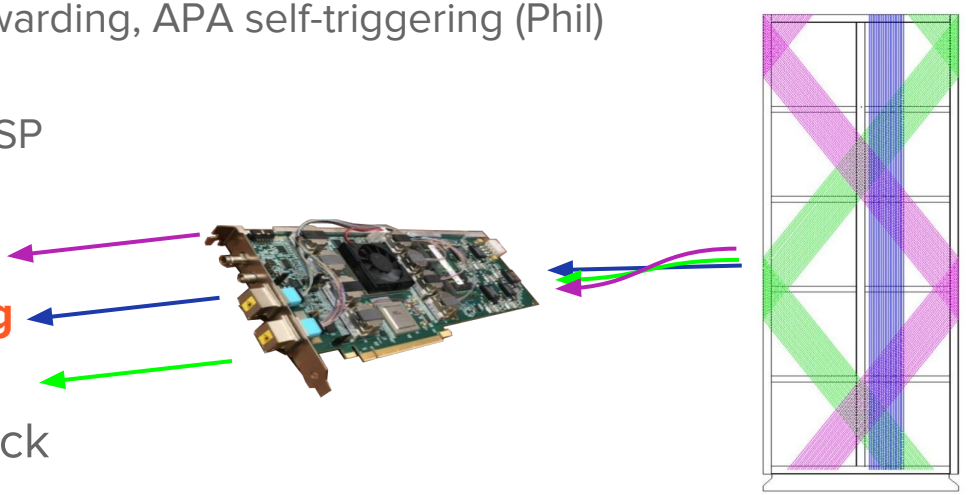
Short-term goals and needs

- Short-term (up to summer):
  - Improve monitoring and more benchmarking/optimization
  - Readout of very large windows (1 second)
  - FELIX firmware block for channel **reordering** (and inflating?) + decoder adjustment
  - Software **hit finding**, primitive forwarding, APA self-triggering (Phil)

- Most items to be tested in ProtoDUNE-SP
- … but we also have a dev setup

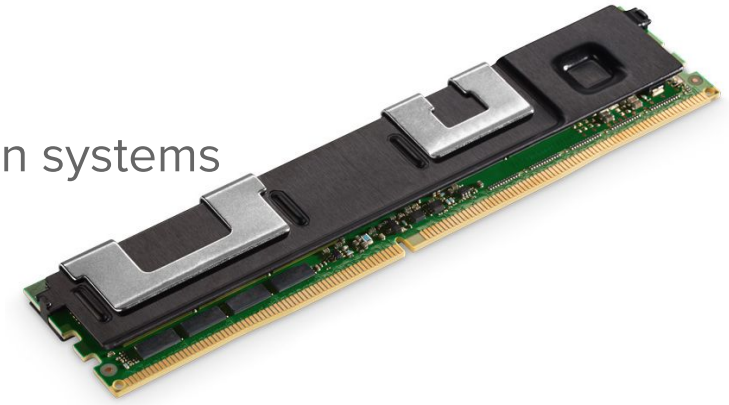


- Channel **reordering** firmware block
  - Demonstrator almost ready
  - Padding from 12b to 16b is achievable in terms of PCIe throughput for 1 plane
  - Will the WIB format change? If yes, how?

Medium-term goals and needs

- Medium-term (up to emptying of the cryostat):
  - **on-host** temporary storage and selection instead of full network dispatching
  - Emulation of SNB data flow exploiting Intel® Optane™ **Persistent memory**
    - (+ **DAQDB)**
  - Gradually transition ProtoDUNE to full FELIX readout
    - agreement to **purchase more cards**
  - Prepare libraries for standalone tests (DAQkit)
    - Requires a **WIB emulator**

- **DAQDB**: Key-Value store for data acquisition systems
  - Prototyping at CERN
  - Can handle APA data for $\mathcal{O}$(minute)



Long-term goals and needs

- Long-term (at cryostat refilling):
  - Revamp software
  - Need **defined interfaces** (CCM, DCS?)
  - Read out Photon-Detector system (?)

Needs for TDR

- Current ProtoDUNE's FELIX technology has been proven to work
  - Minimal firmware modifications required
  - Accelerated compression
  - Careful choice of server specifications

Needs by EDR

- Assessment of prototypes in order to choose technology
- Decision on co-processor integration
- Decision on buffering technology/solution
- Numerology, power, networking infrastructure
- Define interfaces to Photon-detector and Dual-Phase

What must be done at ProtoDUNE

- Deploy upgrades and test them when needed
- Stick to ProtoDUNE “official” planning for now

Backup

Reordering firmware block

- Will the WIB format change? If yes, how?
  - Not scattered channels
  - Ordered by plane
- Demonstrator for reordering firmware block almost ready.
  - Defragmenting channels and reordering by plane (per COLDATA block)
- Padding 12b channels to 16b achievable in terms of PCIe throughput for 1 (or 2) planes:
  - 464 B (144 of which W plane) => 9.28 GB/s
  - 552 B if padding W plane to 16 b => 11.04 GB/s
  - Well below 16 GB/s
  - Need some thought to include it in the present firmware data flow...