The Design and Development of the JSNS^2 DAQ Upgrade

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For the JSNS^2 Collaboration

UNIVERSITY OF MICHIGAN · HEISING-SIMONS FOUNDATION · JSNS^2 J-PARC Sterile Neutrino Search at J-PARC Spallation Neutron Source · NEUTRINO 2020
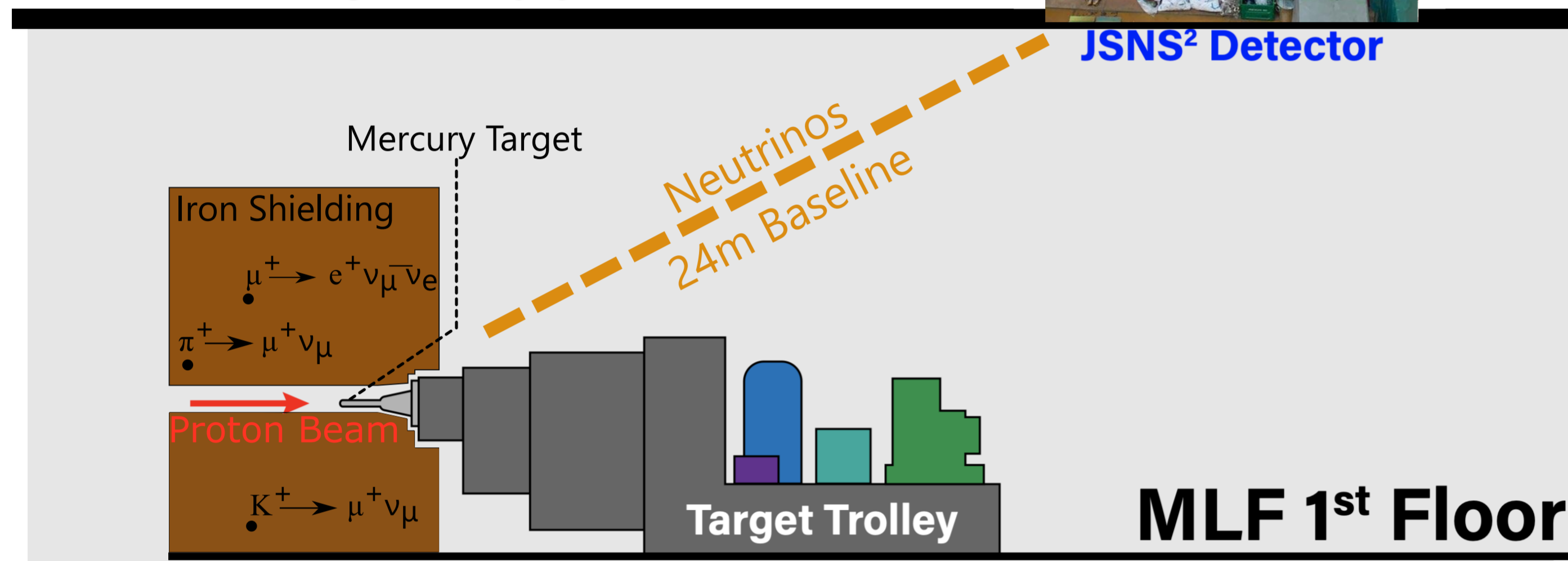
JSNS^2

The J-PARC Sterile Neutrino Search at the J-PARC Spallation Neutron Source (JSNS^2) began taking data with DAQ electronics donated by the Double Chooz experiment. The Double Chooz electronics, however, were not designed for a beam based experiment and are not sensitive across the entire energy range of interest for JSNS^2.

I have been working, as part of a team, to develop upgrade electronics that will be better suited to JSNS^2's energy and timing requirements. The upgrade electronics will **enhance our physics capabilities by providing a excellent efficiency and resolution over a large energy range**.
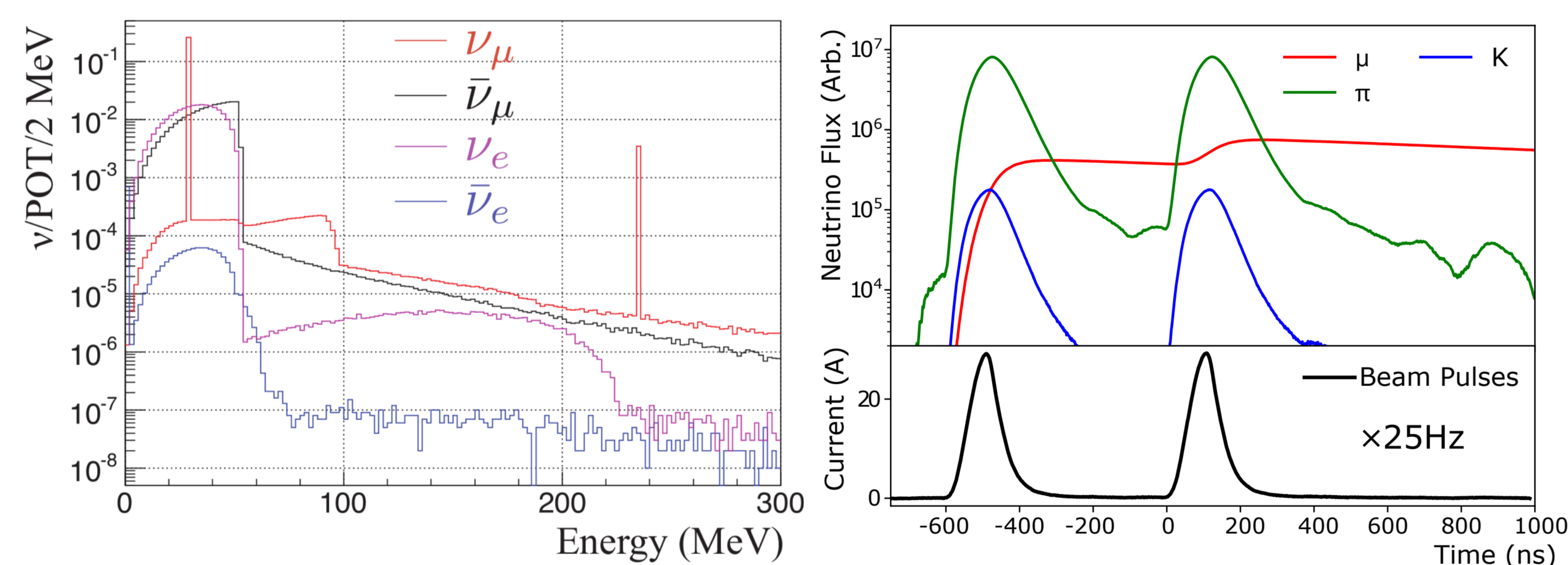
The electronics will need to trigger based upon timing signals from the beam facility as well as event energy and timing conditions. Our system will leverage modern FPGA and telecom electronics to meet these requirements.
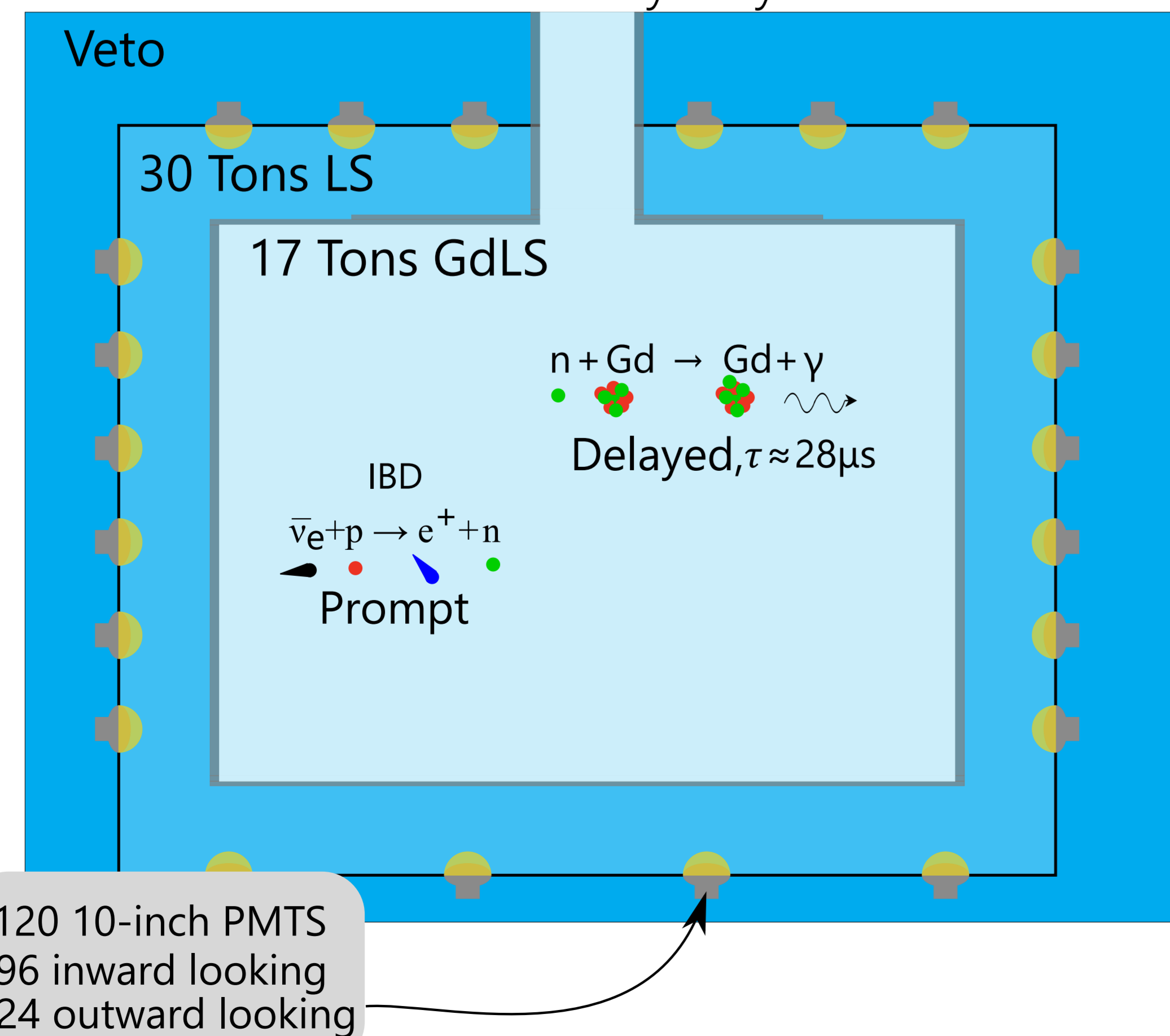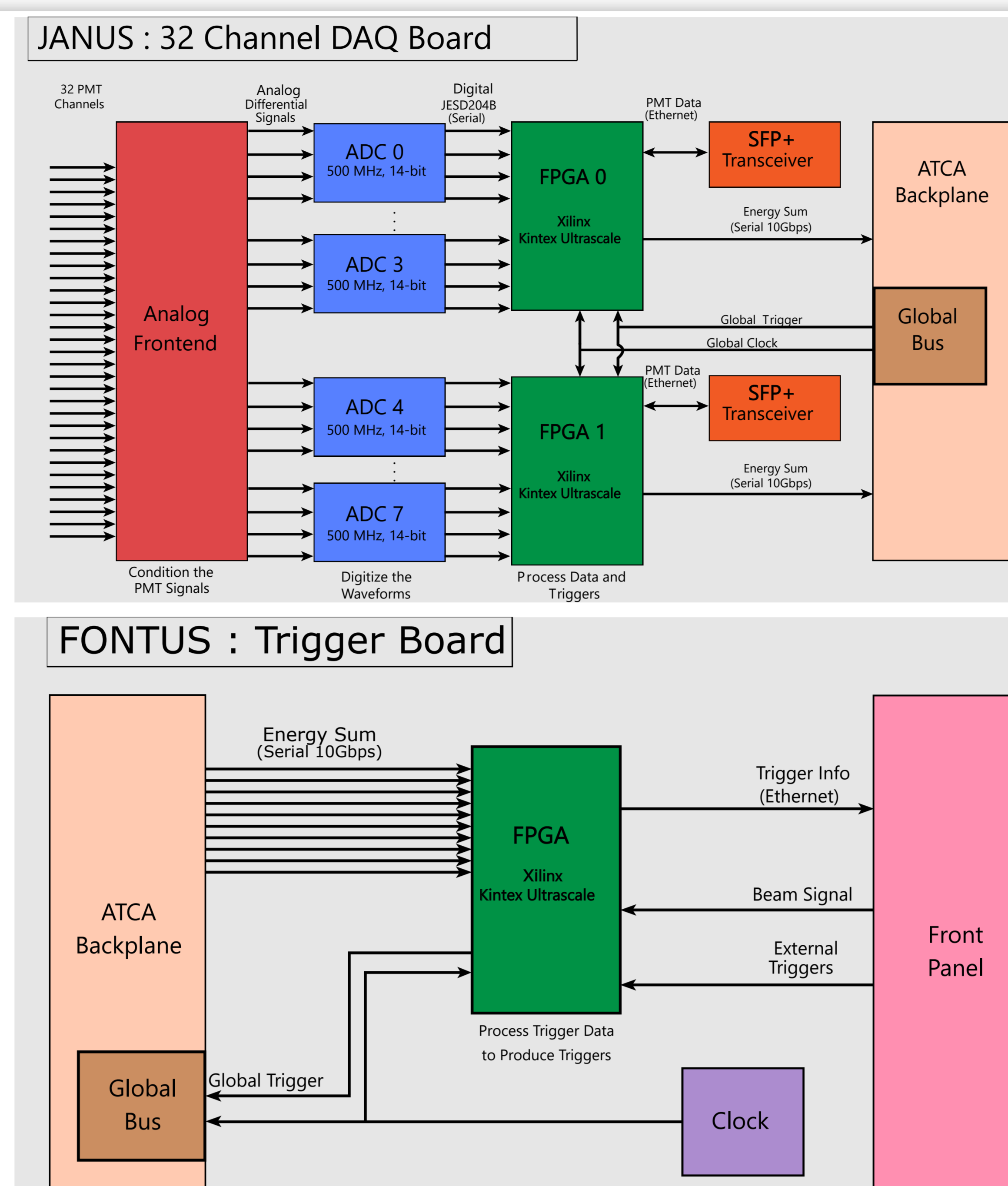

MLF 3rd Floor

JSNS^2 Detector

Mercury Target · Iron Shielding · Neutrinos 24m Baseline · Proton Beam · Target Trolley · **MLF 1st Floor**

$\mu^+ \to e^+ \nu_\mu \bar{\nu}_e$
$\pi^+ \to \mu^+ \nu_\mu$
$K^+ \to \mu^+ \nu_\mu$

Beam Neutrino Production: Spectrum & Timing

JSNS^2 Detector & Primary Physics Interactions

Veto
30 Tons LS
17 Tons GdLS
$n + Gd \to Gd + \gamma$
Delayed, $\tau \approx 28\mu s$
IBD
$\bar{\nu}_e + p \to e^+ + n$
Prompt

120 10-inch PMTS
96 inward looking
24 outward looking

Design

JANUS : 32 Channel DAQ Board

32 PMT Channels · Analog Differential Signals · Digital JESD204B (Serial) · ADC 0 500 MHz, 14-bit · ADC 3 500 MHz, 14-bit · ADC 4 500 MHz, 14-bit · ADC 7 500 MHz, 14-bit · FPGA 0 Xilinx Kintex Ultrascale · FPGA 1 Xilinx Kintex Ultrascale · PMT Data (Ethernet) · SFP+ Transceiver · ATCA Backplane · Energy Sum (Serial 10Gbps) · Global Trigger · Global Clock · Global Bus · Analog Frontend · Condition the PMT Signals · Digitize the Waveforms · Process Data and Triggers

FONTUS : Trigger Board

ATCA Backplane · Energy Sum (Serial 10Gbps) · FPGA Xilinx Kintex Ultrascale · Trigger Info (Ethernet) · Beam Signal · External Triggers · Front Panel · Global Bus · Global Trigger · Process Trigger Data to Produce Triggers · Clock
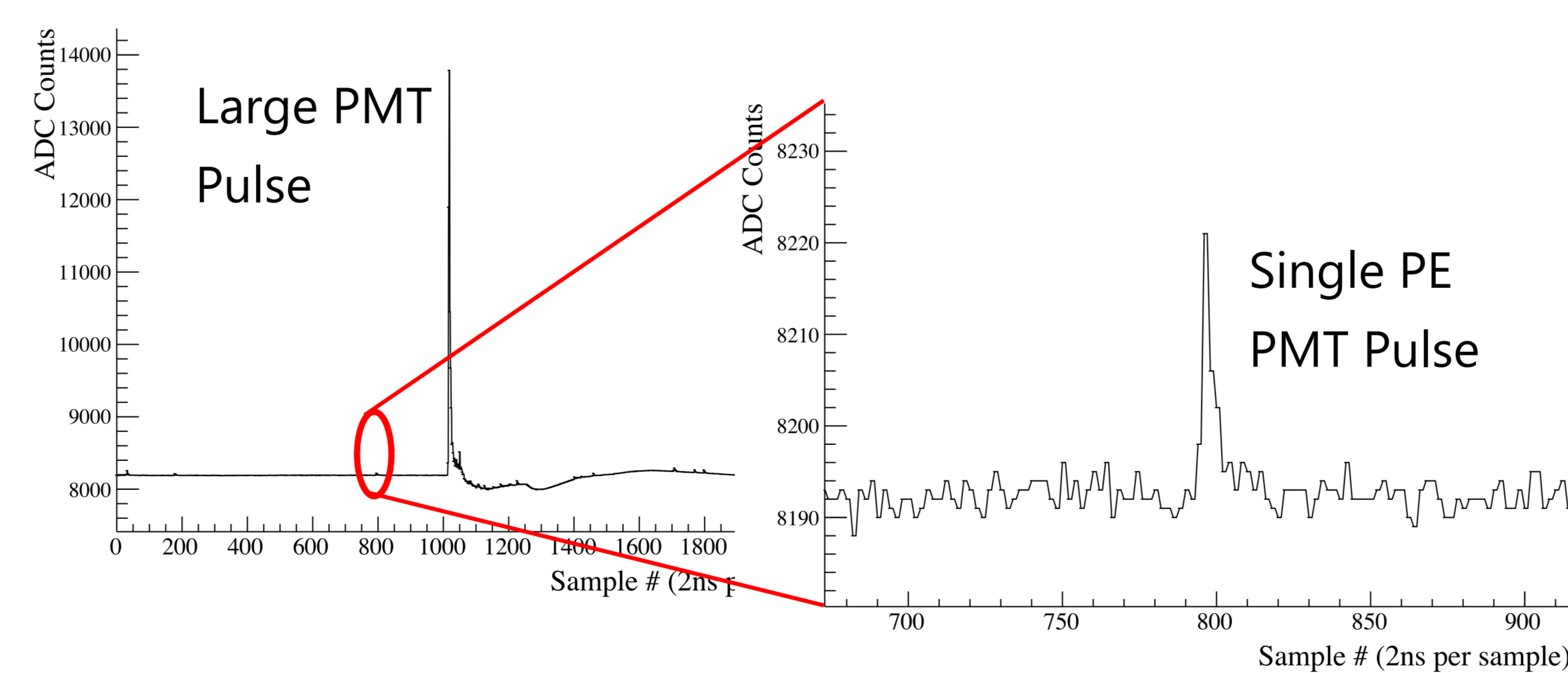
The FPGA based trigger allows event selection based on known event timing relations and the flexibility to design trigger logic specific to the physics of interest. Expected data readout rate is 1Gbps per FPGA.

The upgrade DAQ will be hosted within an ATCA shelf with 5 DAQ boards (JANUS) and one trigger board (FONTUS). **Design can be expanded to fit possible future needs.**
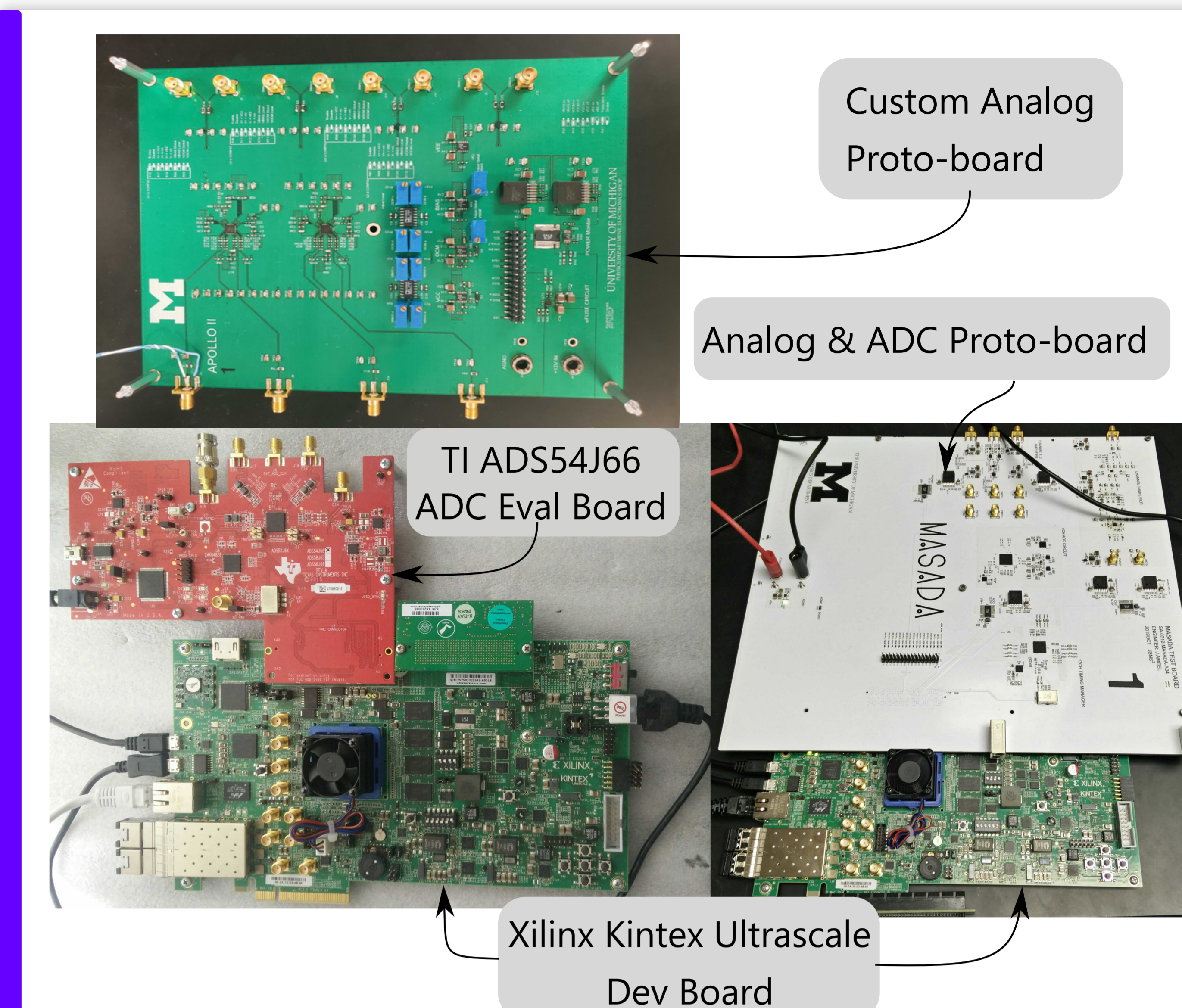

The Benefit of 14-bit Resolution
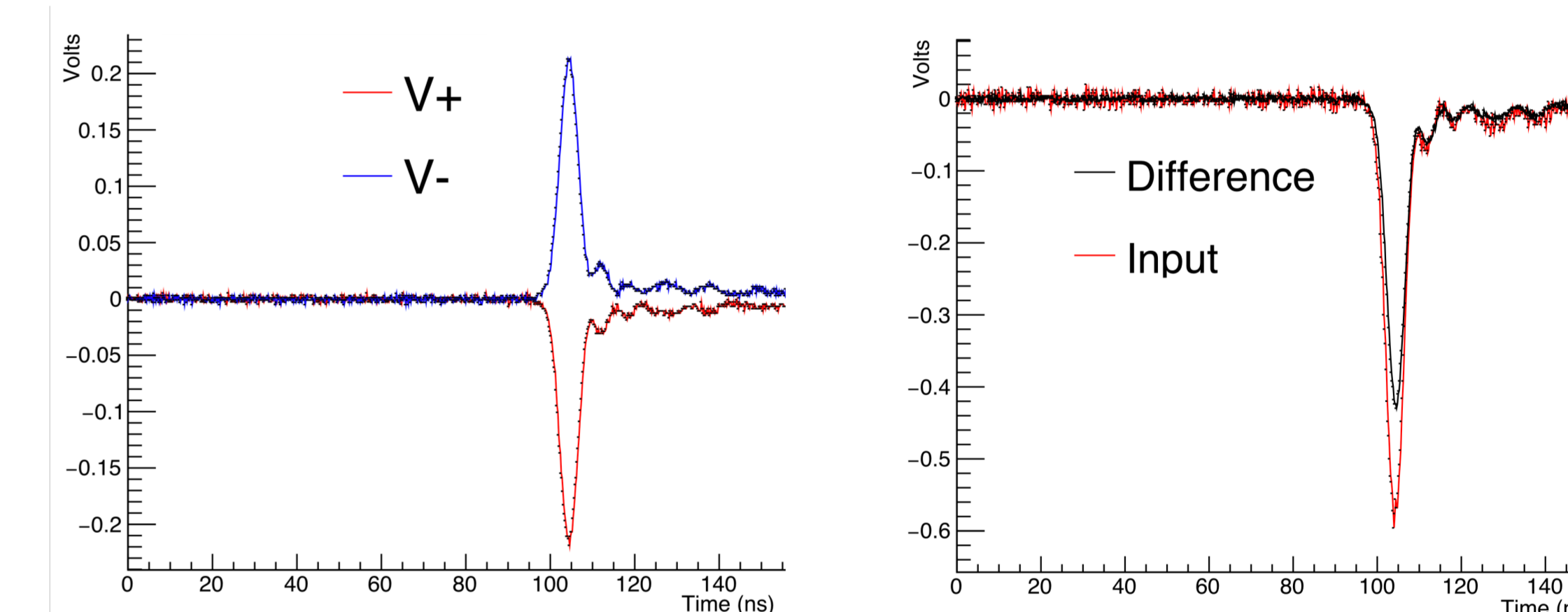

Large PMT Pulse · Single PE PMT Pulse

The 14-bit resolution & large dynamic range provides sensitivity to high energy neutrinos, e.g. KDAR neutrinos, without losing single-PE sensitivity.
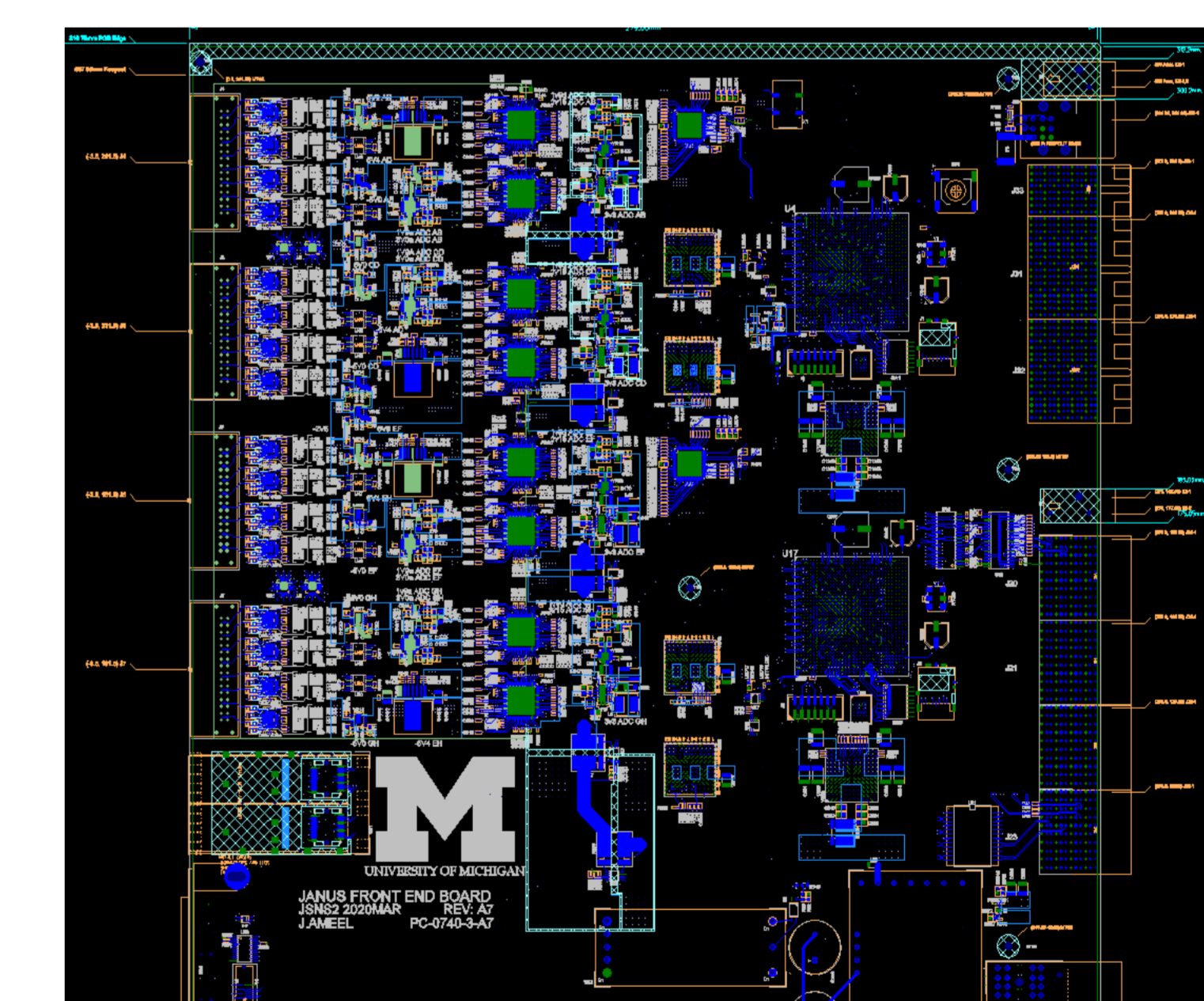
Development

Custom Analog Proto-board
Analog & ADC Proto-board
TI ADS54J66 ADC Eval Board
MASADA
Xilinx Kintex Ultrascale Dev Board

Firmware testing and development underway using commercial and custom bench-top electronics.

V+ · V− · Difference · Input

Tests of the analog circuitry have demonstrated its ability to produce a differential copy of the input with excellent signal integrity.

JANUS PCB design is complete

Proto-board that can emulate both JANUS & FONTUS functionality is being produced. Pending testing and production of the final JANUS & FONTUS PCBs **commissioning of the DAQ will begin Fall 2020**.

Once this design has been sucessfully deployed for JSNS^2 we hope to demonstrate this as a "one size fits all" DAQ solution for medium-scale liquid scintillator detectors.