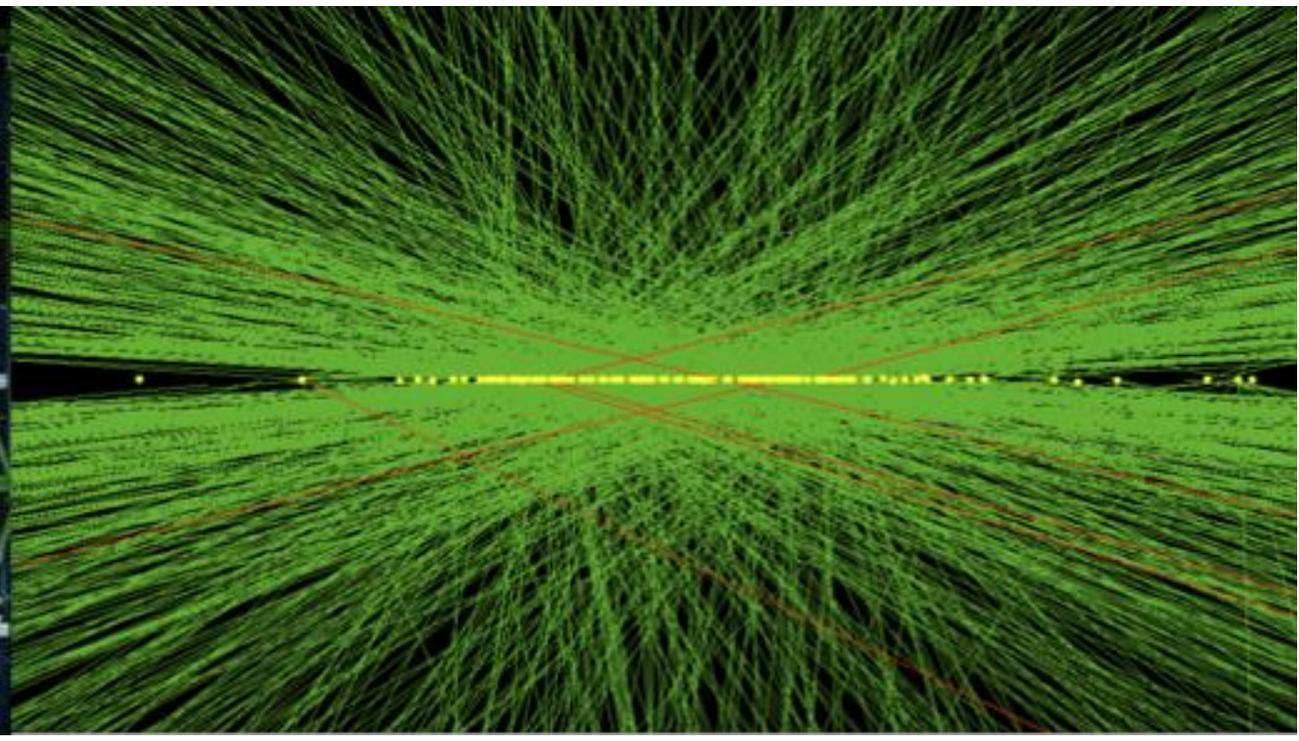
402.4.7 Electronics and Services

Jim Hirschauer (Fermilab)

HL LHC CMS Detector Upgrade CD-1 Director's Review

March 19, 2018



Outline

- Introduction and scope
- Conceptual design
- Cost, schedule, risks
- Organizational aspects
- Contributing institutions and resource optimization
- Quality assurance and quality control
- Prototype 1 plan and progress
- Summary

Biographical sketch

Charge #5

- Fermilab Scientist

HL-LHC upgrade:

- L3 manager for Endcap Calorimeter (EC) – Electronics and services
  - Lead physicist for ECON ASIC development/production
- iCMS coordinator for EC On-Motherboard Electronics

Phase 1 hadron calorimeter (HCAL) upgrade experience:

- L3 manager for barrel/endcap readout electronics since 2013
  - Lead physicist for QIE10/QIE11 readout ASIC development/production
- iCMS coordinator for HCAL barrel/endcap upgrade since 2013

Other experience:

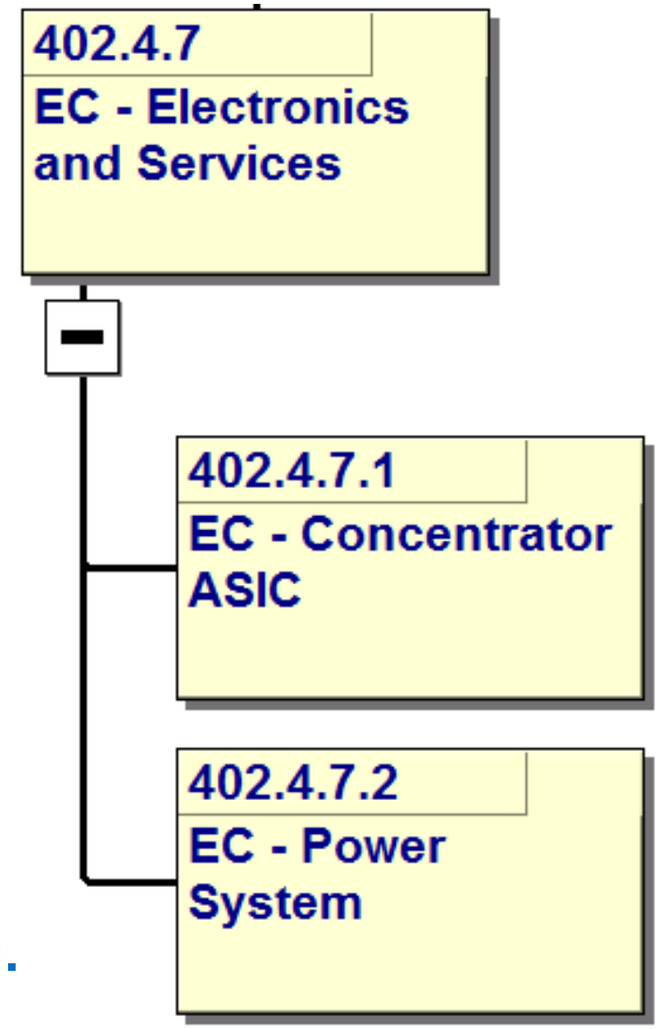
- HCAL Operations Coordinator 2011-12.
- Chair of HCAL Institution Board since 2018.

Research focus: Searches for supersymmetry in fully hadronic final states.

Introduction and scope

Deliverables and WBS structure

- 402.4.7.1 Concentrator ASIC
  - WBS includes specification, design, prototyping, prototype testing, production, packaging, and quality control of the "ECON" ASIC.
  - Deliverable is fully tested set of ASICs for entire EC.
  - Focus of this presentation.

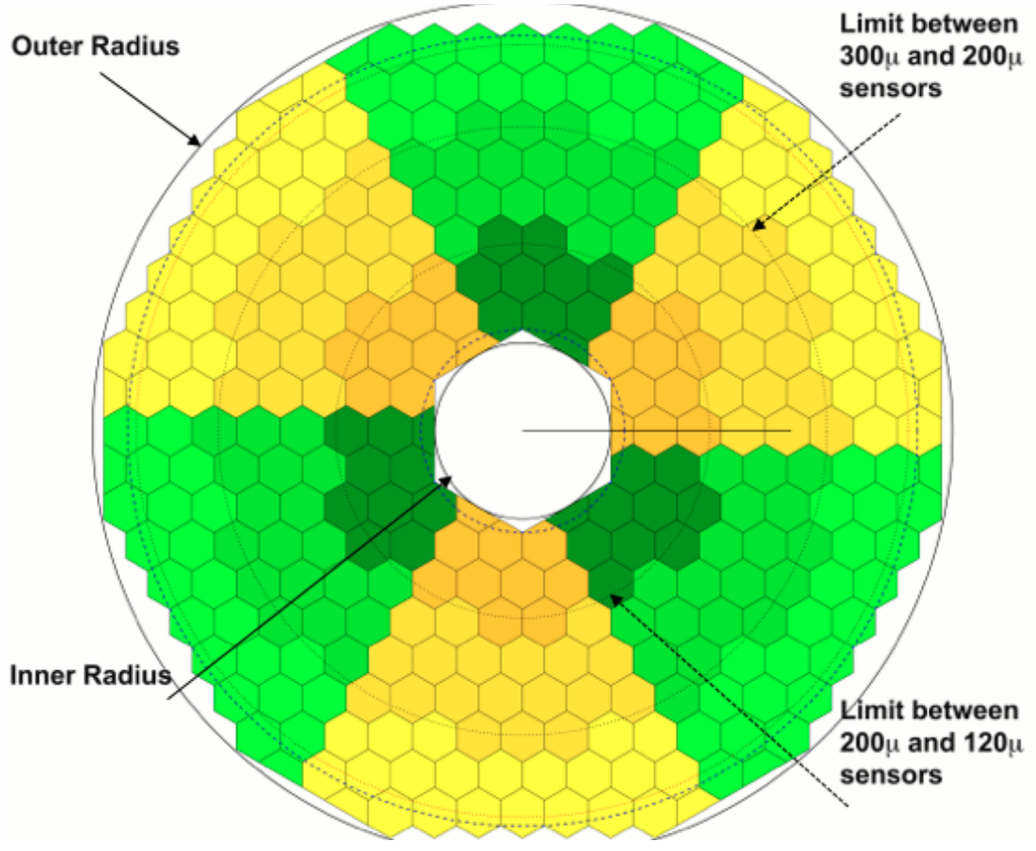


- 402.4.7.2 Power system
  - US is responsible for 40% of the low voltage (10V for electronics) and high voltage (1kV for Si bias) systems.
  - WBS includes specification, prototype evaluation, procurement, and QC of the US fraction of the power system.
  - Deliverable is 40% of the tested power system.

focus on ECON today ...

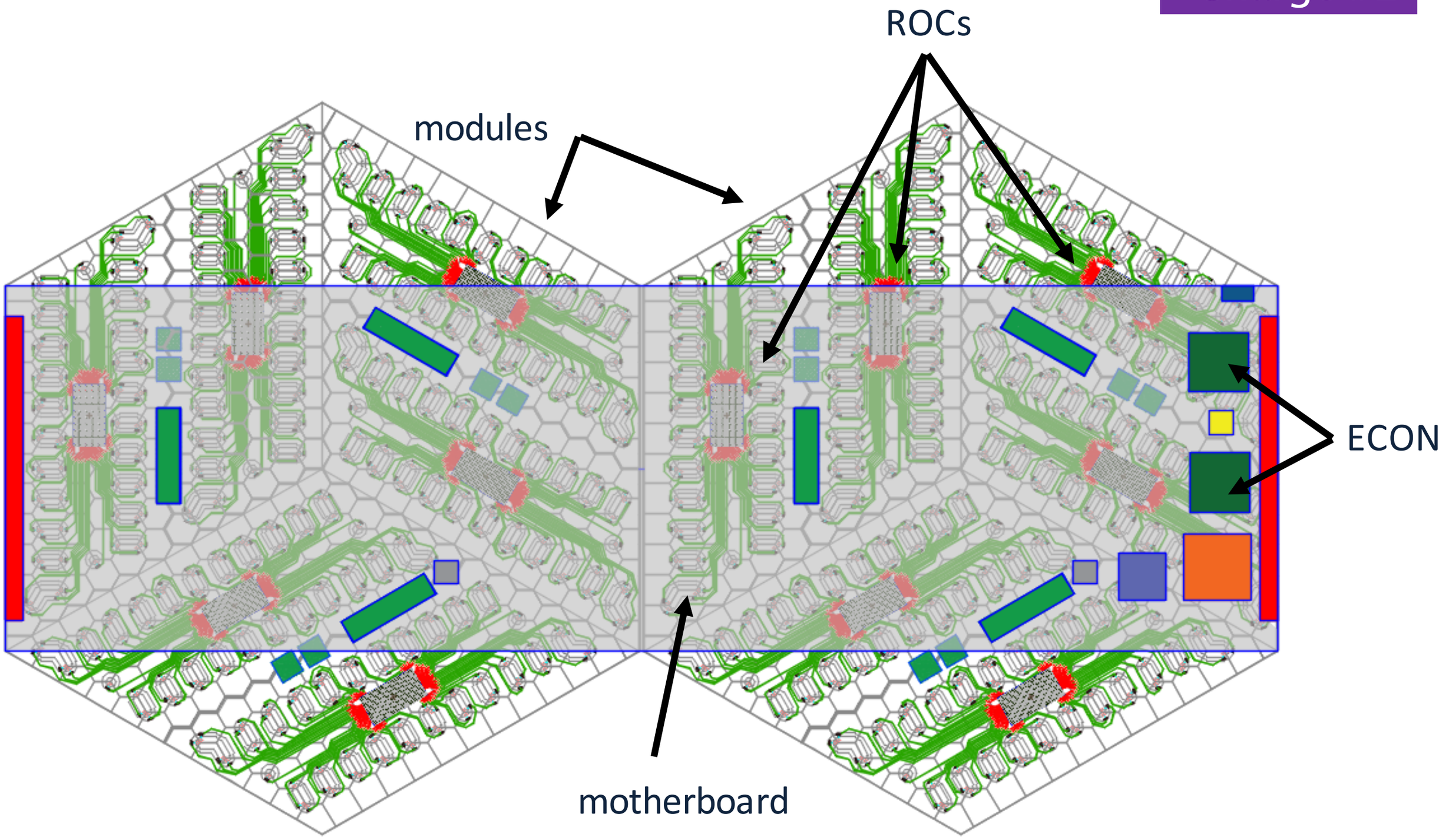
Summary of ECON purpose

- EC has 4.3M trigger channels each sending >10 bits of data at 40 MHz.
  - Naively requires 215k lpGBT links costing $90M at $400/link.
- However, interesting energy is deposited mostly in the central part of the detector.
  - Bandwidth density is lower in outer part of detector.
- ECON will select and concentrate data associated with interesting energy depositions to maximize use of available bandwidth.
- ECON-based system requires 7k links instead of 215k.



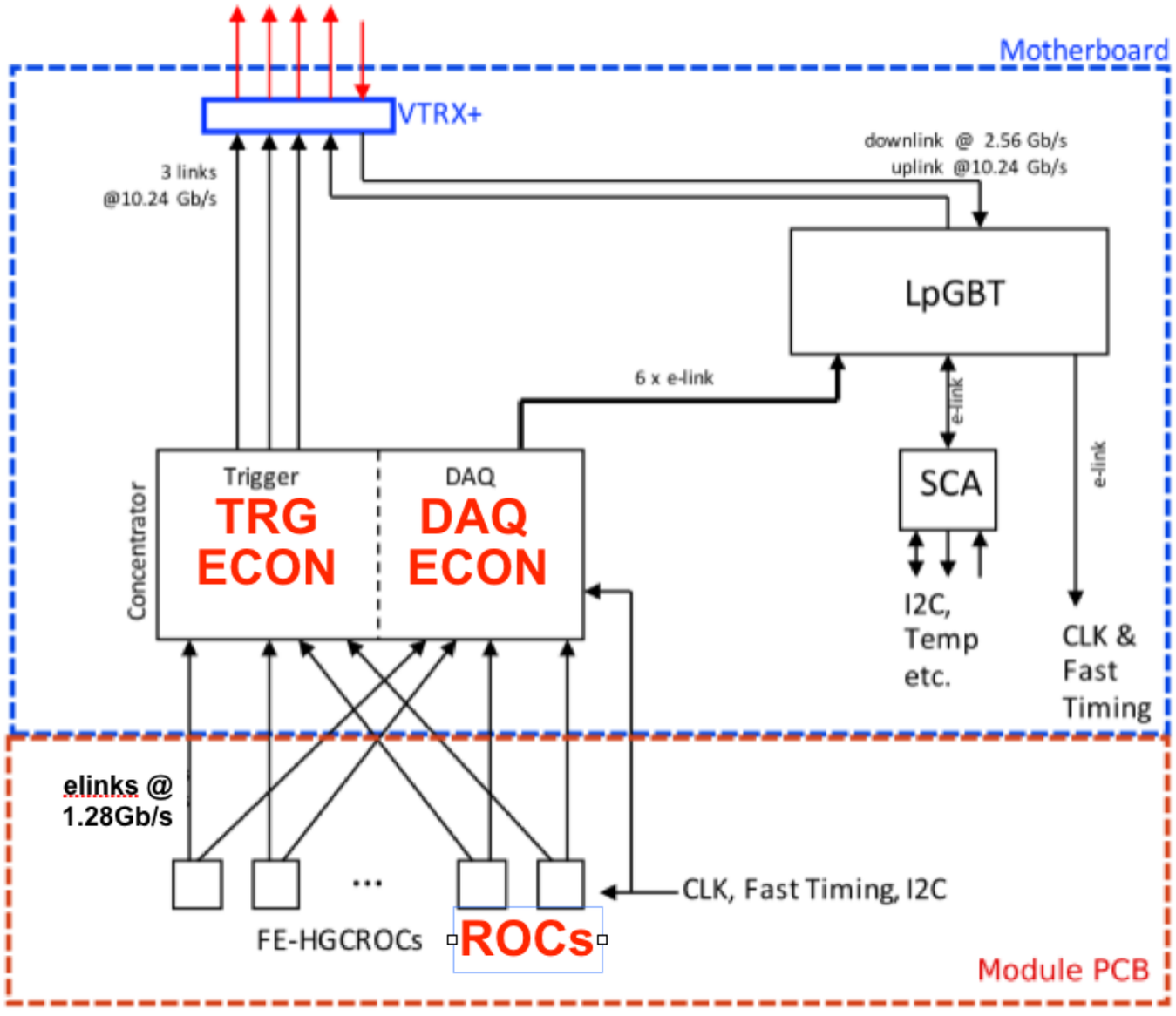
FE electronics architecture

Charge #2



Data flow

Charge #2



- Data flow from **module ROCs** → **motherboard ECONs** → **off-detector electronics** via two paths:
  - **40 MHz trigger (TRG) data:** ECON aggregates, selects/compresses, serializes, and transmits TRG data off-detector.
  - **750 kHz of (DAQ) data:** On L1 accept, ECON applies zero suppression, aggregates, serializes, and transmits off-detector via lpGBT.

Conceptual design

Relevant requirements

Charge #2

- **EC-sci-engr-010**: radiation tolerance for 10 year HL-LHC operation.
  - **EC-engr-083**: ECON rad tolerant to 2 MGy, 1x10^{16} 1MeV-equivalent neutrons/cm^2, with SEU compliance
  - expect maximum of 300 kGy and 3x10^{16}/cm^2 on-detector

- **EC-sci-engr-011**: fit within evolving CMS HL-LHC upgrade requirements of interfacing systems.
  - **EC-engr-084**: ECON power consumption ≤5mW/channel

- **EC-sci-engr-008**: provide trigger info at 40 MHz w/ 5μs latency

- **EC-sci-engr-012**: readout bandwidth to accommodate luminosities up to 7.5e34/cm^2/s and trigger rates up to 750 kHz.
  - **EC-engr-081**: ECON TRG data transmission at 40MHz and DAQ data transmission at 750 kHz
  - **EC-engr-082**: ECON max latency is 16 BX

- Link: https://cms-docdb.cern.ch/cgi-bin/DocDB/ShowDocument?docid=13447

Basic ECON reqs/specs

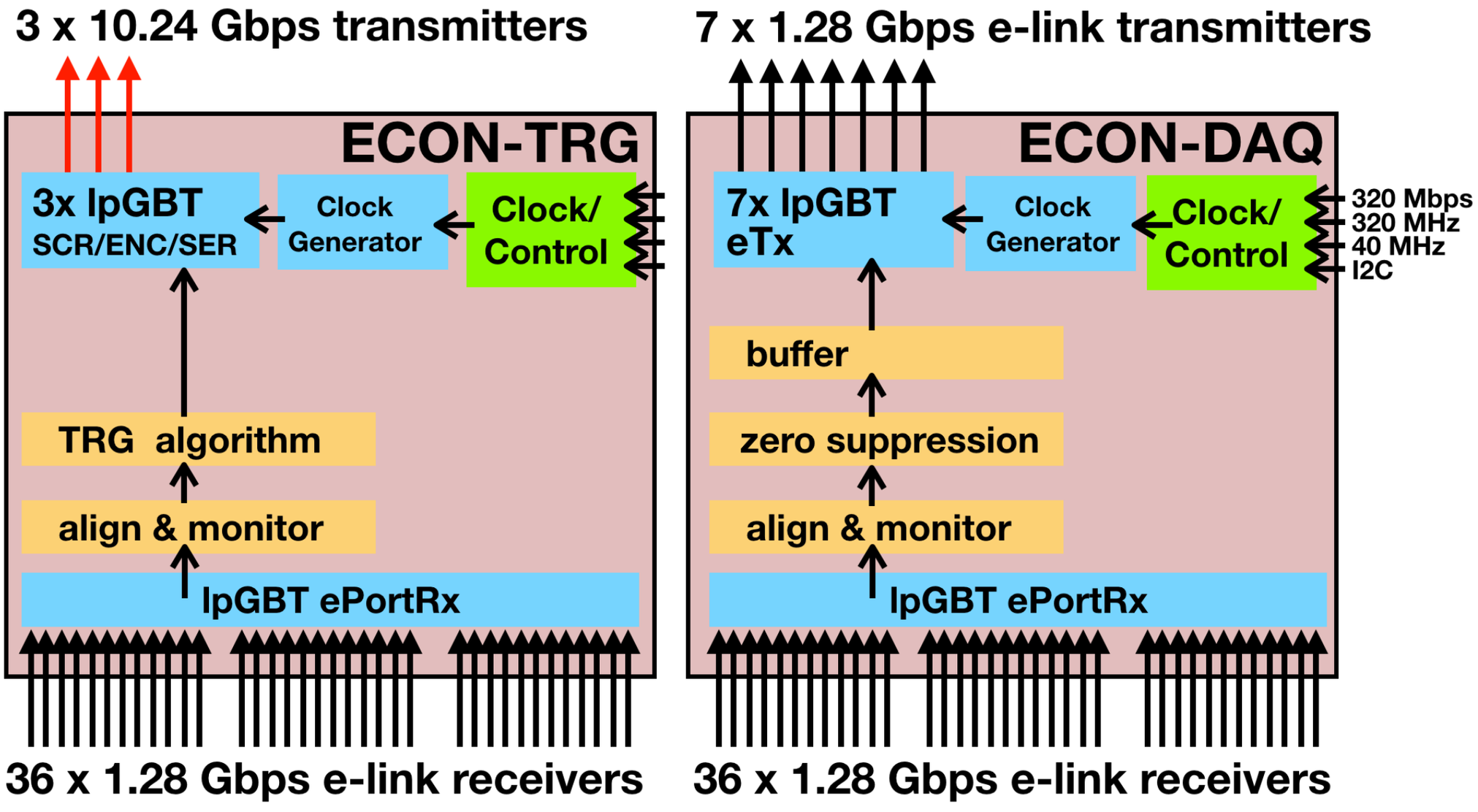
Charge #2

- Trigger data transmission at 40 MHz
- DAQ data transmission at 750 kHz
- 16 BX latency for TRG path
  - Impacts maximum depth of buffers and algorithm choices
- Radiation tolerance
  - Use 65 nm TSMC process
  - triple modular redundancy (where needed)
  - standard cell libraries as characterized for RD53, MPA ASIC
  - extensive testing at each prototype stage
- Low power
  - Use 65 nm TSMC process
  - Use power optimized design and algorithms
- Numbers of inputs/outputs
  - 36 inputs (1.28 Gbps), 7 outputs (1.28 Gbps), 3 outputs (10.24 Gbps).
  - Determined from system architecture.

ECON concept

Charge #2,#3

- Key components of I/O from lpGBT design : ePortRx with phase aligners, Clock Generator, 10.24 Gbps transmitter (scrambler/encoder/serializer and line drivers)
- lpGBT IP, documentation, test benches, etc. received in Sep 2018

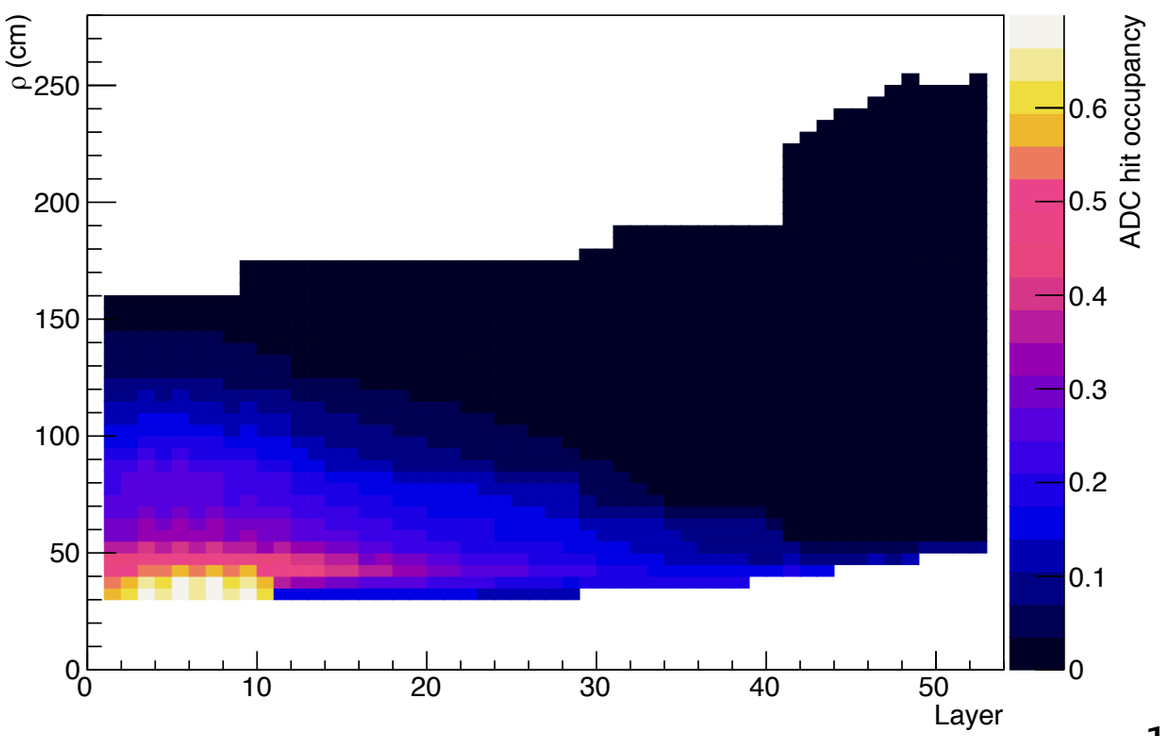


Occupancy and data rates

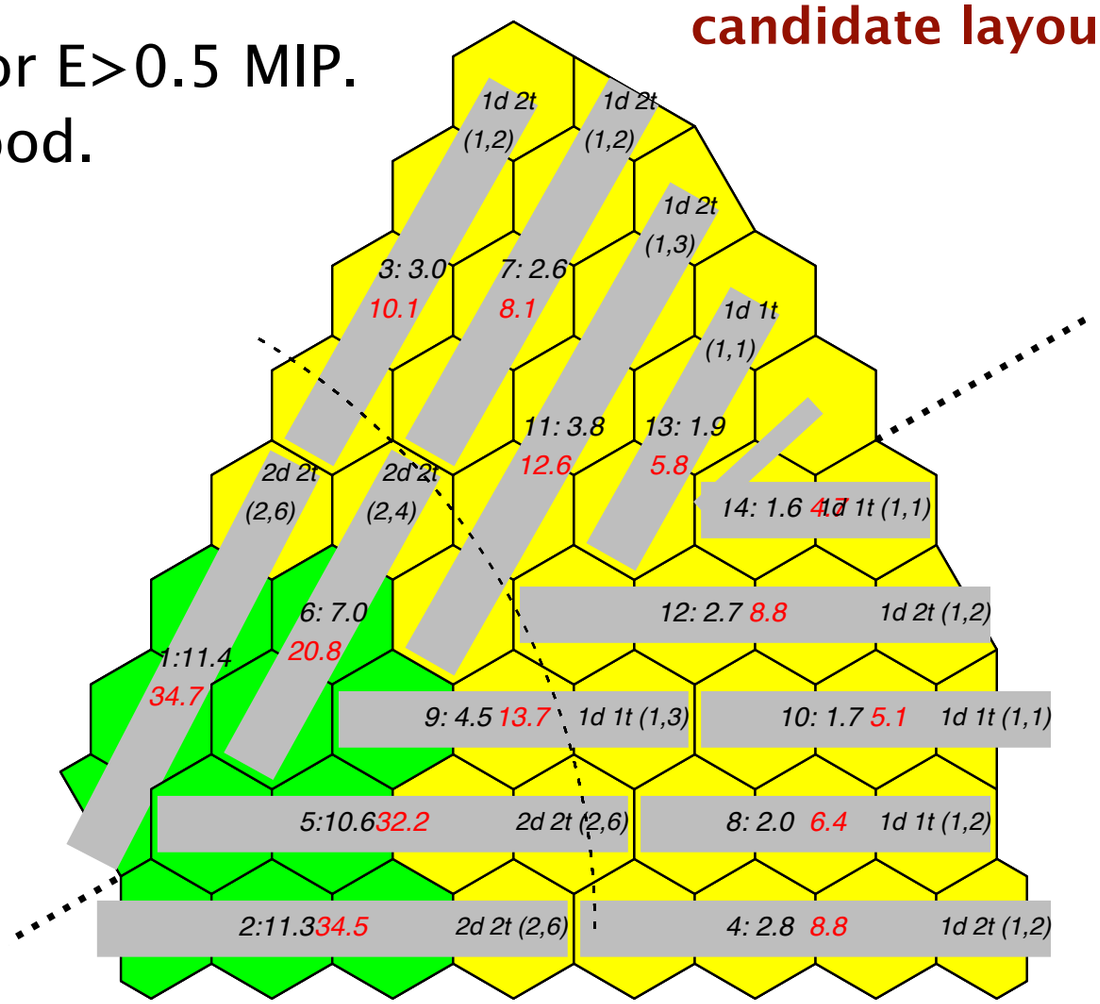
Charge #2

- Motherboard layout for 6th CE-E layer with data rates
  - Includes overhead associated with headers, alignment patterns, etc.
- Red numbers are TRG data rates [Gbps]:
  - Based on simple threshold-based algorithm: read out all TRG data for channels with E>2 MIP_T and sum of energy in each ROC.
- Black numbers are DAQ data rates [Gbps] for E>0.5 MIP.
- Occupancy and data rates are well understood.

Occupancy vs. layer and radius



Layer 6 Module and Motherboard candidate layout



ECON development plan

Charge #2

	2019												2020												2021											
	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D
ECON Prototype 1	Design								Fab			Package	Test				Extended	test																			
ECON Prototype 2									Design										Fab			Package	Test													
ECON Production																				Prep								Fab			Package	Test				

- Prototype 1 will allow characterization of:
  - power distribution for full chip
  - all I/O necessary for both ECON-T and ECON-D
  - clock generation with lpGBT clock manager
  - full size BGA package with close-to-final pin out
  - synchronization and monitoring for TRG path
    - Trigger algorithm development on ongoing.
      - Algorithm will be decided by July 2019.
      - Engineers will start Verilog in Sep 2019.
- Prototype 2 will allow characterization of:
  - synchronization and monitoring for DAQ path
  - Full logic for both ECON-T and ECON-D:
    - ECON-T TRG algorithm
    - ECON-D zero suppression
- Final chip

ECON design features & philosophy

Charge #4

lpGBT-related features

- **Challenging pieces of ECON design are taken from the lpGBT ASIC**, which as now been fabricated, evaluated, and characterized. ✅
  - ECON timing **jitter requirement less stringent** than for lpGBT since ECON does not distribute system clock for precise time measurement. ✅
  - **Power dissipation** of lpGBT is 50% of original estimate.
- Use **lpGBT transistor layouts** wherever possible. ✅
  - In few cases where RTL must be (re)synthesized (both lpGBT and new designs), use **standard cells recently characterized** for radiation corners (100, 200, 500 Mrad).
    - Will reduce challenge of timing closure experienced during lpGBT design ✅

Other features

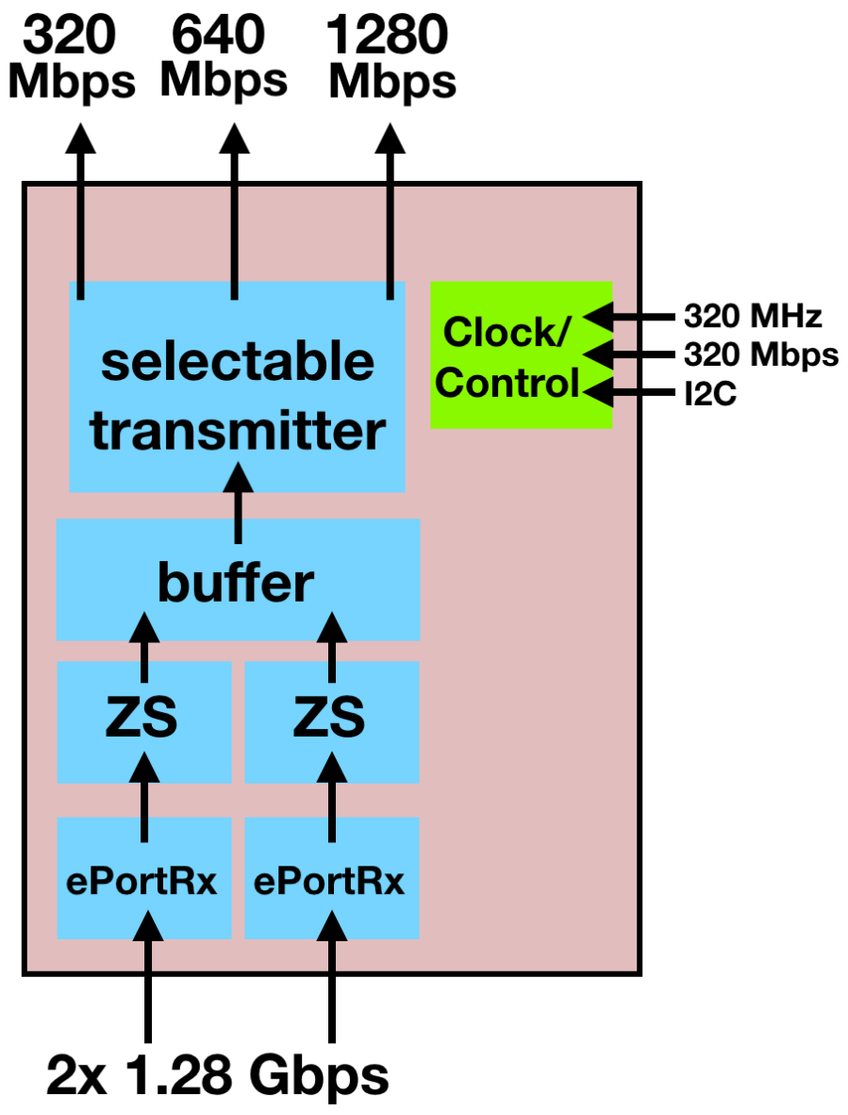
- Capitalize on **verification** tools and extensive verification experience developed for DUNE ASICs. ✅
- **Modularity** of design simplifies timing closure and interactions among the team. ✅
  - Possible (and required) because of use of lpGBT IP.
- **Parallelism of modular design** allows large team to make simultaneous progress. ✅
- **Functionality built in** to allow independent and easy testing of individual blocks. ✅
- **Individual lpGBT blocks** drive ECON floor plan and architecture since we reuse these blocks.

Architecture choices

- **Baseline architecture**
  - ECON-T with 3x 10.24 Gbps transmitters
    - *minimize motherboard complexity*
  - ECON-D with 36x inputs and 7x 1.28 Gbps outputs
    - *minimize complexity and variety of motherboards*
    - *minimize number of links*

- **Alternate architectures**
  - ECON-T with 1x 10.24 Gbps transmitter or 7x 1.28 Gbps transmitters
    - *requires 3 ASICs in close proximity to VTRx+ in high occupancy regions of detector*
  - ECON-D ➔ ECON-Dlite with 2x 1.28 Gbps inputs and 1x output with selectable rate
    - *motherboard schematic/layout depends on layer*
    - *increase number of links by ~10% with respect to baseline architecture*

ECON-Dlite concept

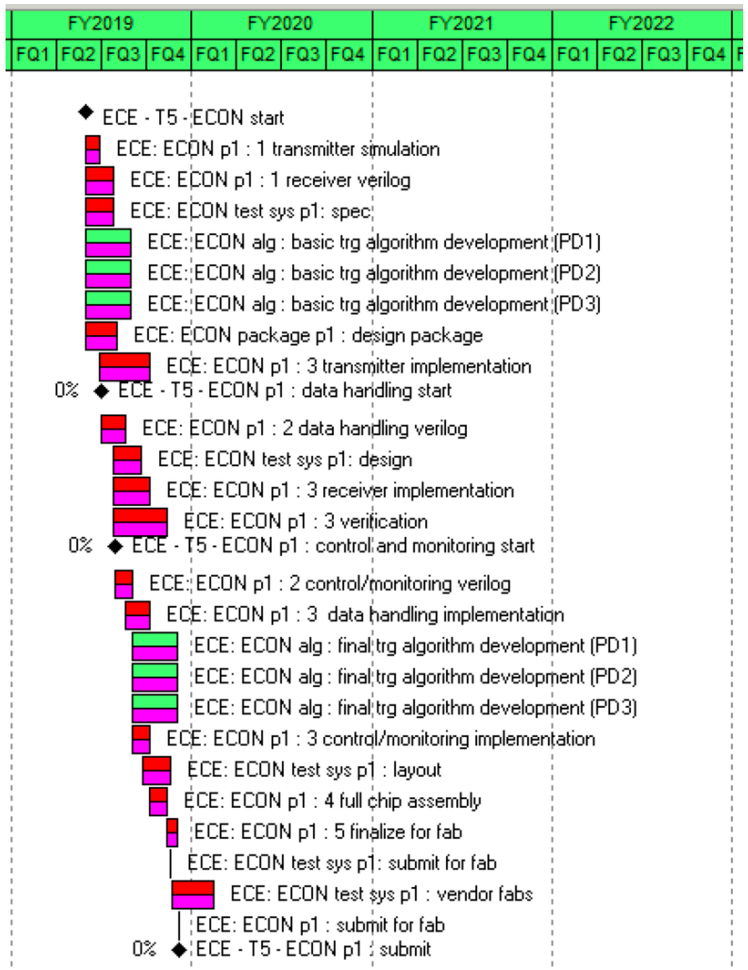


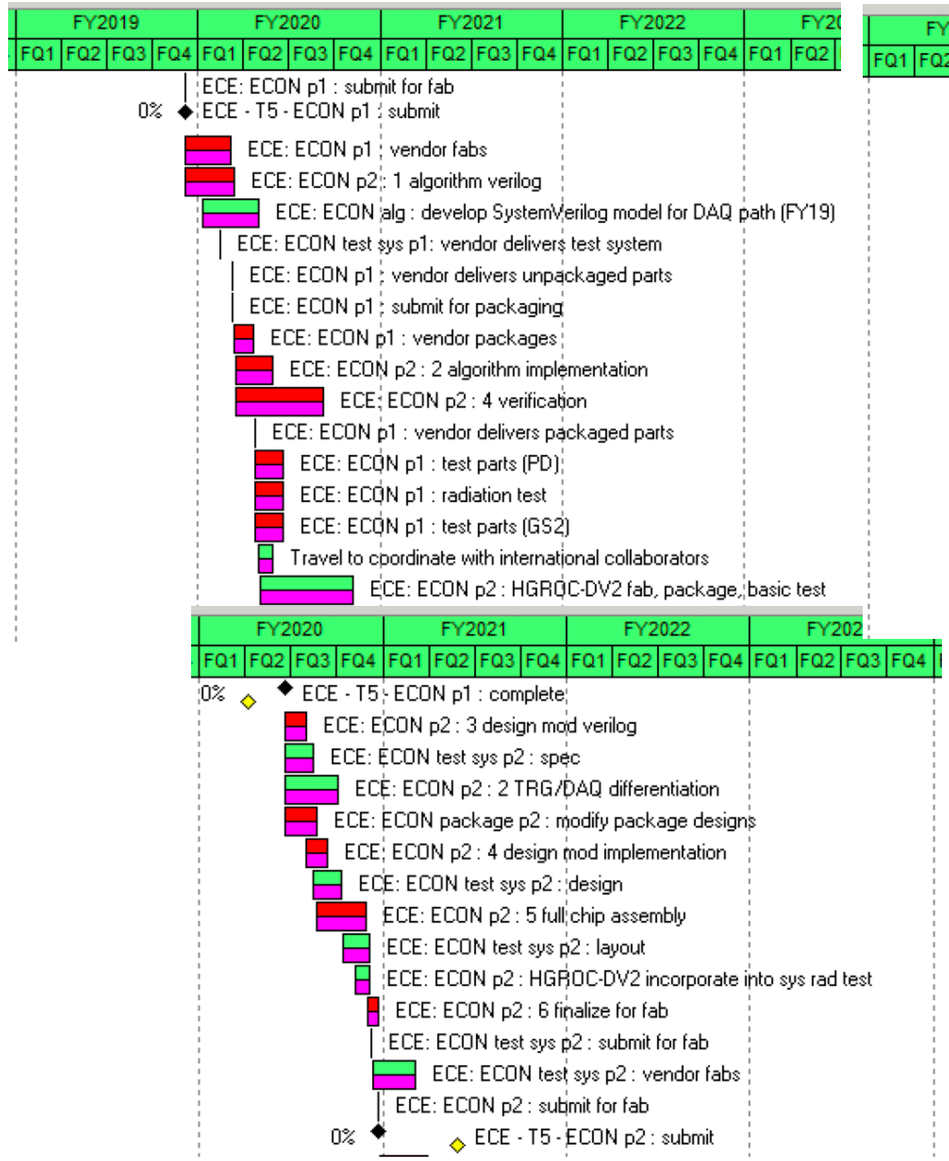
Cost and schedule

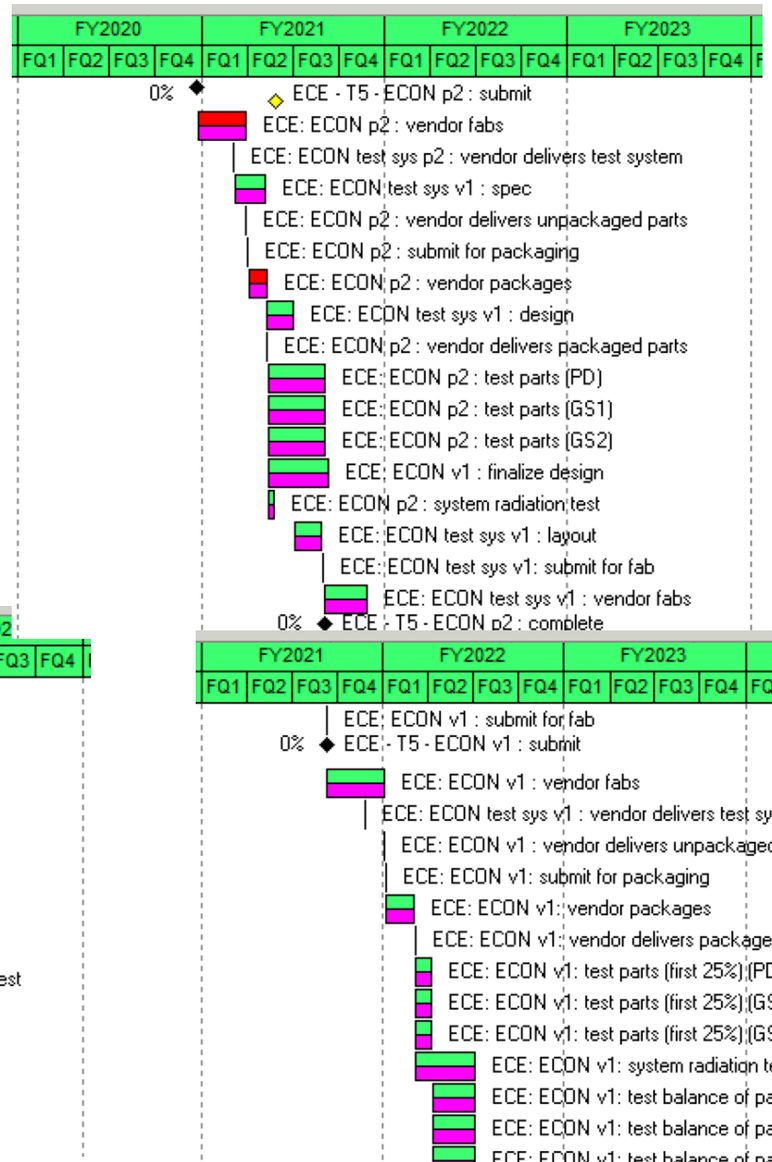
Schedule

Charge #3

- ECON working schedule was updated after freezing CD-1 DR documentation based on
  - analysis lpGBT designs by engineering team
  - finalization of spec based on lpGBT analysis
  - finalization of design team
  - design features/philosophy on slide 15
- P6 schedule in frozen CD-1 DR documentation does not reflect this new plan.
- New plan (which is cost neutral) has been implemented in P6:







Milestones

Charge #3

Layout: JFH start-BL-BL1 finish-BL-BL1 | Filter: All Activities

Activity ID	Activity Name	Start	Finish
402.4W-sandbox.7.1	**CE - Concentrator ASIC**	01-Mar-19	05-Apr-22
ES10000	ECE - T5 - 1 ECON start	01-Mar-19*	
ES10001	ECE - T5 - 2 ECON p1 : data handling start	01-Apr-19*	
ES10002	ECE - T5 - 3 ECON p1 : control and monitoring start	29-Apr-19*	
ES30110	ECE - T5 - 4 ECON p1 : submit		04-Sep-19
ES10280	ECE - T5 - 5 ECON p1 : complete		18-Mar-20
ES10510	ECE - T5 - 6 ECON p2 : submit		22-Sep-20
ES30100	ECE - T5 - 7 ECON p2 : complete		02-Jun-21
ES30120	ECE - T5 - 8 ECON v1 : submit		10-Jun-21
ES19990	ECE - T5 - 9 ECON : complete		05-Apr-22

- Milestones are from working schedule.
- Milestones for submission and completion of each stage of ECON development.
- ECON interface is to supply prototype 2 and production ASICs for motherboard assembly – each connection occurs at appropriate milestone.

Cost estimate

Charge #3

WBS	Direct M&S ($)	Labor (Hours)	FTE	Direct + Indirect + Esc. ($)	Estimate Uncertainty ($)	Total Cost ($)
402.4 CE - ENDCAP CALORIMETER	**$21,522,856**	**307884**	**174.15**	**$40,937,225**	**$11,938,425**	**$52,875,650**
402.4.2 CE - Management	$1,931,044	84688	47.90	$4,003,027	$748,653	$4,751,680
402.4.3 CE - Sensors	$7,412,621	9484	5.36	$8,147,707	$2,329,734	$10,477,440
402.4.4 CE - Modules	$3,377,138	96746	54.72	$9,549,106	$2,006,872	$11,555,978
402.4.5 CE - Cassettes	$3,374,244	43980	24.88	$9,027,990	$3,348,887	$12,376,877
402.4.6 CE - Scintillator Calorimetry	$2,078,576	44834	25.36	$3,827,891	$1,312,408	$5,140,299
402.4.7 CE - Electronics and Services	$3,349,233	28152	15.92	$6,381,503	$2,191,872	$8,573,375
402.4.7.1 CE - Concentrator ASIC	$1,906,300	25792	14.59	$4,396,258	$1,808,514	$6,204,772
402.4.7.2 CE - Power System	$1,442,933	2360	1.33	$1,985,246	$383,357	$2,368,603

- Cost drivers (direct+indirect+esc):
  - ECON production & prod. packaging (M&S) : $0.781M + $0.611M
  - ECON design (labor) : $1.774M (prototypes + production)
  - ECON testing (labor) : $0.574M (prototypes + production)

Critical path and float

Charge #3

- ECON p2 is on the critical path for validation of motherboard design; ECON final production is near the critical path.
  - 2 month float for providing final ECON for motherboard assembly
  - 3.5 month total US project float
  - 8.6 month international CMS float

- As described later, greatest schedule risk is need for another round of ASIC production
  - 7.5 month mean schedule impact

- More discussion at end of talk on how schedule can absorb ECON delays.

Risk : additional MPW run

Charge #3,#7

RT-402-4-18-D CE - Additional concentrator ASIC engineering (MPW) run is required

Risk Rank:	3 (High) **Scores:** Probability : 4 (H) ; Cost: 2 (M) Schedule: 3 (H))	**Risk Status:**	Open
Summary:	Current planning includes the cost of two Multi-Project Wafer (MPW) prototype runs. If a significant flaw is observed after the second run, a third cycle may be required. This risk addresses the need an additional single run (either DAQ or TRG).		
Risk Type:	Threat	**Owner:**	James F Hirschauer
WBS:	402.4 CE - Calorimeter Endcap	**Risk Area:**	Technical Risk / Quality
Probability (P):	50%	**Technical Impact:**	0 (N) - negligible technical impact
Cost Impact:	PDF = 3-point - triangular Minimum = 164 k$ Most likely = 241 k$ Maximum = 385 k$ Mean = 263 k$ P * <Impact> = 132 k$	**Schedule Impact:**	PDF = 3-point - triangular Minimum = 6 months Most likely = 7.5 months Maximum = 9 months Mean = 7.5 months P * <Impact> = 3.8 months
Basis of Estimate:	Current planning includes the cost of two Multi-Project Wafer (MPW) prototype runs. If a significant flaw is observed after the second run, a third cycle may be required. This risk addresses the need an additional single run (either DAQ or TRG). The M&S costs are $136k for the MPW run and $28k for packaging. The labor cost for additional design work to fix the observed flaw is a 3-pt triangular PDF : 0/0.17/0.5 FTE. It is assumed the flaw is fairly easy to fix and the exact time needed depends on when when the issue is discovered, if in the beginning, middle, or end of the cycle. The additional testing is assumed to be modest and covered by the labor included for ASIC testing in the baseline. The min/likely/max cost is hence 164/209/295 k$. The L3 burn rate due to the delay of downstream activities is $21k/month (CMS-doc-13481), but there are 6 months of float available before cassette assembly is affected. therefore: Min cost = $164k + 0 = $164k. Likely cost = $209k + 1.5 months * $21k burn rate = $241k. Max cost = $295k + 3 months * $21k burn rate = $385k.		
Cause or Trigger:		**Impacted Activities:**	JM: Implemented in P6 between 'ECON p2 test parts' and 'ECON v1 finalize design'
Start date:	31/Aug/2020	**End date:**	30/Aug/2021
Risk Mitigations:	We will work closely with engineers to make sure that two planned engineering (MPW) runs are sufficient. We will be using some code blocks from the lpGBT that would have undergone some testing before the two MPW runs, and we will be including the prototype ECON ASIC in a major system prototype vertical slice test before the production run.		
Risk Responses:	Request additional funding for a third MPW run and for design changes. Reduce the needed testing time. Accelerate or parallelize the production of the motherboards if possible and if needed accelerate the cassette assembly and testing. The cost of accelerating the assembly of cassettes is covered by a separate risk.		
More details:	CMS-doc-13481		

Risk : additional prod run

Charge #3,#7

RT-402-4-04-D CE - Concentrator does not meet specifications

Risk Rank:	2 (Medium) **Scores:** Probability : 2 (L) ; Cost: 3 (H) Schedule: 3 (H))	**Risk Status:**	Open
Summary:	If the concentrator ASIC does not meet specifications after the production masks are produced then an additional set of masks will need to be produced and additional engineering effort is required to adjust the design so that the ASIC meet specifications. The risk probability depends on how many engineering/multi-project wafer runs are done and tested before the production masks are produced, and also on the exact maturity of the design (progress made), and on the schedule, e.g. if all irradiation tests can be done before the production masks are fabricated. The full packaging costs are realized only once since we would find the problem before packaging. The masks will include both TRG and DAQ chips.		
Risk Type:	Threat	**Owner:**	James F Hirschauer
WBS:	402.4 CE - Calorimeter Endcap	**Risk Area:**	Technical Risk / Requirements
Probability (P):	10%	**Technical Impact:**	2 (M) - significantly substandard
Cost Impact:	PDF = 3-point - triangular Minimum = 907 k$ Most likely = 971 k$ Maximum = 1035 k$ Mean = 971 k$ P * <Impact> = 97 k$	**Schedule Impact:**	PDF = 3-point - triangular Minimum = 6 months Most likely = 7.5 months Maximum = 9 months Mean = 7.5 months P * <Impact> = 0.8 months
Basis of Estimate:	The M&S cost is $690k for masks and wafer and $25k for a single set up to package a few chips. The labor cost for the additional engineering effort is a 3-pt triangular PDF: 0.25-0.375-0.5 FTE. The min/likely/max cost is hence 781/813/846 k$. The L3 burn rate due to the delay of downstream activities is $21k/month (CMS-doc-13481). **Min cost = $781k + 6 month * $21k burn rate = $907k.** **Likely cost = $813k + 7.5 months * $21k burn rate = $971k.** **Max cost = $846k + 9 months * $21k burn rate = $1035k.**		
Cause or Trigger:	Concentrator ASIC as returned from production does not meet specification despite the two previous multi-project wafer runs (MPWs)	**Impacted Activities:**	
Start date:	30/Aug/2021	**End date:**	29/Aug/2022
Risk Mitigations:	This risk is mitigated by prototyping and testing the full design through two multi-project wafer submissions, and by design and production reviews. The ASICs from these will be used in full vertical slice tests, as well as beam tests and irradiation tests.		
Risk Responses:	To reduce the impact due to the delay of this ASIC we will need to implement a combination of the following: accelerate the production and testing of motherboards (MB) once the ASIC is available, and also the assembly of cassettes; do more assembly and testing in parallel for pieces that do not require the ASIC (for the MB), or that do not require the MB, to minimize the time to complete assembly of the MB and cassettes, and to minimize the time needed to for tests.		
More details:	CMS-doc-13481		

Contributing institutions and resource optimization

Resources and optimization

Charge #4,#5

- Fermilab is the only US group with sufficient expertise and personpower for ECON design.
- All work will be done by vendors except design and testing.
- Designs for high speed I/O will be taken from lpGBT.
- Many blocks for ECON-T and ECON-D will be common.

- FNAL : ECON design and testing; ASIC design group has extensive digital design experience and 65nm experience.
  - **FNAL Engineer 1**: 20+ yrs in mixed signal design; Fermilab ASIC Dev Group lead
  - **FNAL Engineer 2** : 15+ yrs experience in ASIC industry, 14nm development, 20+ Gbps transmission
  - **ANL Engineer** : 40 years digital design experience, X-Ray pixel detectors, 3D memories, low-latency financial trading, numerous high-speed comm. protocols
  - **FNAL Engineer 3**: 5+ yrs digital design experience; recently Velopix 65nm (low power, rad tolerant, 5.12 gbps serializer/transmitter)
  - **FNAL Engineer 4**: 20+ yrs in digital design experience; recently DUNE ColdADC and ColDATA prototypes (65nm), Vipram, BTeV FPIX, FSSR readout architecture
  - **FNAL Engineer 5 :** 10+ years of mixed signals design experience
  - **FNAL Engineer 6 and 7** : extensive FPGA / PCB / system experience for test stand development.
  - **Split/FESB Engineer :** EE post doc and faculty with verilog experience

- FNAL, Florida Tech, Northwestern: ECON algorithm development and ECON testing.

Quality assurance and control

Charge #6

- Conforms to cms-doc-13093

- Quality assurance
  - Design will be based on results of extensive verification :
    - Power integrity with Cadence Voltus
    - ASIC- and system-level data integrity with SystemVerilog + UVM
  - Modular design of internal block allows simplicity of interface
  - Designs include functionality to simplify testing
  - Design process employs two prototype steps
    - Prototypes will undergo radiation and accelerated aging tests.
    - Vertical slice tests will be performed with all prototypes

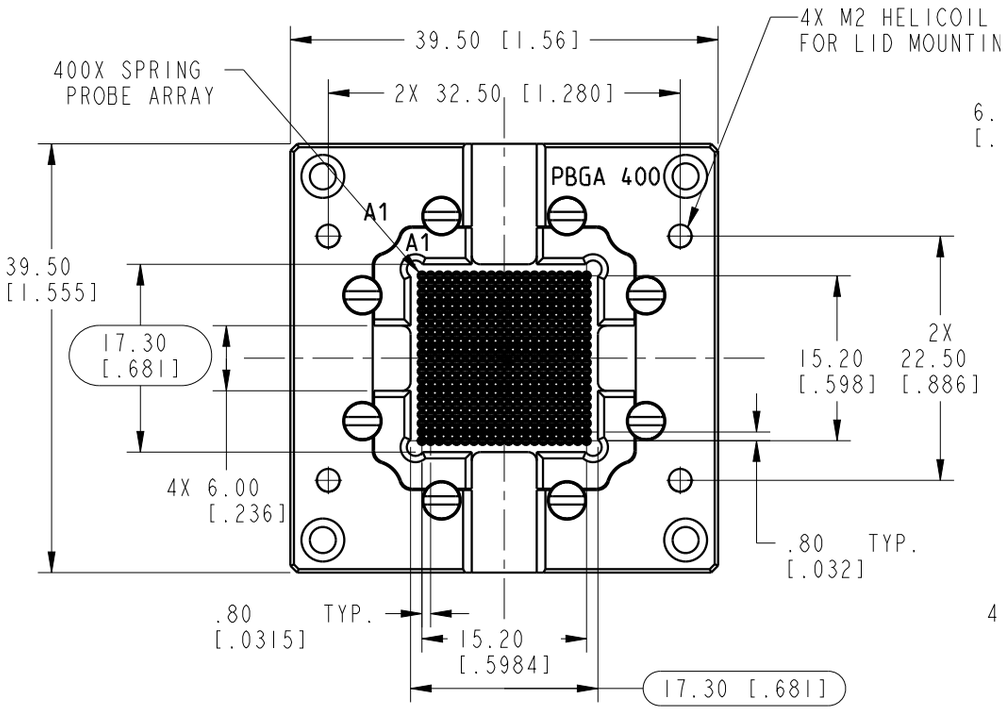
- Quality control
  - Full functionality of all ASICs will be tested with robotic ASIC tester.
  - Sample of production run will undergo radiation and accelerated aging tests.

ECON testing

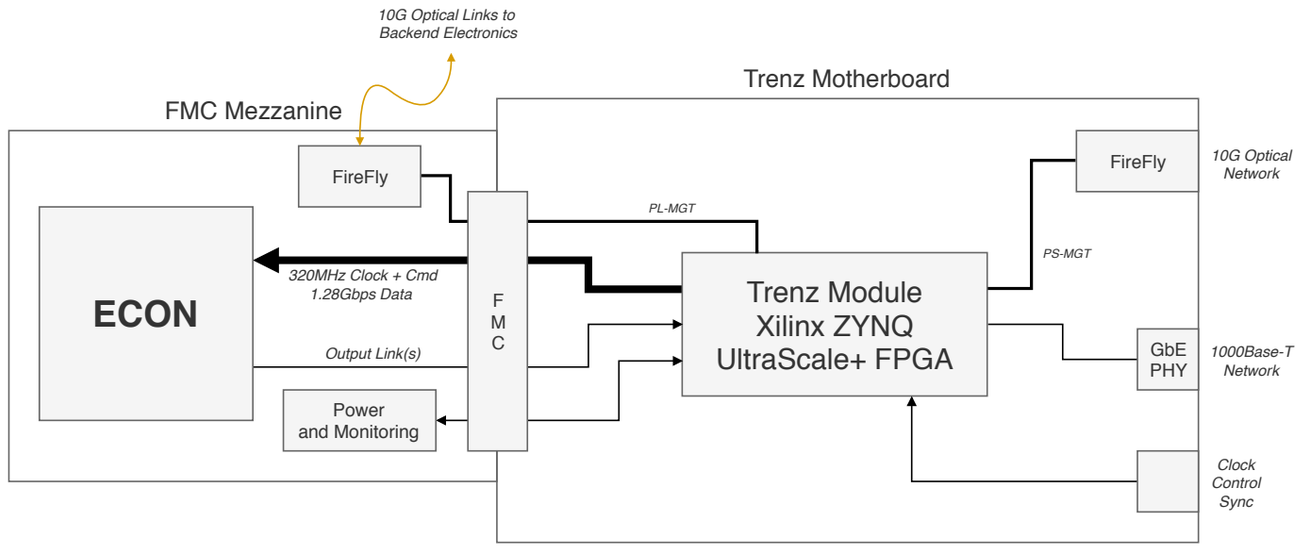
Charge #6

- Prototype / single chip evaluation
  - Must be ready to test ECON p1 immediately in Feb 2020.
  - System based on MPSoC w/ Zynq UltraScale+ FPGA
  - Will allow standalone testing of precise timing characteristics and coarse logic-level testing.
  - Will also serve as ECON emulator in early vertical slice tests.
- Socket-based and robotic test system for 100 -10k parts
  - based on prototype test system and experience with lpGBT

Candidate socket for robotic ASIC tester

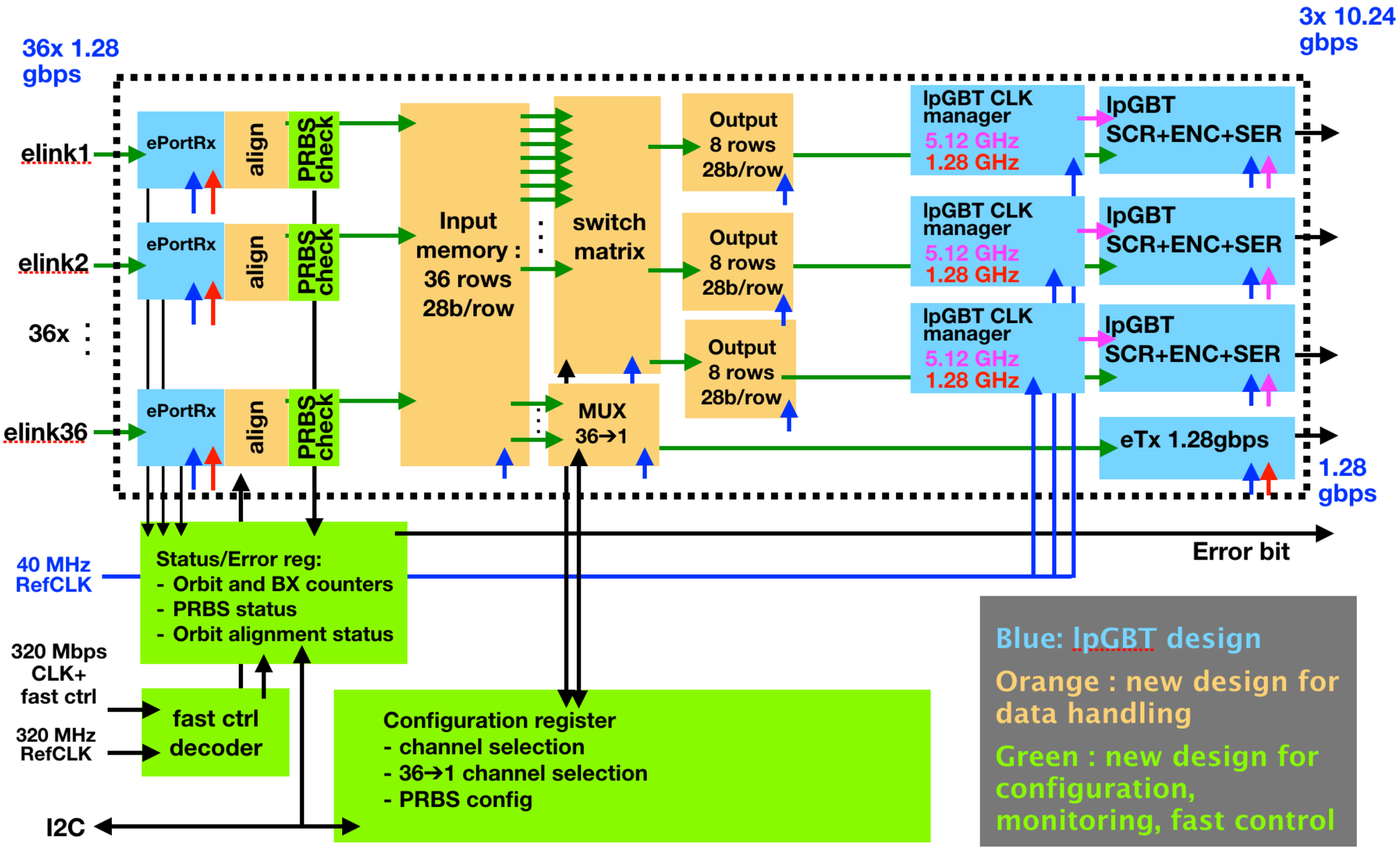


ECON TEST PLATFORM (physical)



ECON prototype 1 plan and progress

ECON p1 concept



ECON p1 engineering resources

Charge #8

- Engineering resources have been challenging to obtain.
  - Primary resource conflict is two DUNE ASICs:
    - **ColdADC submitted in October 2018** ✅
    - **ColDATA ongoing** – submission target is March 2019
- ECON team is now coming together; approximate effort in 2019:
  - FNAL 1 : **0.5 FTE**
  - FNAL 2 : **1 FTE** : joined the lab in Jan 2019
  - ANL : **0.8 FTE** : collaborator from Argonne (at FNAL 4 days/week)
  - FNAL 3 : **1 FTE** : Join ECON effort at end of March after leave.
  - FNAL 4 : **0.8 FTE** : Join ECON effort at end of March after DUNE.
  - FNAL 5 : **0.8 FTE** : Join ECON effort at end of March after DUNE
  - Split/FESB: **1 FTE** : EE post doc from University of Split / FESB with support of 1 faculty
    - Several extended trips to FNAL in 2019 – first visit Feb 17–Mar 16.
    - Direct coordination with FNAL 3
- **Effort for 2019 ECON p1 : ~7 total engineers; ~3 FTE-yrs by Aug 2019**

ECON p1 schedule and plan

Activity	Jan				Feb				Mar					Apr				May				Jun				Jul					Aug				Sep			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39
Packge/lpGBT-driven floor plan	Floor plan																	Power studies																				
ePortRx 1.28 Gbps					Simulation				Integration																													
Add Word & Orbit aligners							Verilog							synthesis with TMR, P&R, timing																								
PRBS comparator										Verilog								synthesis with TMR, P&R, timing																				
Memory and switch matrix														Verilog																								
10.24 Gbps transmitter					Simulation									Integration																								
eTx 1.28 Gbps + 1-chnl selector							Simulation							Channel selector verilog and implementation																								
Fast Ctrl + I2C decoders							Verilog											Implementation & integration																				
Configuration register							Verilog											Implementation & integration																				
PRBS generator Tx														Tx from COLDATA																								
Full chip assembly																																						
Top level connectivity and verification																																						
Reviews															X												X								X			
Submission																																					X	

FNAL 3 + 7

ANL

FESB/Split

FNAL 5 +FESB/Split

FNAL 1

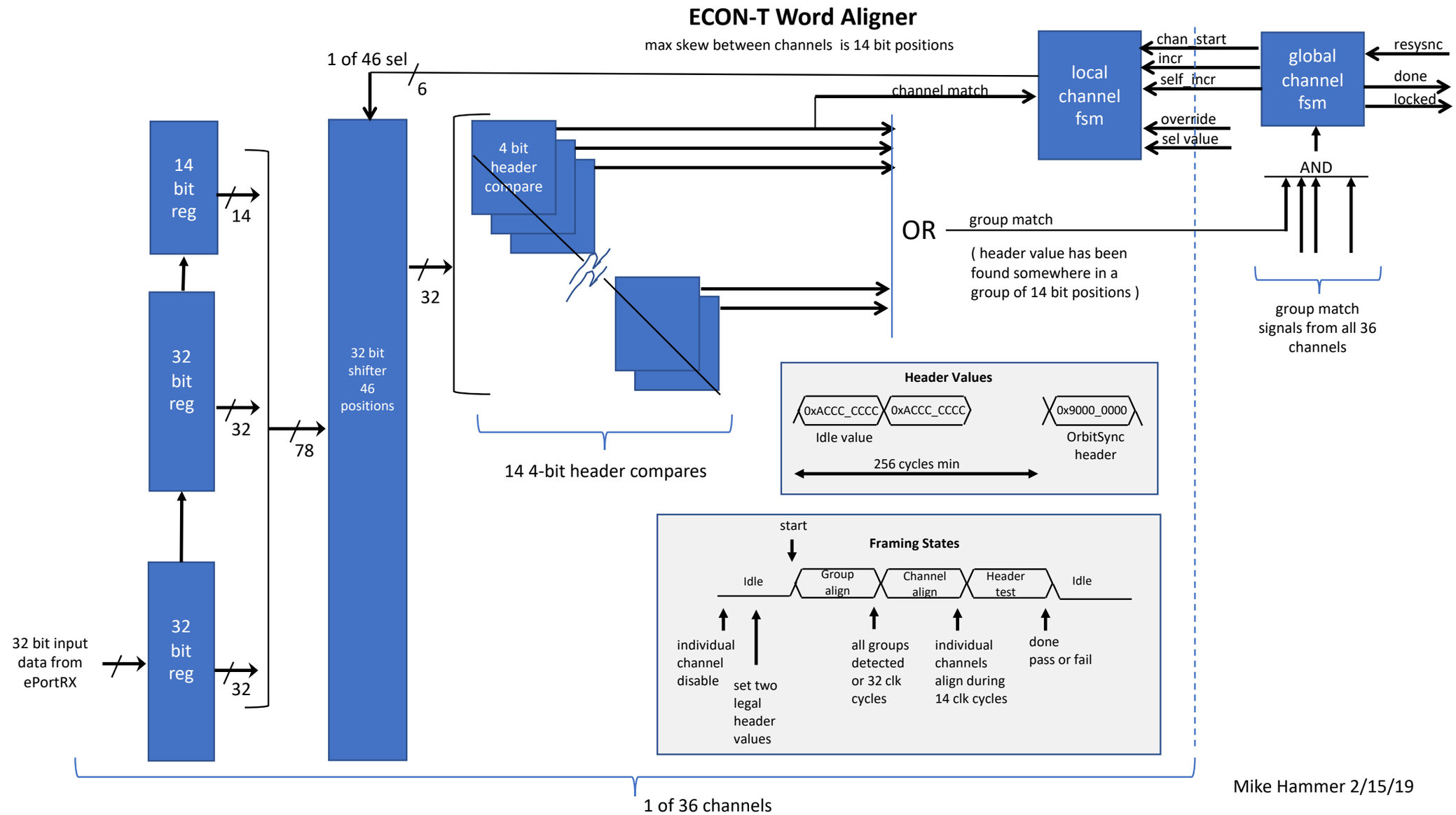
FNAL 2

FNAL 2, FNAL 3+4

FNAL 4

- Work grouped into **7 parallel activities for 7 people**
  1) Floor plan and package
  2) eRx, aligner, data handling, PRBS self test
  3) Memory and switch matrix
  4) 10.24 gbps transmitter + clock generator
  5) eTx and single channel selector
  6) Control and monitoring
  7) Top-level connectivity and verification

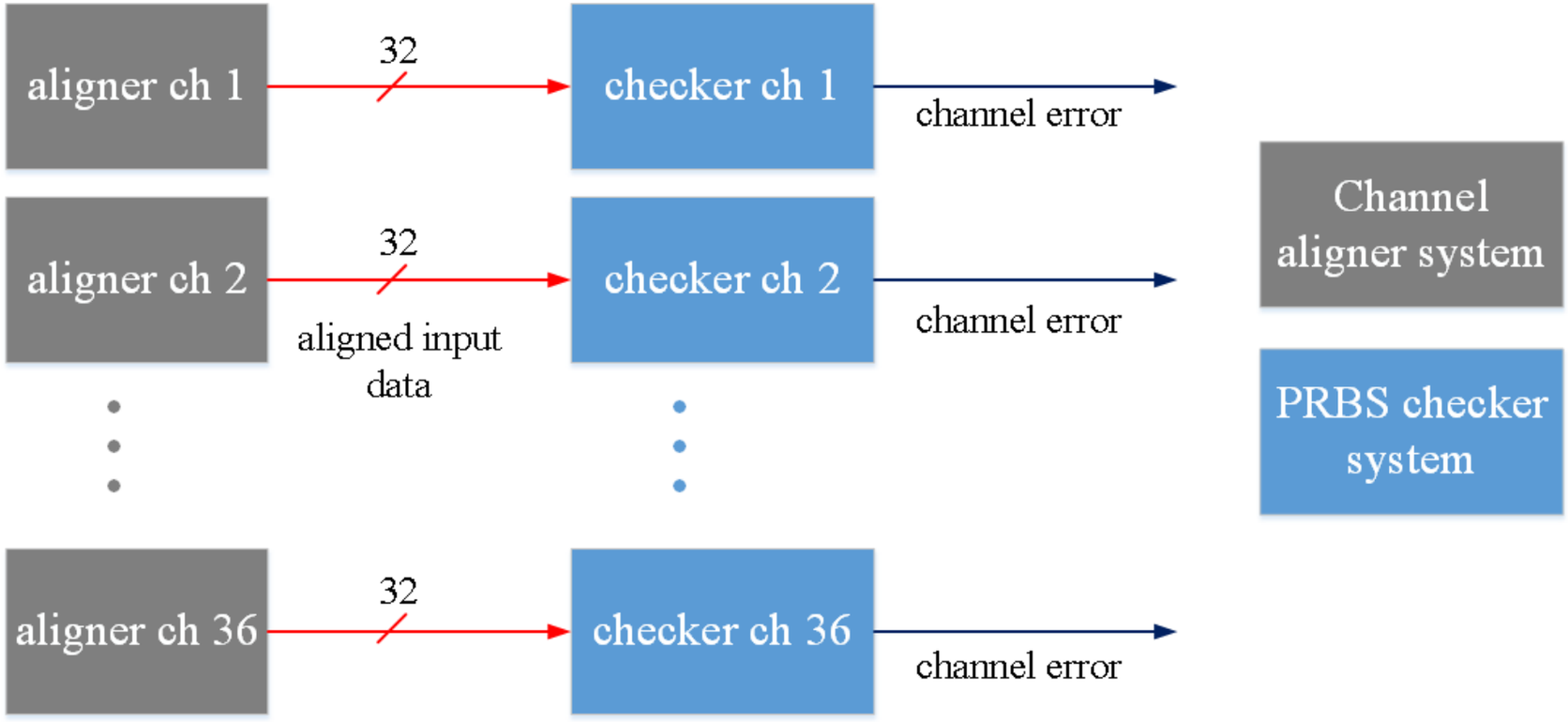
Word aligner : verilog complete



- Bit aligner included with lpGBT ePortRx
- Word aligner finds and aligns 32-bit words for all elinks
- Assumes skew b/w elinks of ≤ ±7 1.28G clocks
- Next step: verilog for counting and monitoring LHC orbit sync signals

PRBS15-based BIST : verilog complete

- Built In Self Test for ePortRx
- Off-ECON test system generates separate PRBS15 for each input elink.
- Each of 36 aligners passes data to checker in "pass through" mode
- Following basic PRBS usage:
  - Entire $2^{15}-1$ pseudorandom binary sequence can be generated from first 15 bits.
  - Use first bits to generate PRBS for comparison
  - Try again in case of initial failure



Reviewers' question

EndCap Calorimeter: Critical path for HGCal goes through the ECON ASIC development at this time, with only 3.5 months float to need-by-date. This part of the project is at least 1 year late based on the milestones in the Monthly report forecasts. Given this history, what is the project plan to keep this section of the project from slipping more and threatening the need-by-date?

The reasons for the delay were (a) lack of availability of lpGBT designs and (b) the lack of engineering resources at Fermilab. Item (a) is no longer a concern because lpGBT designs were transferred to the ECON team in September 2018. Item (b) has been mitigated by bringing new engineering resources to the project: (i) hiring a new ASIC designer with 15+ years experience, (ii) recruiting an ASIC engineer from a nearby lab, and (iii) hiring a new co-leader for the Fermilab ASIC Development Group to free some of the time of the current group leader for ECON ASIC design. In addition, the two DUNE ASICs that also require ASIC engineer effort have been or will soon be submitted freeing more effort for ECON development.

What is to prevent additional delays?

The largest risk for additional delays now are lack of clear specifications, so the team is working to clarify and finalize outstanding details of the specification. We now have a plan for parallel design of individual blocks, which allows efficient employment of a large team.

How will delays impact the rest of the schedule?

Refer to Gantt chart on next slide.

Reviewers' question

Red activities denote the critical path

Long Shutdown 3

Aug 2023: Cassettes delivered to CERN

has 3.5 months of float to:

Dec 2023: CMS requests-by date

Plus 8.6 months float

In iCMS master schedule

Threshold KPP: T-KPP-CE-1

Oct2023: Endcap Calorimeter Construction Complete

Summary

- ECON is needed to manage transmission of data off detector.
- ECON design maturity has advanced beyond conceptual level.
  - Basic components based on mature lpGBT design.
  - Verification based on extensive DUNE experience
- ECON design methodology and philosophy chosen to
  - maximize efficiency, minimize errors, simplify testing
- Initially challenging to identify resources, but team is making rapid progress since ramping up in late January 2019.
- Cost, schedule, and risks are understood.

Additional material

Trigger algorithm

Charge #2

- Significant progress made on understanding trigger algorithm performance.
- **Most important question**: can system meet requirements with simple algorithm?
- Compare variety of algorithms:
  - threshold algo : apply simple E_T thresholds to TRG cells
  - sorting algo : sort TRG cells to readout highest energy preferentially
  - super trigger cells : combine adjacent TRG cells and readout all

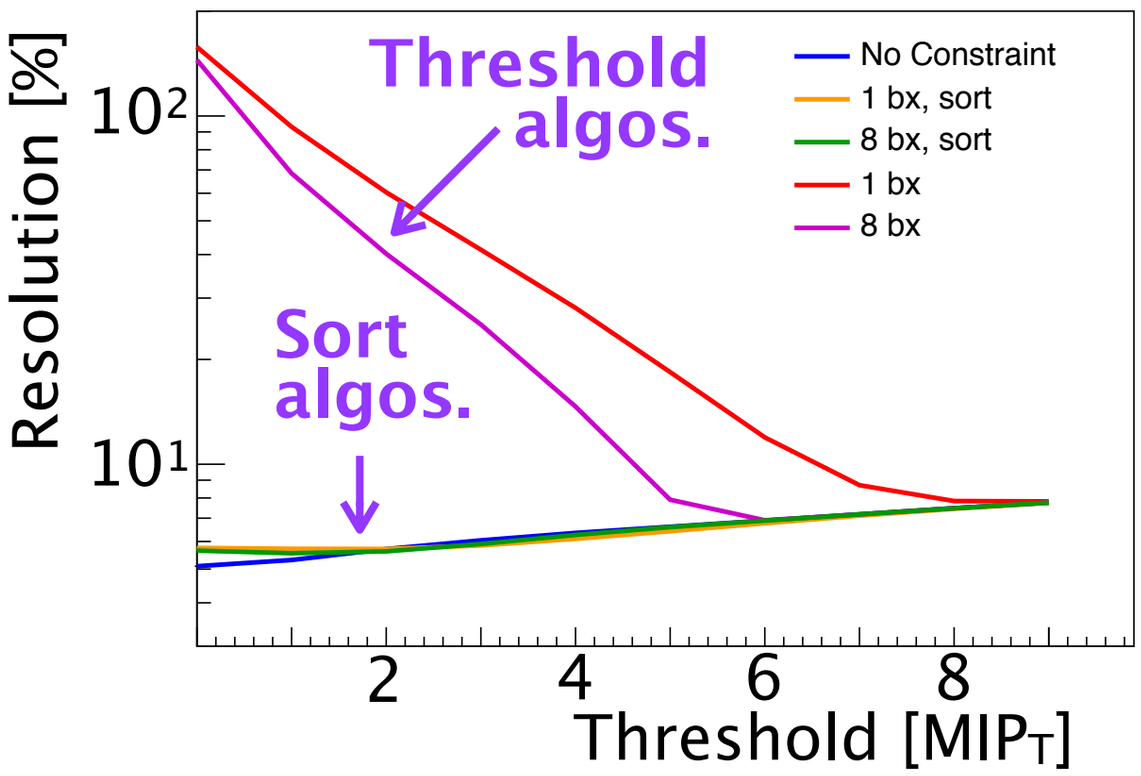
Compare 5 scenarios:

- **No constraint** : readout all trigger data above threshold
- **Unsorted** (1 or 8bx): readout data in order received until bandwidth limit reached
- **Sorted** (1 or 8bx): sort data by energy and readout until limit reached

Conclusion:

- Best resolution ~ 5%.
- Threshold-based algo achieves ~7% resolution for 6 GeV threshold.

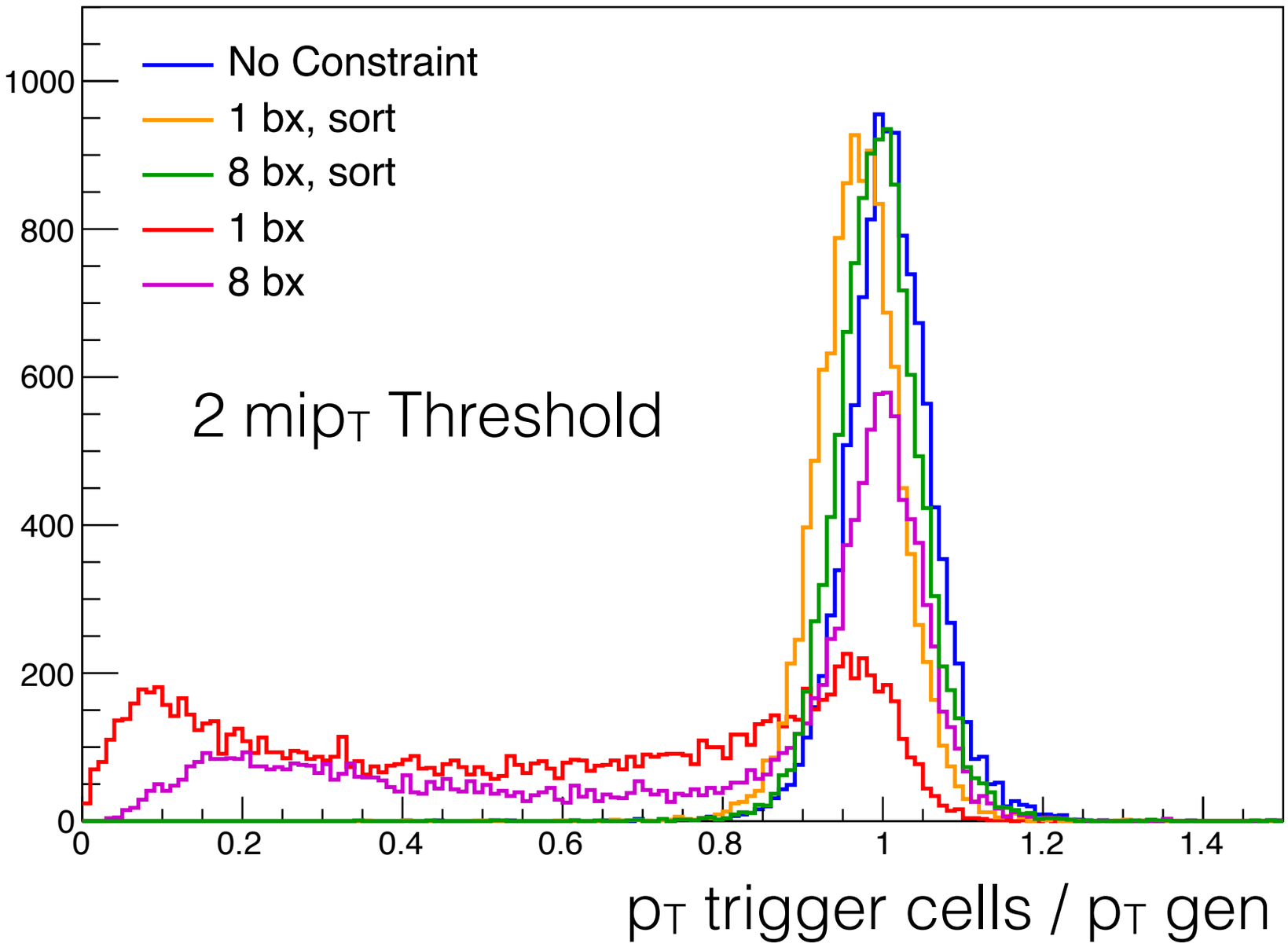
25 GeV electrons
inner detector, CE-E layer 8



Trigger algorithm

Charge #2

- Resolution plot for 2 MIP_T threshold choice for 5 trigger algorithm scenarios.



Compare costs for Feb 2019 schedule

Charge #3

- RLS in official CD-1 DR documentation:

Activity ID	Activity Name	Start	Finish	Planned Duration	Planned Total Cost	Planned Labor Units	Remaining Nonlabor Units
402.4W-Status-FY19.7	CE - Electronics and Services	01-Aug-18 A	02-Jan-24	1358.0d	$6,534,078.14	2014d	1668d
402.4W-Status-FY19.7.1	CE - Concentrator ASIC	01-Aug-18 A	09-Jun-22	967.0d	$4,610,732.30	2014d	1373d

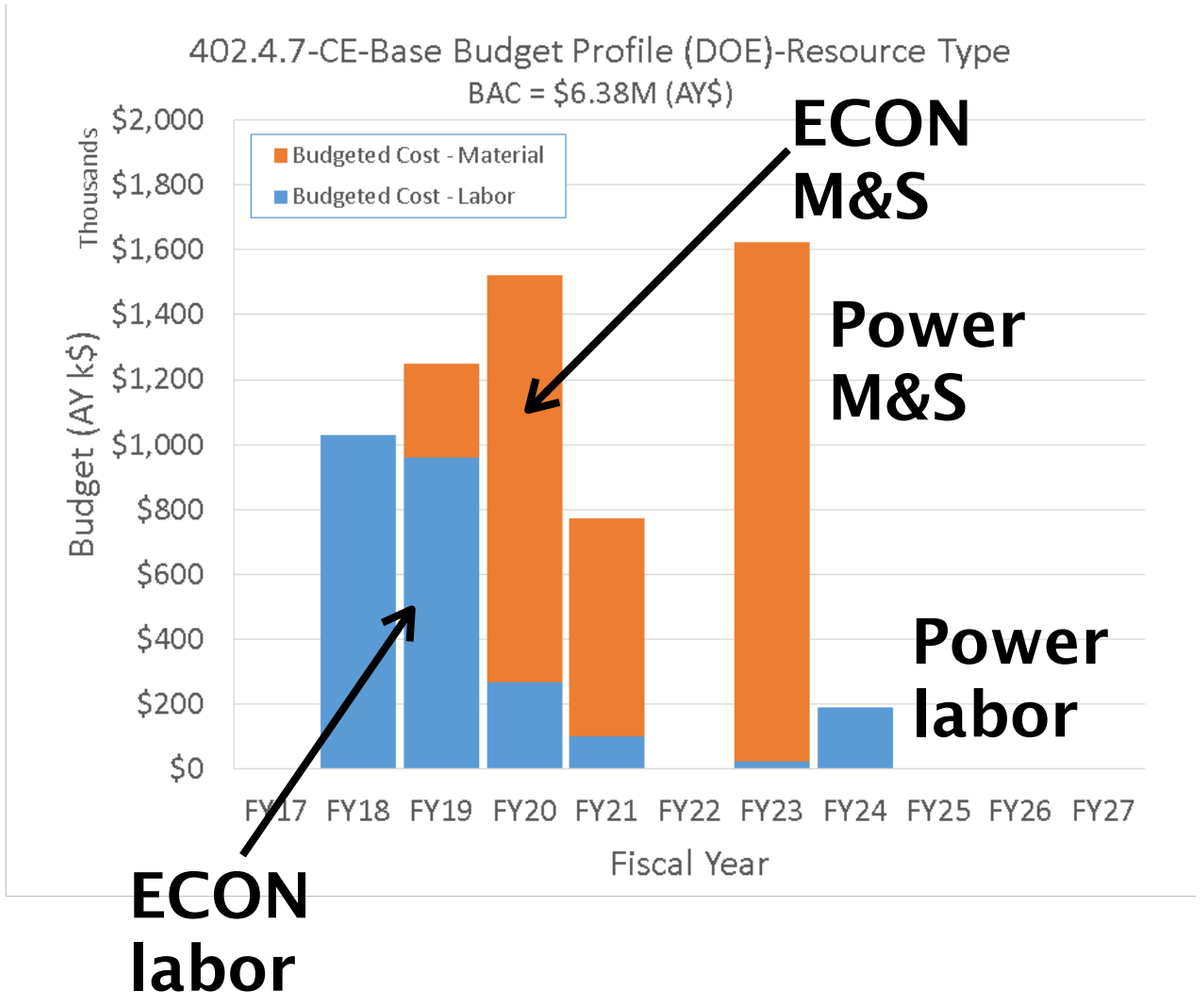
- RLS based on Feb 2019 ECON work plan that will be implemented before CD-1 review in June 2019:

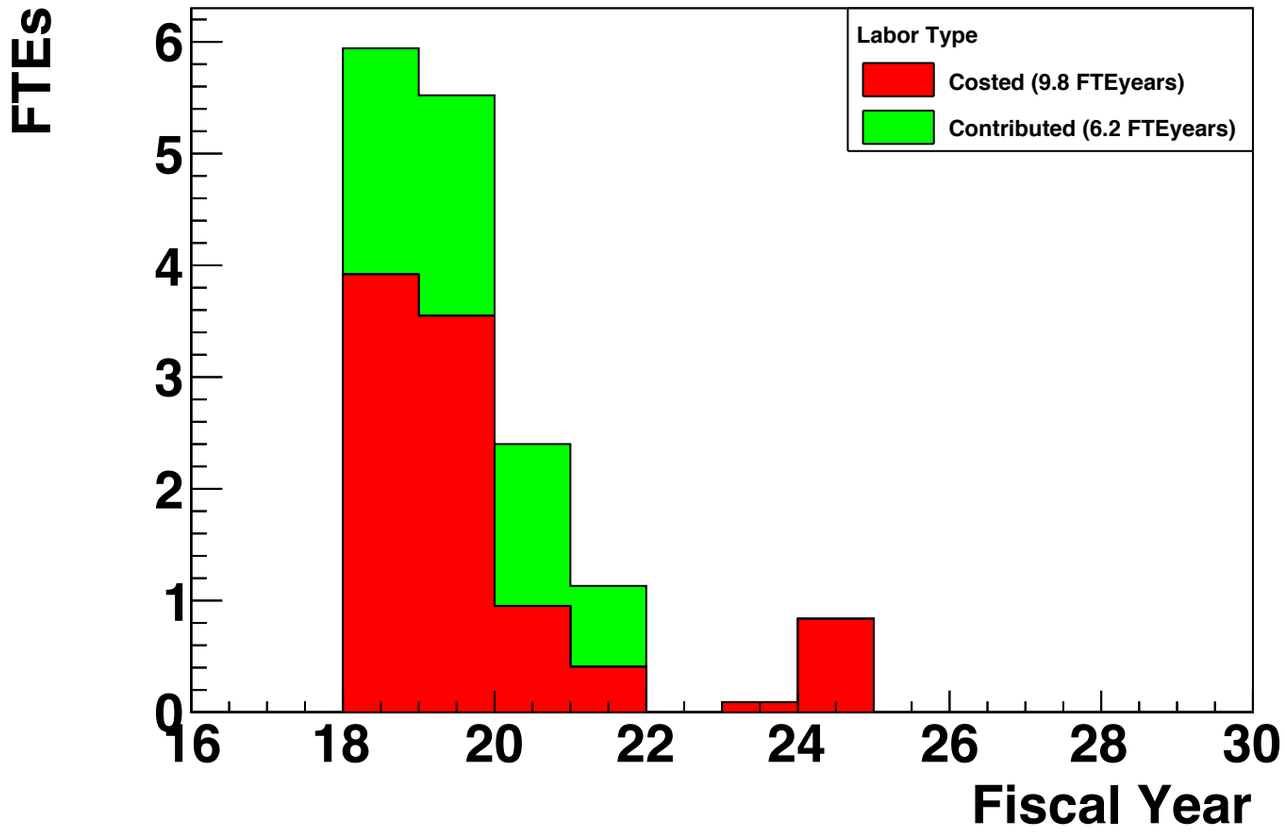
Activity ID	Activity Name	Start	Finish	Planned Duration	Planned Total Cost	Planned Labor Units	Remaining Nonlabor Units
402.4W-sandbox.7	CE - Electronics and Services	01-Mar-19	02-Jan-24	1214.0d	$6,584,523.57	2001d	1628d
402.4W-sandbox.7.1	CE - Concentrator ASIC	01-Mar-19	05-Apr-22	777.0d	$4,574,908.89	2001d	1333d

Cost profiles

Charge #3

- Cost drivers indicated on cost profile.
- Contributed labor is for ECON testing, algorithm development, and power system testing.
- These profiles are from CD-1 June 2018 -- amounts are the same, but dates are later.

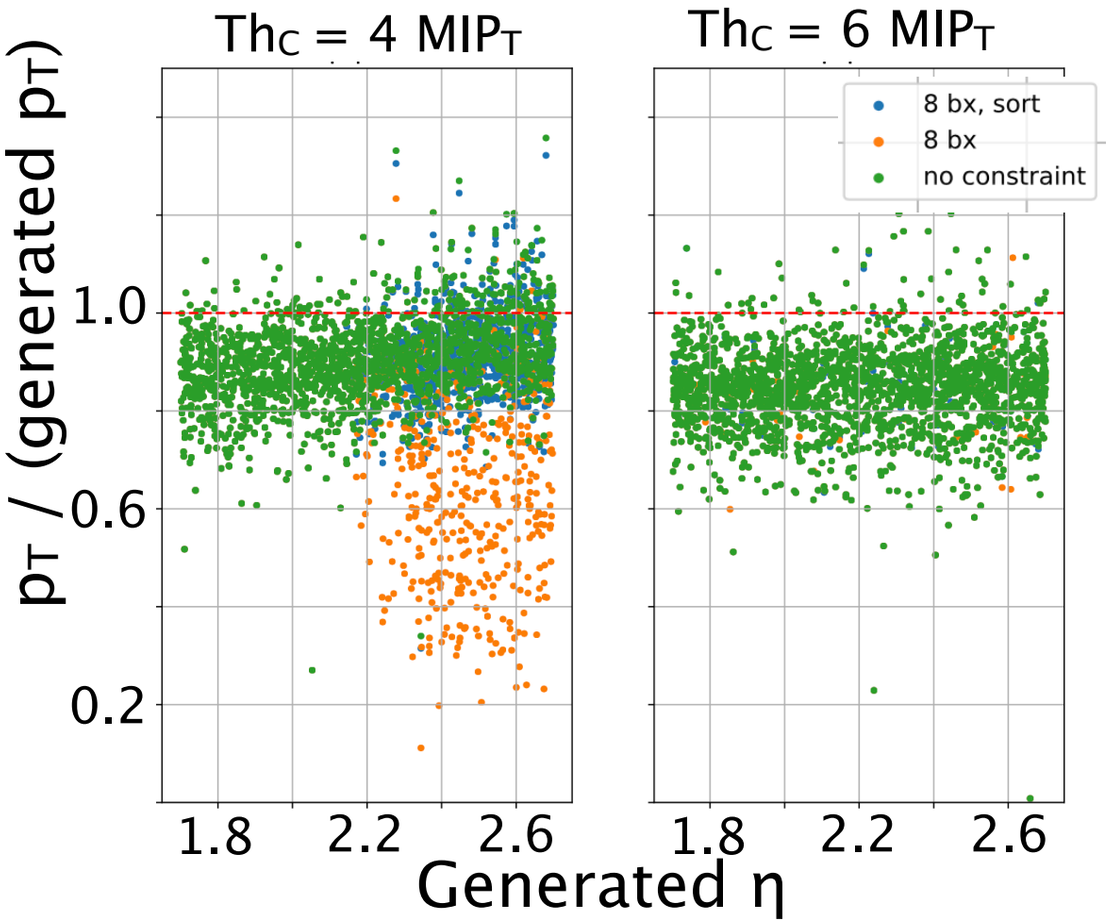


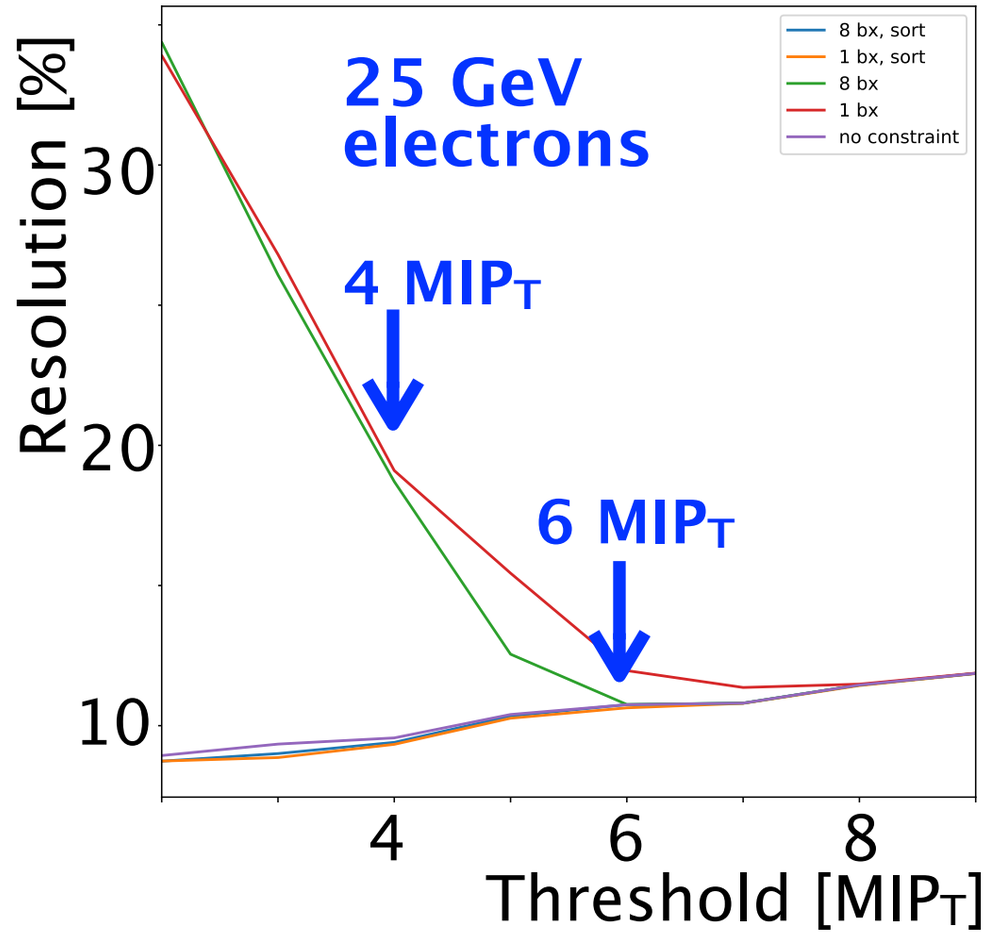


Trigger algorithm

Charge #2

- How does critical threshold for reaching sort performance depend on detector η?





Radiation requirements

Charge #2

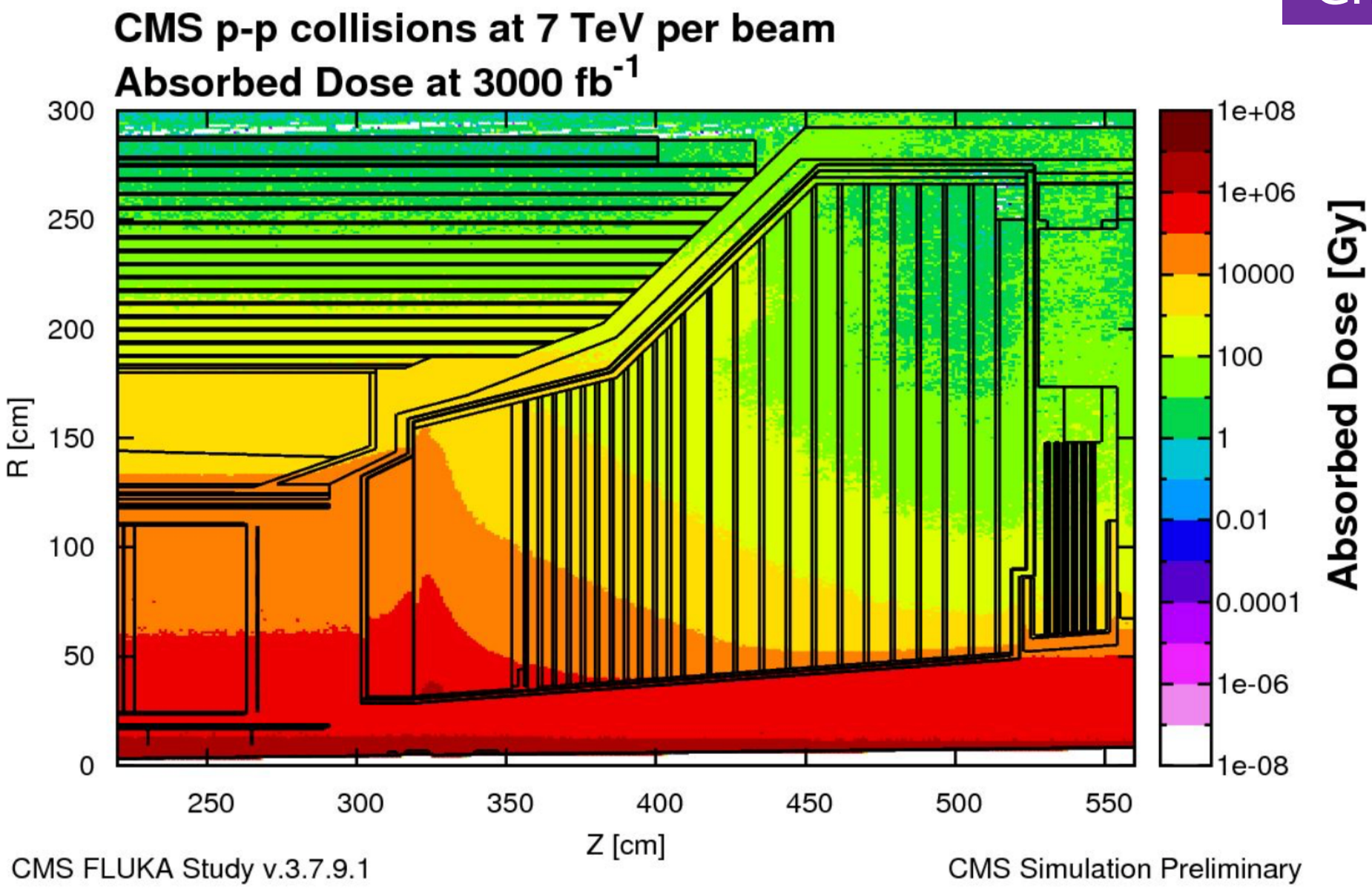


Figure 1.1: Dose of ionizing radiation accumulated in HGCAL after an integrated luminosity of3000 fb^{-1}, simulated using the FLUKA program, and shown as a two-dimensional map in the radial and longitudinal coordinates, r and z.

Radiation requirements

Charge #2

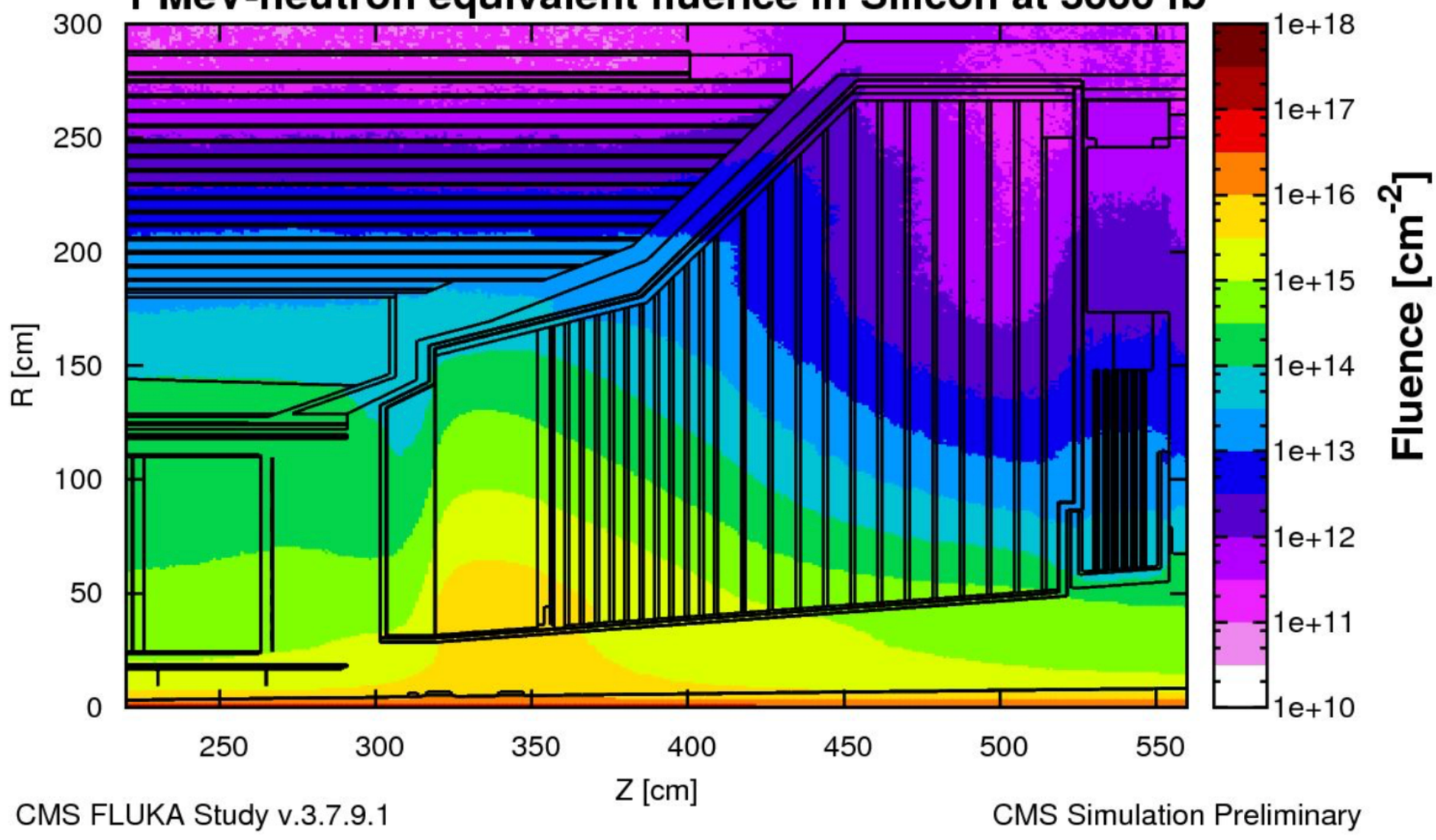


Figure 1.2: Fluence, parameterized as a fluence of 1 MeV equivalent neutrons, accumulated in HGCAL after an integrated luminosity of3000 fb^{-1}, simulated using the FLUKA program, and shown as a two-dimensional map in the radial and longitudinal coordinates, r and z.

Resources and optimization

Charge #4,#5

- Fermilab is the only US group with sufficient expertise and personpower for ECON design.
- All work will be done by vendors except design and testing.
- Designs for high speed I/O will be taken from lpGBT.
- Many blocks for ECON-T and ECON-D will be common.

- FNAL : ECON design and testing; ASIC design group has extensive digital design experience and 65nm experience.
  - **Gregory Deptuch** : 20+ yrs in mixed signal design; Fermilab ASIC Dev Group lead
  - **Ralph Wickwire** : 15+ yrs experience in ASIC industry, 14nm development, 20+ Gbps transmission
  - **Mike Hammer (Argonne National Laboratory)** : 40 years digital design experience, X-Ray pixel detectors, 3D memories, low-latency financial trading, numerous high-speed comm. protocols
  - **Sandeep Miryala** : 5+ yrs digital design experience; recently Velopix 65nm (low power, rad tolerant, 5.12 gbps serializer/transmitter)
  - **Jim Hoff** : 20+ yrs in digital design experience; recently DUNE ColdADC and ColDATA prototypes (65nm), Vipram, BTeV FPIX, FSSR readout architecture
  - **Farah Fahim:** 10+ years of mixed signals design experience
  - **Jamieson Olson and Paul Rubinov** : extensive FPGA / PCB / system experience for test stand development.
  - **Ante Kristic and Duje Coko (Split/FESB) :** EE post doc and faculty with verilog experience

- FNAL, Florida Tech, Northwestern: ECON algorithm development and ECON testing.

Design maturity

Charge #1,#2#,7

- Documented in cms-doc-13417**
- ECON conceptual design is complete
  - ECON selected over lpGBT-based alternative based on value engineering principles.
  - R&D plan understood and on track.
  - Risks determined and documented.
- ECON preliminary design in progress
  - Interfaces identified
  - Development of QA plan in progress : currently developing hardware/ software for evaluating performance of 1st prototype.

ESH

Charge #6

- All ES&H aspects of the HL LHC CMS Detector Upgrade Project will be handled in accordance with the Fermilab Integrated Safety Management approach, and the rules and procedures laid out in the Fermilab ES&H Manual (FESHM).

- We are following our Integrated Safety Management Plan (cms-doc-13395) and have documented our hazards in the preliminary Hazard Awareness Report (cms-doc-13394).

- In general, safety is achieved through standard Lab/Institute practices
  - No construction, accelerator operation, or exotic fabrication
  - No imminent peril situations or unusual hazards
  - Items comply with local safety standards in site of fabrication and operation
  - Site Safety officers at Institutes identified in the SOW

- Specific hazards are ionizing radiation during ASIC testing and mechanical hazards during operation of robotic ASIC tester.