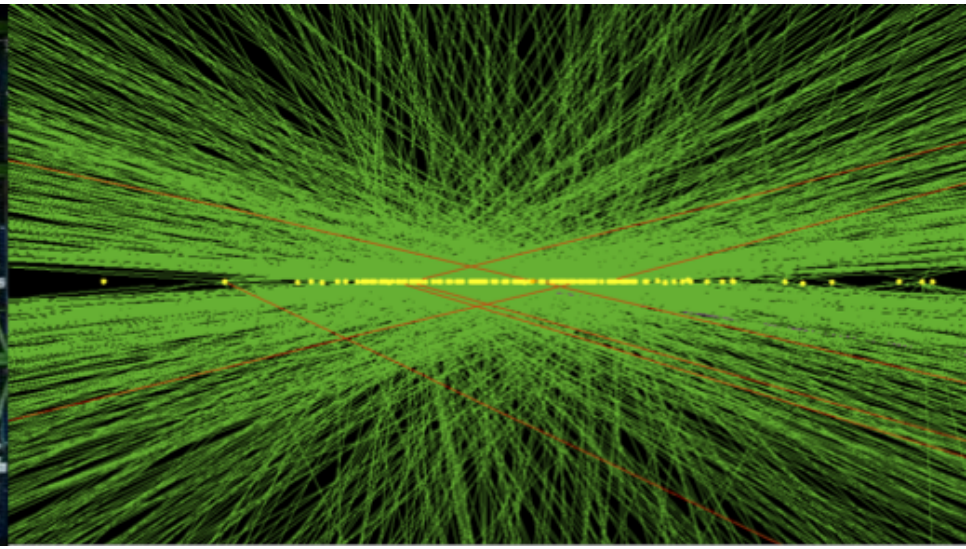
402.2 Test Systems and QC

Anadi Canepa, Yuri Gershtein

CD1 Director's Review

March 20, 2019



Outline

Overview of technical progress since the June 2018 IPR review

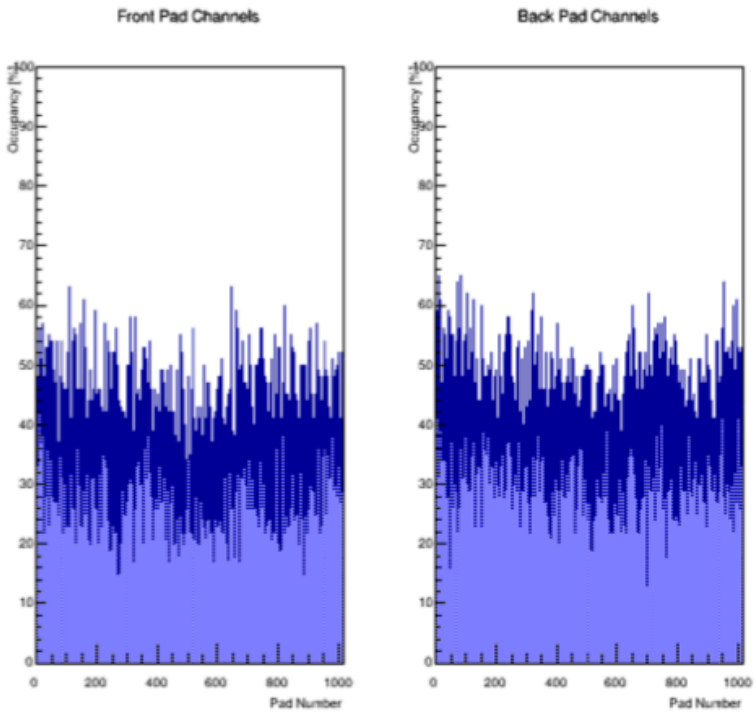
- 402.2.4.2 Test Systems
  - Hybrids
  - Modules
  - MaPSA
- Testing Campaigns
- Summary

Test Systems: Hybrids (1)

- USCMS has agreed to contribute to the testing of the prototype hybrids shipped to CERN prior to distribution to the assembly sites
- The task includes the development of the test system, the development of the QC SW, the development of the QC protocol, and the qualification of devices
  - 8CBC2 hybrids have been qualified (electrically and thermally) and distributed in early January 2018
    - Utilized by the various module assembly centers to build the first functional 8CBC2 modules (outside CERN)
  - 8CBC3 hybrids are being qualified now
    - To be distributed soon

Test Systems: Hybrids (2)

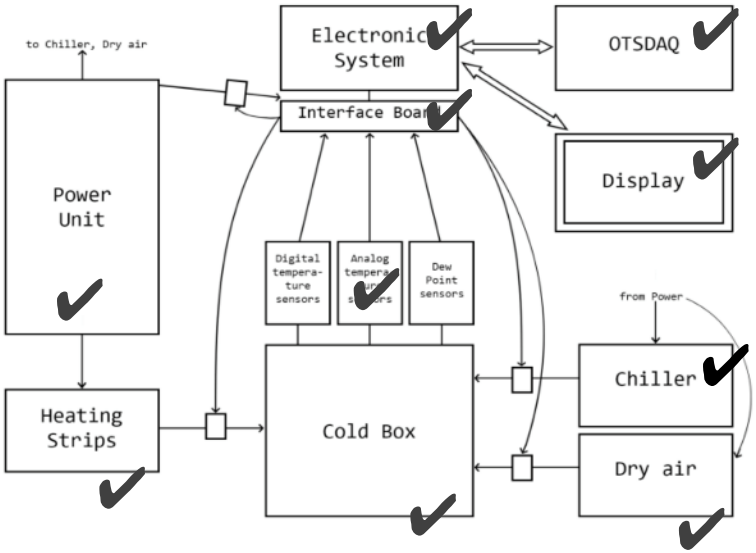
- 10 Test 8CBC3 hybrids were delivered to CERN in late 2018
  - Based on the FR4 stiffeners instead of CF stiffeners
- The test setup was upgrade from the GLIB to the FC7 technology and the UIB (universal interface board) tested
- Electrical characterization includes: monitoring of power consumption, I2C communication with ASICs, register read/write tests, inspection for shorts, inspection for open channel with antenna, calibration, measurement of occupancy after calibration, count of read-back errors



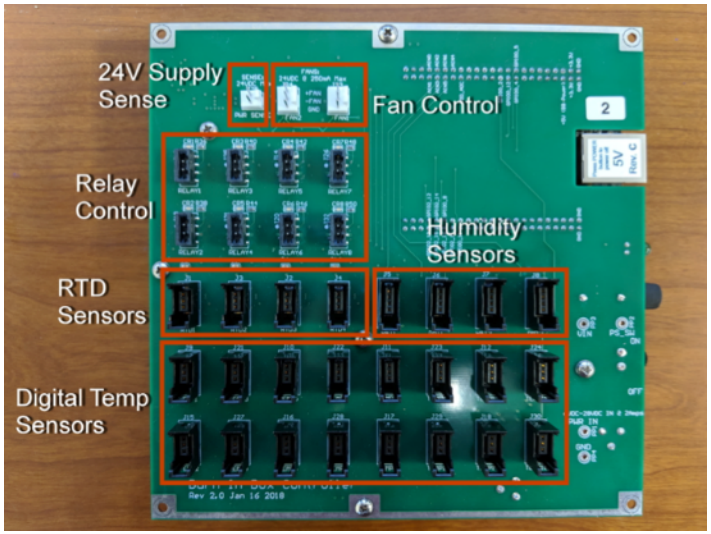
- Current batch does not exhibit any problem
  - Except for Chip 6 on each hybrid (issue at vendor, understood)

Test Systems: Modules (1)

- USCMS is responsible for designing the module burn-in station for long term tests
- 10 modules will be cycled through room- and the operating-temperature and electrically tested
- Assumptions: power, max 100W; operating temperature, -35deg; modules on carriers; final configuration of LV/HV/Optical readout; system runs un-attended

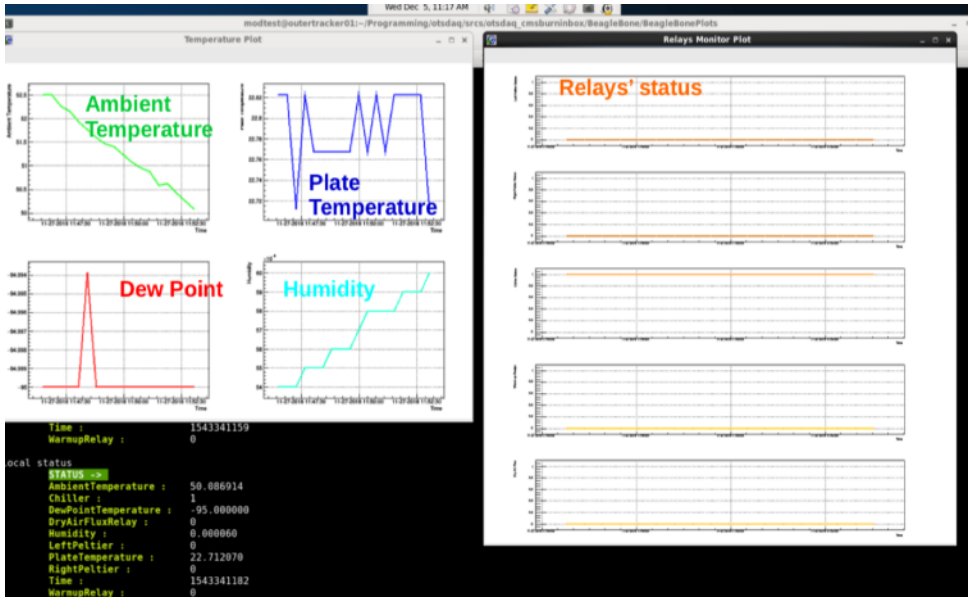


- The monitoring SW runs on the BeagleBone Black board communicating with sensors through dedicated interface card (designed by USCMS, shown on the right)
- The control SW is interfaced to OTSDAQ. It can also run standalone



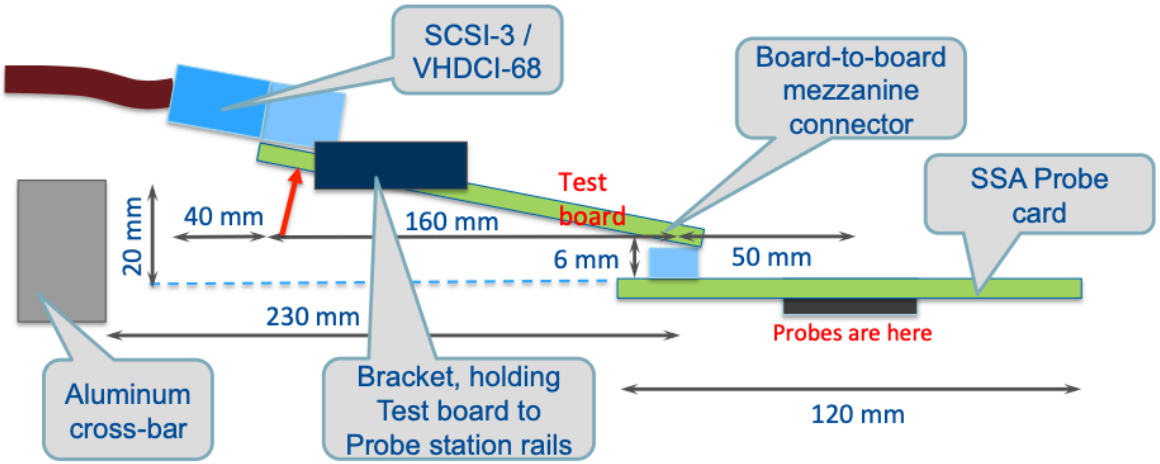
Test Systems: Modules (2)

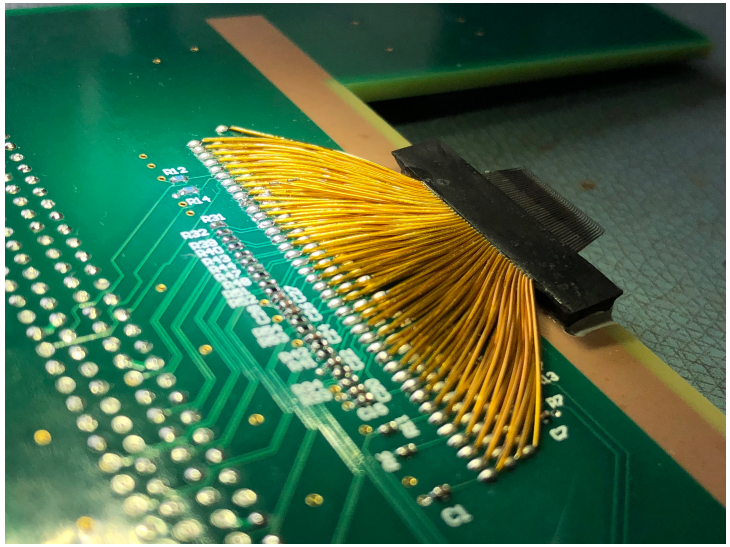
- The prototype burn in system was built by the June 2018 review and used to optimize the design in view of the final version
- The final system is in place (available: thermally insulated enclosure, chiller, cooling system, module support structure, beagle bone black and interface card, control SW)
- The system has been tested with a load of 80W: performance meets requirement with ample margin



Test Systems: MPA/SSA Overview

- USCMS is responsible for the design of the test system for MaPSA (including R&D on MPA/SSA test systems)
- USCMS designed the probe and interface cards to test the MPA/MaPSA and the SSA
  - MPA/MaPSA, production complete; cards in use
  - SSA probe cards production complete; shipped to other centers

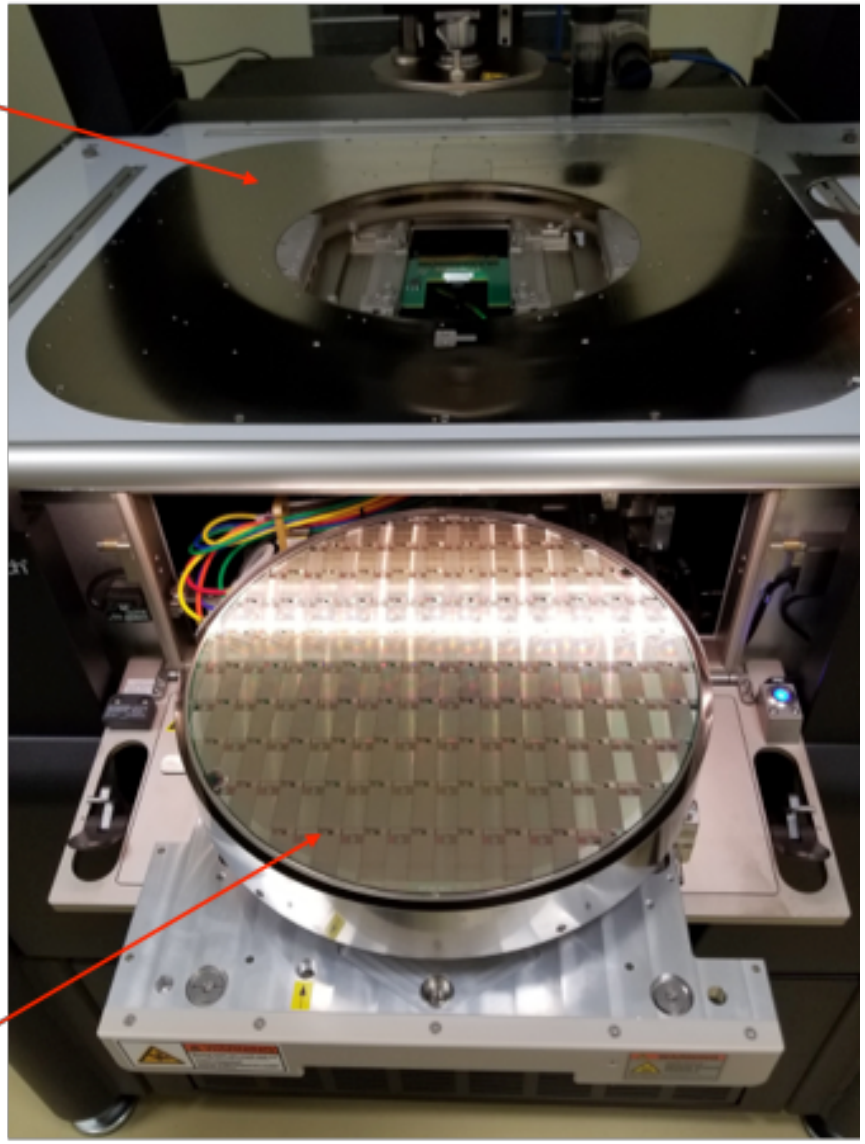




Test Systems: MPA (1)

Cascade Microtech Probe Station (similar to the one use at FNAL for MPA-light probe card tests)

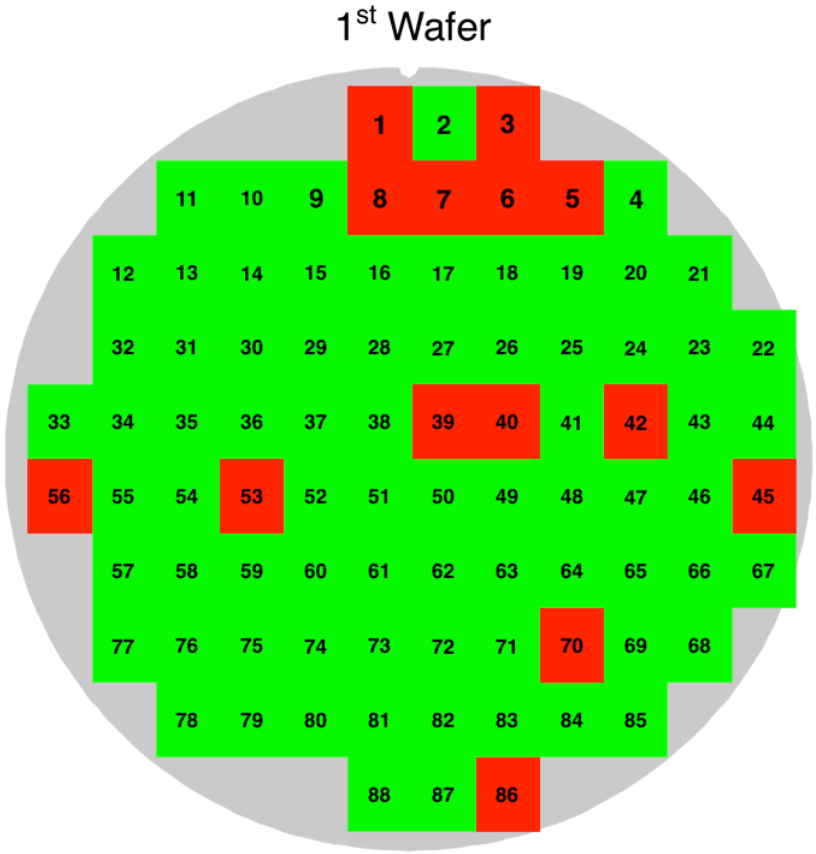
- The first MPA Wafer probing took place at CERN with USCMS personnel carrying out the testing
  - Categorization of individual MPAs on the 12 inch wafer
  - Identification of faulty chips (for multiple failure modes)
  - Collection of information about each chip
  - Comparison to performance of bump-bonded chips

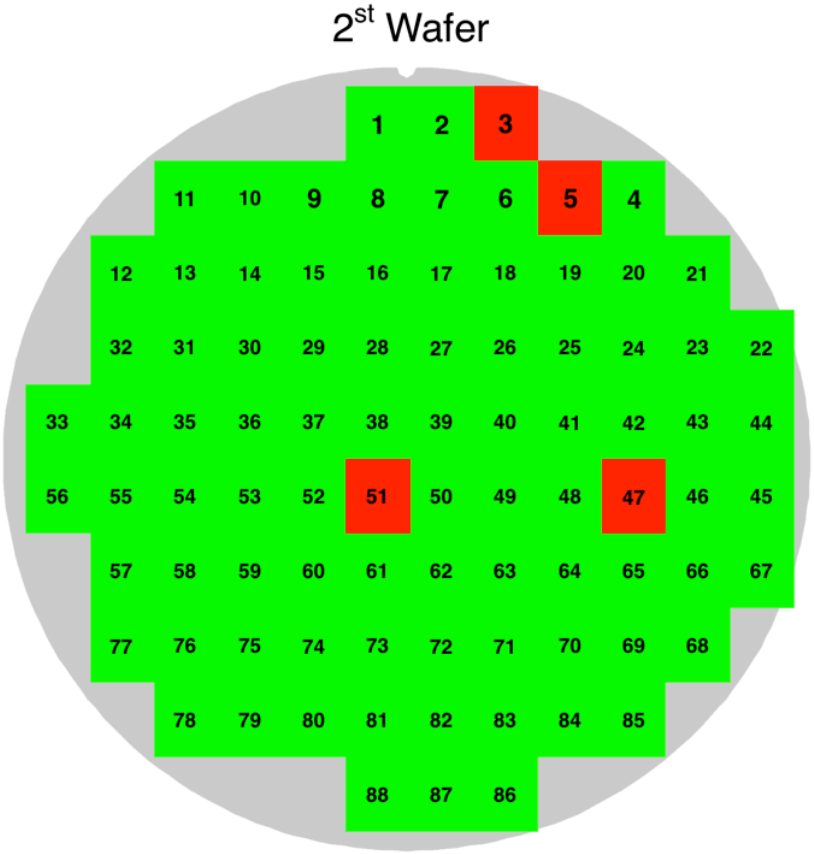


12" wafer with 88 functional MPAs

Test Systems: MPA (2)

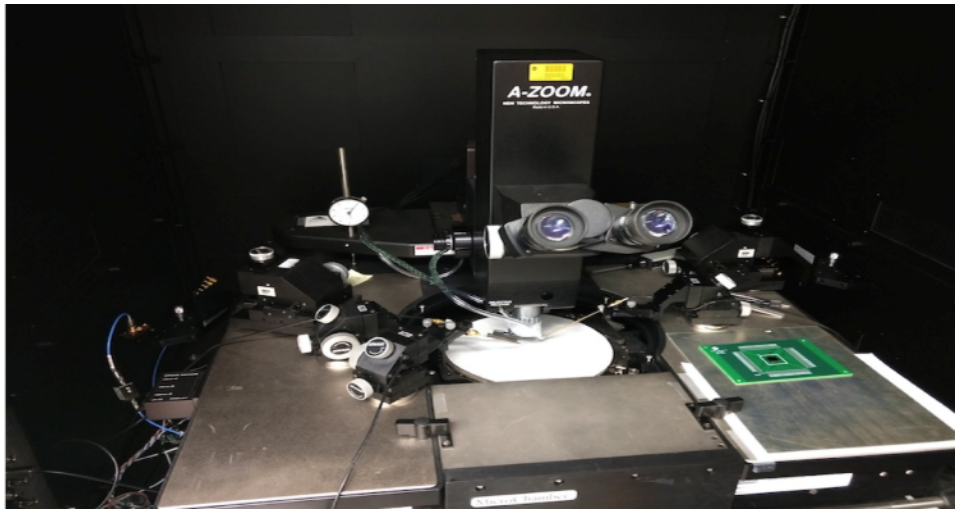
- Results (from ~10 wafers tested)
  - High efficiency for good chips

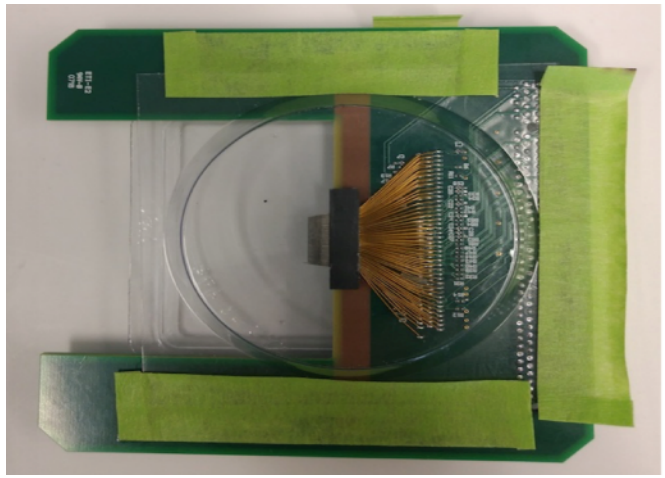


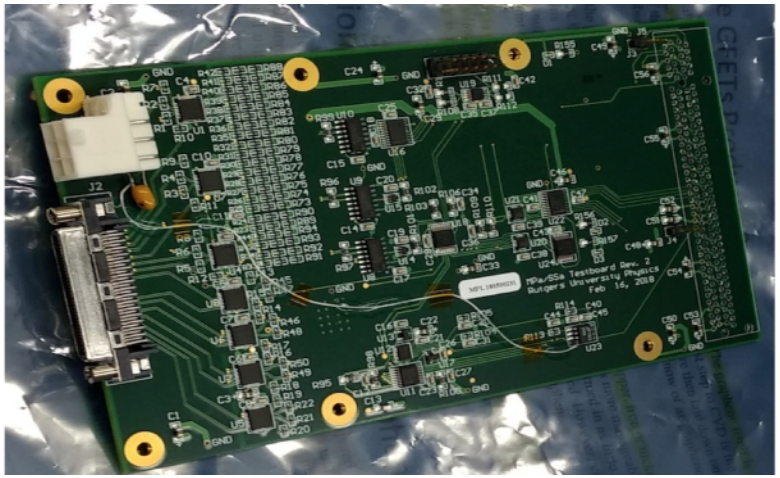


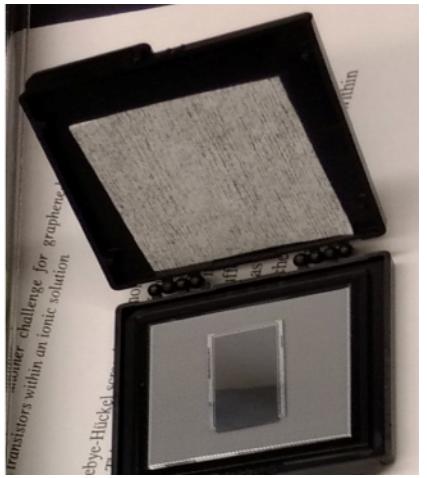
Test Systems: MaPSA

- A test setup is being assembled at Fermilab
  - Functional MaPSAs are expected to be delivered shortly







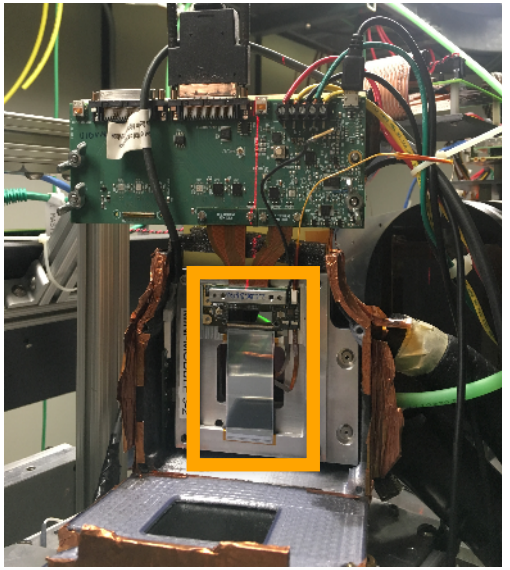


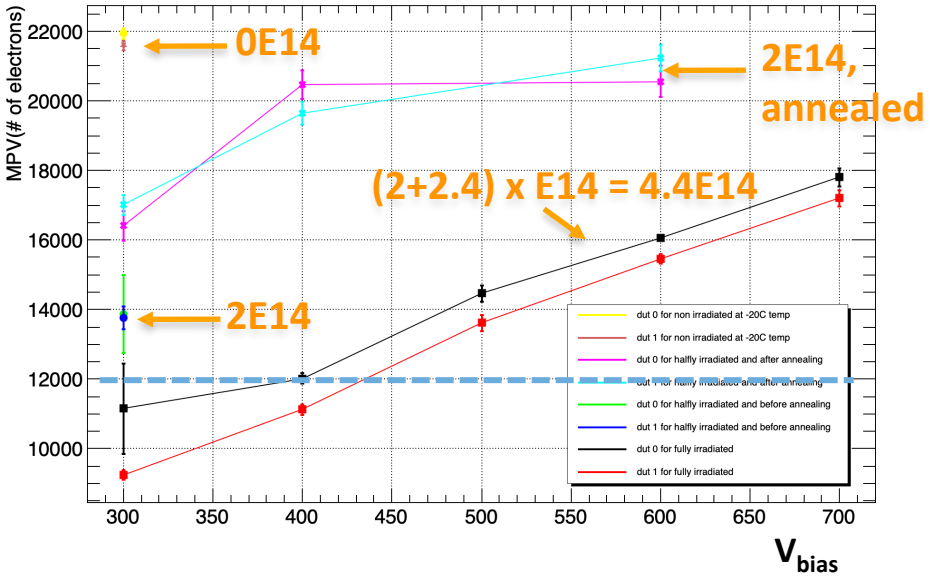
Characterization of Prototypes

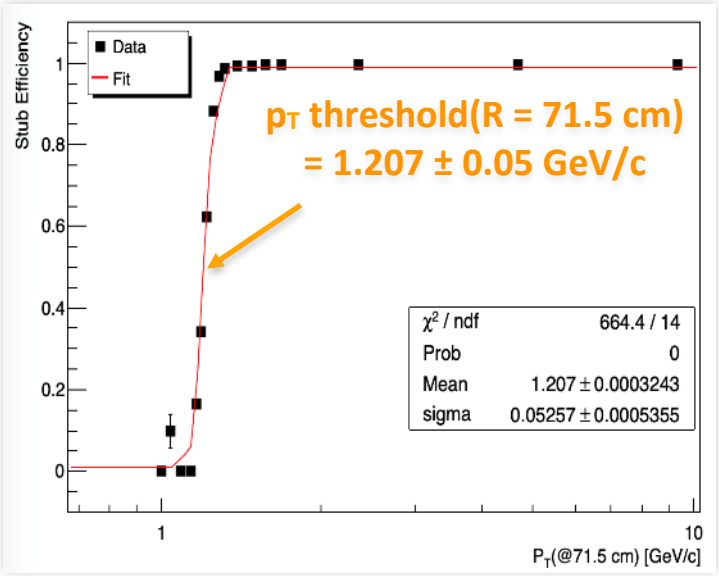
- Since the June 2018 review (when results from the 2CBC2, MaPSA-Lite and 8CBC2 modules where presented), USCMS has tested new prototypes:
  - 2CBC3 minimodule
  - Baby MaPSA
  - 2xSSA minimodule

Characterization of Prototypes (1)

- USCMS tested in beam the first 2CBC3 minimodule built by CERN
- The mini module was tested before irradiation, after irradiation and before/ after mechanical stress
- Full efficiency reached after the total fluence expected for the HL-LHC 2S tracker.





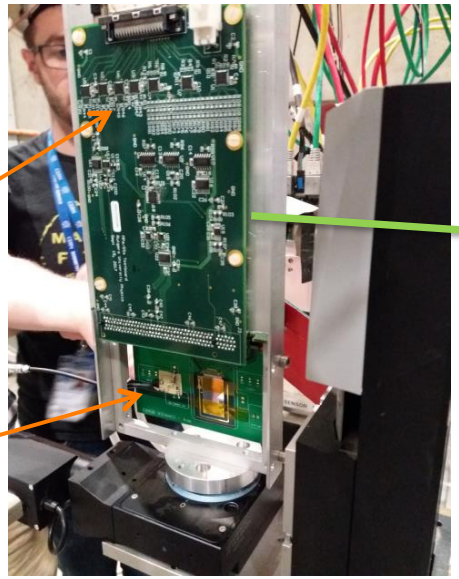


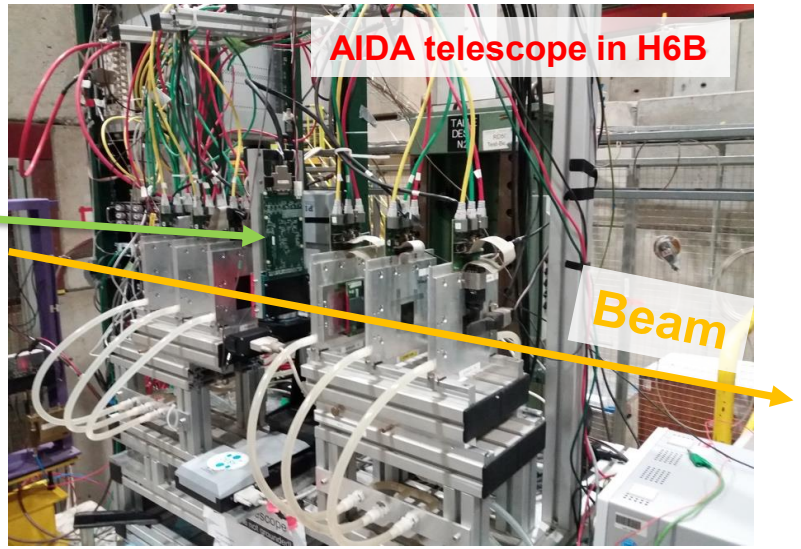
Characterization of Prototypes (2)

- USCMS contributed to the testing of the first PS-like device under beam at CERN
  - Baby MaPSA devices gold-stud-bonded at KIT
- The apparatus included
  - CERN H6 test beam with AIDA telescope
  - Electronics and DAQ from the US
  - Firmware from US, CERN and DESY

Same interface board as used for probe station

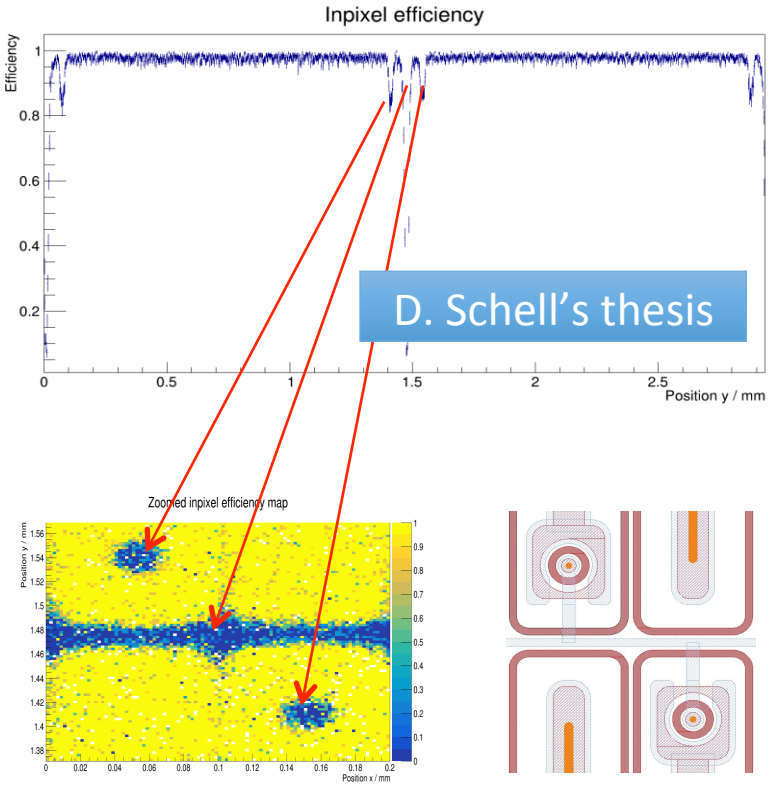
Baby MaPSA

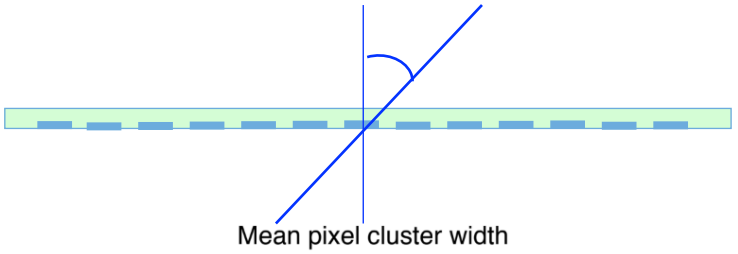


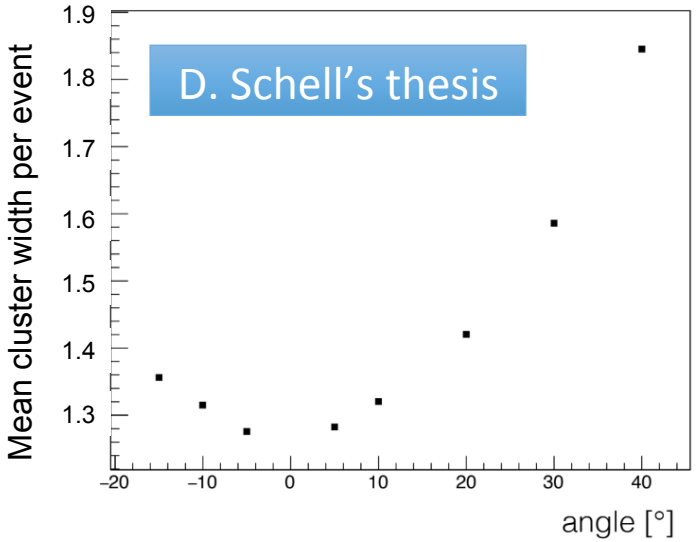


Characterization of Prototypes (3)

- Preliminary results from the baby MaPSA test beam campaign are being reviewed
  - Hit efficiency >98%, with small expected inefficiencies due to bias rail and bias punch-through
  - Angular scan: longer path through the sensor leads to larger clusters



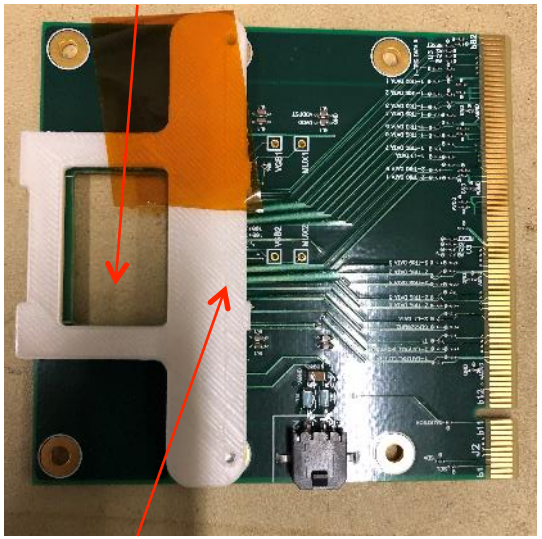




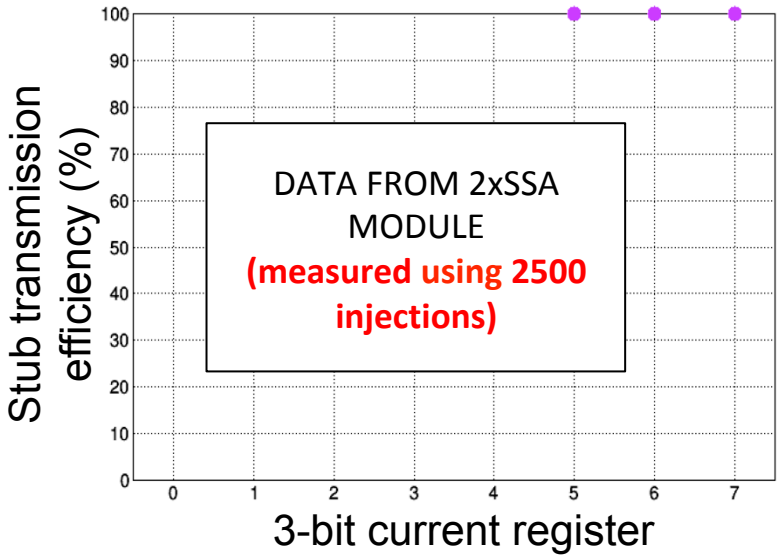
Characterization of Prototypes (4)

- Investigation of a 2xSSA module is on-going:
  - Verification of the SSA chip front end
  - Test of the inter-chip communication
- Status:
  - Working wire-bonded version of the 2xSSA was tested, lateral SSA inter-chip communication was verified
  - The bump bonded version of the 2xSSA module is expected this month
- The 2xSSA can be considered the precursor to a baby module consisting of a baby SSA sensor and a baby MaPSA

Sensor to be placed here



2 SSA chips under protective cover



Overview of QA/QC (1)

- Alan Honma was selected as the QA/QC coordinator for the OT within CMS (currently employed by Brown University)
- QC protocols are being developed as the final version of the front end ASICs and service hybrids become available
  - Until now CMS (and USCMS) has focused on the remaining validation of prototypes using ad-hoc test systems (*e.g. testing of 8CBC3 modules will be done using CIC1 mezzanine card and GBTx*)
  - The CMS DAQ is charged with releasing the final system for testing production service hybrids, front end hybrids, modules
    - USCMS is an active contributor to the development of the QC protocol for modules through our work on the middle-ware development
    - Test infrastructure for front end hybrids is being developed by CERN. USCMS is involved in the testing the front end hybrids.
    - Aachen/CERN are responsible for developing the QA/QC protocol for service hybrids. The first 2S functional service hybrids (v3) will be distributed to USCMS in the late Spring, along with the QC protocol.

Overview of QA/QC (2)

- USCMS started developing the QC protocol for MaPSA
  - Documents includes
    - Description
    - Parts
    - Handling and Packaging
    - Mechanical tests and inspection 5.Electrical tests
    - Fermilab Documentation
    - Con-conformity actions
  - We expect USCMS personnel to ensure knowledge transfer to the vendor through active participation in setting up the system at the company and site visits as deemed necessary
  - Vendors will be expected to have a probe station compatible with the test setup designed by USCMS. USCMS will provide the test setup

More details in backup slide

Status of the OT ASICs

- USCMS is not responsible for the the OT ASICS.
- Shown here for completeness is the status of the international contributions
  - Service Hybrids
    - 2S V3 will be distributed to the module assembly centers in late Spring 2019 (Aachen). Test boards for V3 are under commissioning. CERN will develop V4 and the associated test board.
    - PS POH V1 (and the associated test system) will be distributed for PS functional modules contribution in late 2019. PS POH V2 (and the associated test system) will be developed by CERN.
    - PS ROH (and the associated test system) will be developed by CERN.
  - Concentrator Chip CIC
    - 16 boards equipped with CIC1 delivered for testing January 30th. Tests are on going.
    - CIC2: chain test on going to ensure compatibility with FE ASICs and BE system.
  - 2S module front end chip CBC3.1
    - 13 CBC3.1 wafers had been tested. CBC3.1 chips are performing well.
  - PS module front end chip MPA, SSA
    - The SSA and MPA ASICs proved to work together and to produce correct stubs on 8 MPA and 8SSA (SRAM failure is being investigated)

Summary

Significant progress has been made in the development of the test systems in the past year

- 402.2.4.2 Test Systems
  - Hybrids
    - US CMS is acquiring knowledge about testing of the FEH and contributed to the QC of the prototypes delivered (to be delivered) to the assembly centers
  - Modules
    - US CMS finalized the development of the module burn in system and demonstrated that its performance meets the specifications
  - MaPSA
    - US CMS designed and produced the test systems for the MPA[MaPSA]/SSA and used it to carry out the MPA wafer testing at CERN and test beams at CERN
- Testing Campaigns
    - US CMS has successfully tested prototypes of growing complexity (2CBC3 minimodule before and after irradiation in beam, baby MaPSA in the lab and in beam, 2xSSA minimodule in the lab)
- QA/QC protocols are being developed as advanced prototypes become available

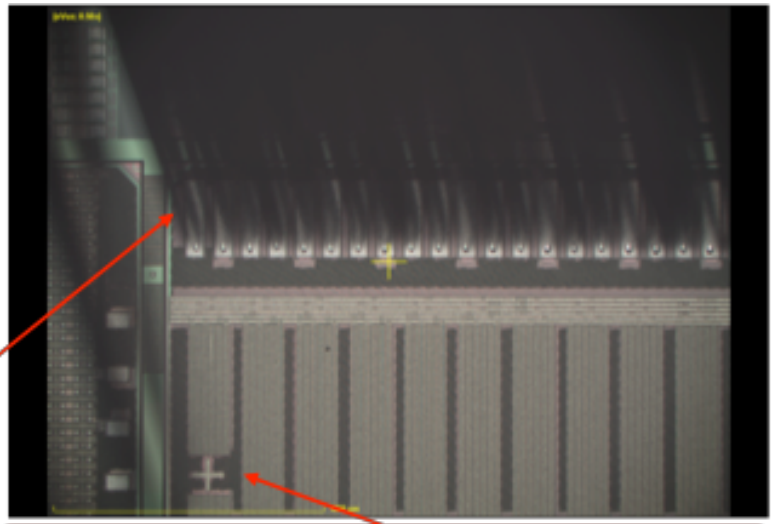
Additional Material

Availability of components

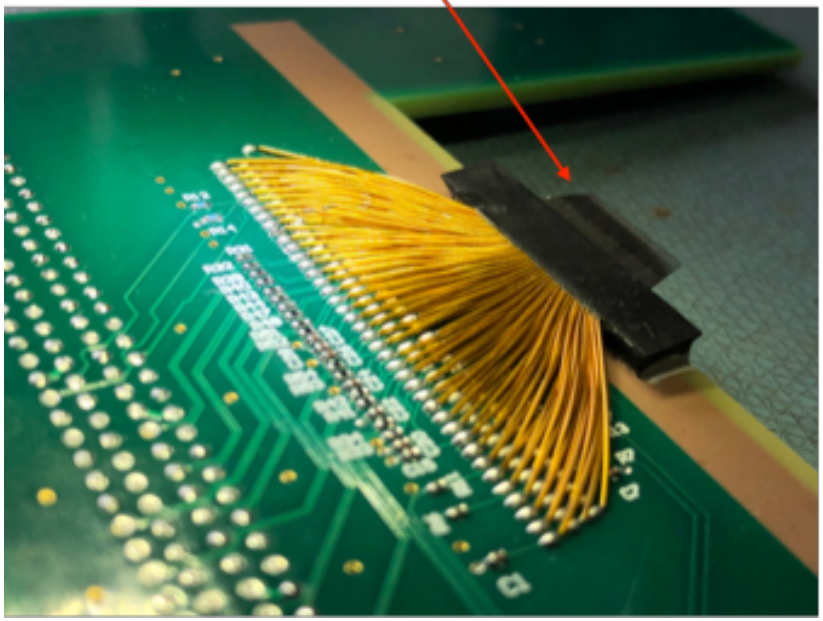
- The current plan is to assemble 5 2S modules per production line in the US
- This plan entails
  - 20 8CBC3 front end hybrids (expected in May-June 2019)
    - Options to read out out all CBCs or use a CIC1 mezzanine
  - 10 SEH3.1 service hybrids (expected in May 2019)
    - With GBT instead of lpGBT

Test Systems: MPA/MaPSA

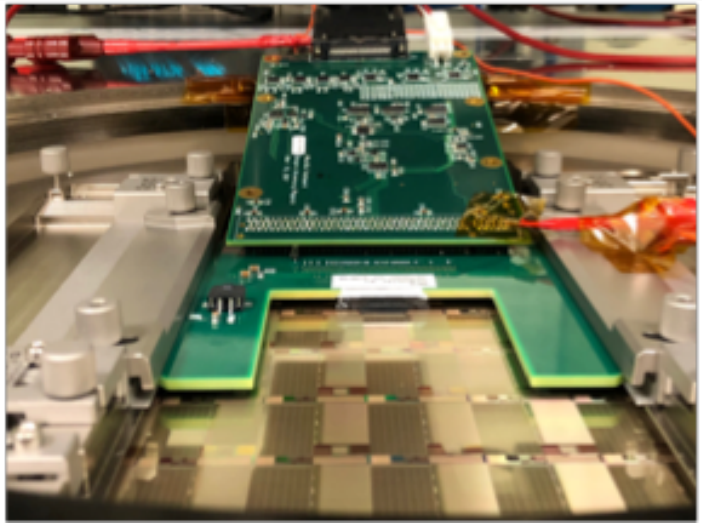
- The Probe Card lowers to contact wire-bonding pads on the MPA
- A probe station is programmed with the wafer map to facilitate moving from MPA to MPA



Probe card needles



Probe Station has image recognition for easy alignment



QC for MaPSAs (1)

- Mechanical/visual tests (after assembly and underfill application):
  - Check the bow of the MaPSA
  - Check wirebonds (free of contaminations)
  - Check sensor backside (no scratches)
  - Check that there is no excess underfill material that would interfere with spaces of the PS module
- x-ray or ultrasonic imaging to verify presence and location of bumps and penetration and continuity of the underfill.
- electrical tests (after assembly and underfill application):
  - Power on sequence
  - Power consumption
  - Bias DAC
  - Sensor current on a sample MPA
  - Bias DAC calibration
  - Write/Read to registers
  - Memory and Strip Input checks
  - Individual pixel tests -noise measurement is diagnostic of bump connectivity (Trimming and pulse injection, s-curves)

QC for MaPSAs (2)

- From experiences at CERN/Rutgers, the tests are expected to take ~4 minutes per chip.
  - We still need to define pass/fail and/or grading criteria.
- We will provide vendors with most elements of the teststand:
  - probe card / interface board, FC7 with all small attachment boards, power supplies, necessary cables, the software (eventually even a linux host computer).
  - We will be willing to help setup the system at the vendor sites.
  - We expect the vendors to have a probing station that is able to (automatically) move the MaPSA,