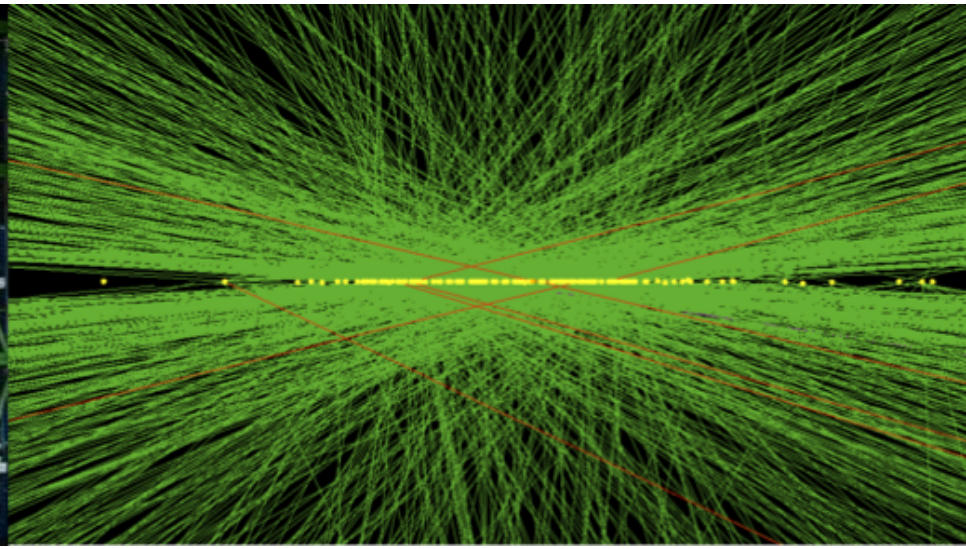
MTD-BO 5:
In-depth: ETL ASIC (ETROC) 402.8.4.2

Ted Liu (FNAL)

HL-LHC CMS Upgrade CD-1 Director's Review

20 March 2019



Brief Biographical sketch

- Ted Liu (Fermilab)
- Coordinator for front-end electronics in MTD/ETL
- L4 for ETL ASIC in US-MTD
- Relevant Expertise for ETL:
  - LBNC review committee member
    - DUNE cold electronics (with a few ASIC chips in 65nm and 130nm)
  - Tracking Trigger R&D for HL-LHC (AM based)
    - 3DIC Vertically Integrated Pattern Recognition AM (VIPRAM) chip R&D
    - ATCA based system demonstration for HL-LHC tracking trigger
    - ATLAS FTK (90nm AMchip04 R&D and data formatting system)
  - God-parent committee for Pico-second timing project (U Chicago)
  - Review Committee chair for Fermilab Electrical Engineering
  - CDF Trigger Coordination (+ muon/calorimeter/SVT/L2 trigger upgrade)
  - Babar Drift Chamber Tracking Trigger project coordination
  - Belle Aerogel Cherenkov Particle Identification Detector
    - Preamp/front-end + SCA-based-TDC ASIC waveform readout system design
  - CLEO Time-Of-Flight calibration for Particle Identification
  - Silicon Drift Detector R&D with SCA (Switch Capacitor Array)

Outline

- Scope and Deliverables of ETL ASIC 402.8.4.2
- Conceptual Design
- Cost and Schedule
- Contributing Institutions
- Resource Optimization
- ES&H
- QA/QC
- Response to previous reviews
- Summary

Design ETL ASIC to fully meet the ETL requirements
Fully test and verify the design
Procure ASICs to cover 50% of ETL

ETL ASIC (ETROC: ETL Readout Chip)

- ***Will first provide a concise overview of the technical design, then cover the schedule, cost, project management aspects***
- ***Full design details of ETL ASIC available in MTD CDR: Page 217- 220 (intro), page 277– 300 (design details)***
- ***Only a few highlights below***
  - ***ETL ASIC Overview and Design Study***
  - ***Preamp/Discriminator Design Performance Simulation***
  - ***TDC Design***
  - ***Clock Tree Distribution Design Study***
  - ***Power Consumption Estimate vs Performance***
  - ***Development Plan and Schedule***

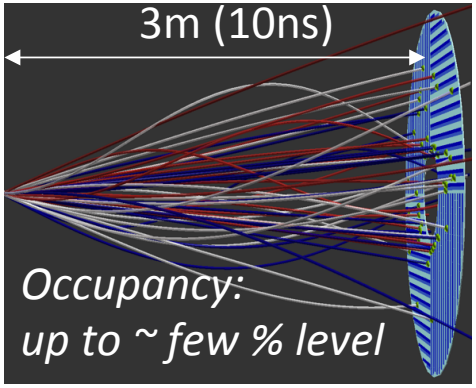
The ETROC design study started June 2018, the actual design implementation since Sept 2018, has been making rapid progress

ETL Timing Resolution

- The MTD design goal is to achieve timing resolution of ~35 ps per track (50 ps @ end of life), and ***for the ETL this will be achieved by having two hits per track***.
  - The time resolution is required to be < ~50 (71) ps per hit
    - *Will use 50 ps per hit as reference in this talk (to keep it simple)*
- Contributions to the total time resolution:
  - LGAD contribution due to Landau fluctuation of charge deposition of MIP; ~ 30ps (40ps @end of life @highest eta)
  - Jitter due to the preamp and discriminator; < 40ps
  - TDC (bin size and clock distribution within chip); < ~10 ps
  - Residual of the time-walk correction; < ~10ps
  - System level clock distribution; < ~15ps

Will get back to this later in the talk

ETL: The view from the ASIC

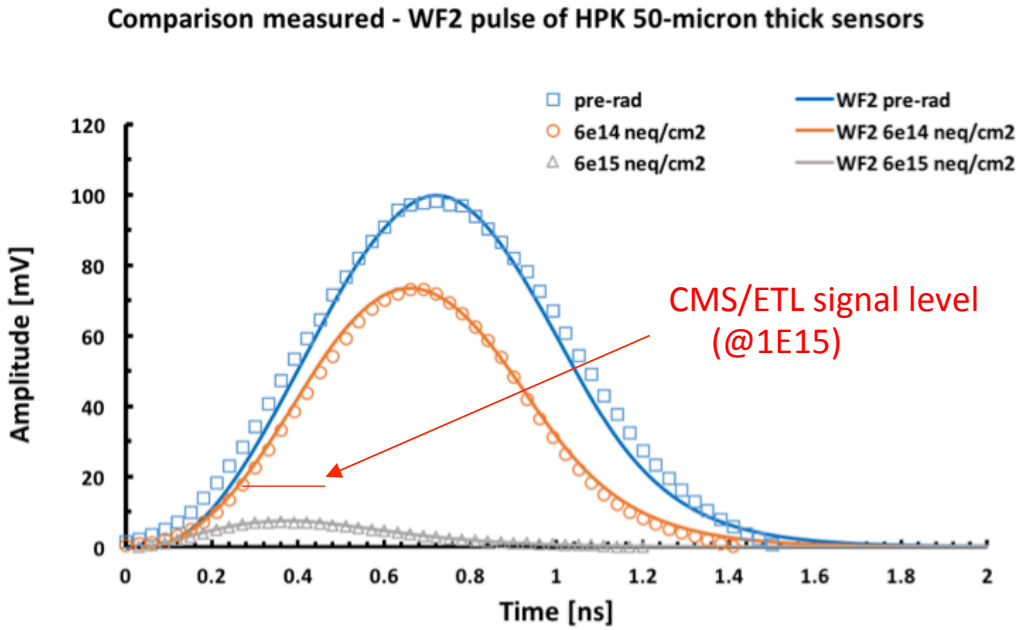


- *LGAD sensor*
  - LGAD gain is modest: 10-30
  - LGAD (50um) intrinsic time resolution: ~ 30-40ps
  - Targeted signal size: 6 -20 fC
  - ~1 × E15 *n*eq/ cm^2 at high eta
    - Gain drops with increasing dose
    - → ***signal size drops***

Main challenge for ASIC design:

Extract precision timing information from small LGAD signal size at high radiation dose

The front-end design has to be optimized for small LGAD signal at high radiation dose while keeping the power consumption low



ETROC: ETL Read-Out Chip

ETROC is bump-bonded to LGAD sensor, to handle a 16 × 16 pixel matrix, each 1.3 mm × 1.3 mm. chip size ~21mm x 21mm.

ASIC contribution to time resolution < ~40ps

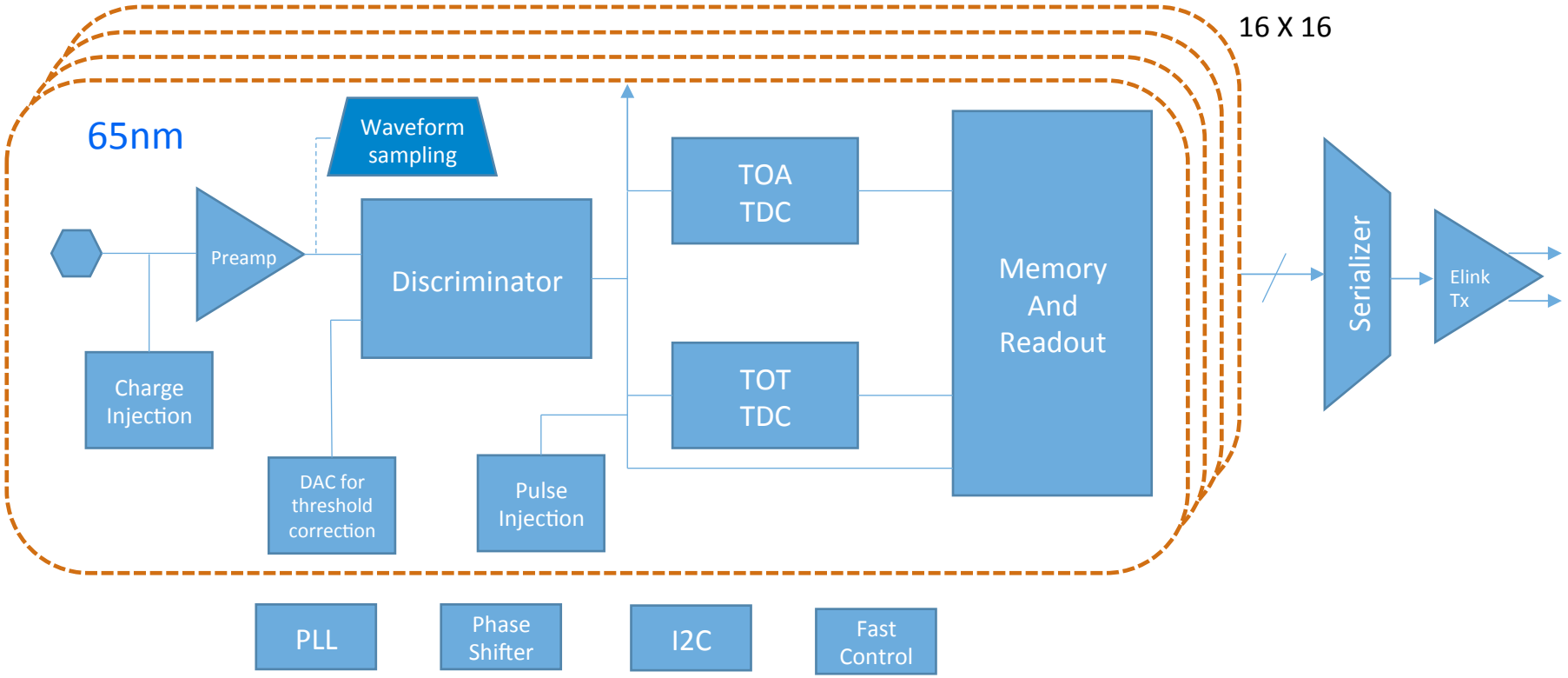
Targeted signal charge (1MIP): 6fC

TDC range: ~5ns TOA and ~10ns TOT

L1 buffer latency: 12.5 us

with power consumption < 1W/chip

Whenever possible, the ETROC design will be based on existing designs already available, esp the supporting circuitries.



ETL ASIC Specifications

Table from MTD CDR

Table 3.5: A summary of ETROC requirements.

Requirement	Value	Comments
Process	TSMC 65 nm MS RF LP 2.5 V with metal stack `1P9M_6X1Z1U_RDL (CERN)`	
Power supply	1.2 V	
Timing resolution	40 ps	Total timing resolution per hit including 30 ps contribution from sensor is 50 ps. Total timing resolution per track is about 35 ps considering two layers of sensors.
Pixel size	1.3×1.3 mm^2	
Pixel capacitance	3.4 pF	50 μm thickness
Pixel matrix size row x column	16×16	
Power consumption	below $\approx$ 1 W/chip	
Data storage capability	12.8 μs	Level-1 trigger latency
Trigger rate	Up to 1 MHz	
Operation temperature	-30 °C to +20 °C	
TID	100 MRad	
SEU	TBD	system requirements

Development Plan

- The development plan consists of three phases
  - Design specification study (see next)
  - Prototyping phase
  - System level testing phase
- Prototyping phase: a series of prototype chips each focusing on different aspects of the design
  - ETROC0: preamp and discriminator (most critical)
  - ETROC1: preamp + discriminator + TDC, 4x4 clock tree
  - ETROC2: + all supporting circuits, 8x8 clock tree
  - ETROC3: scale up to 16x16 clock tree (full size)

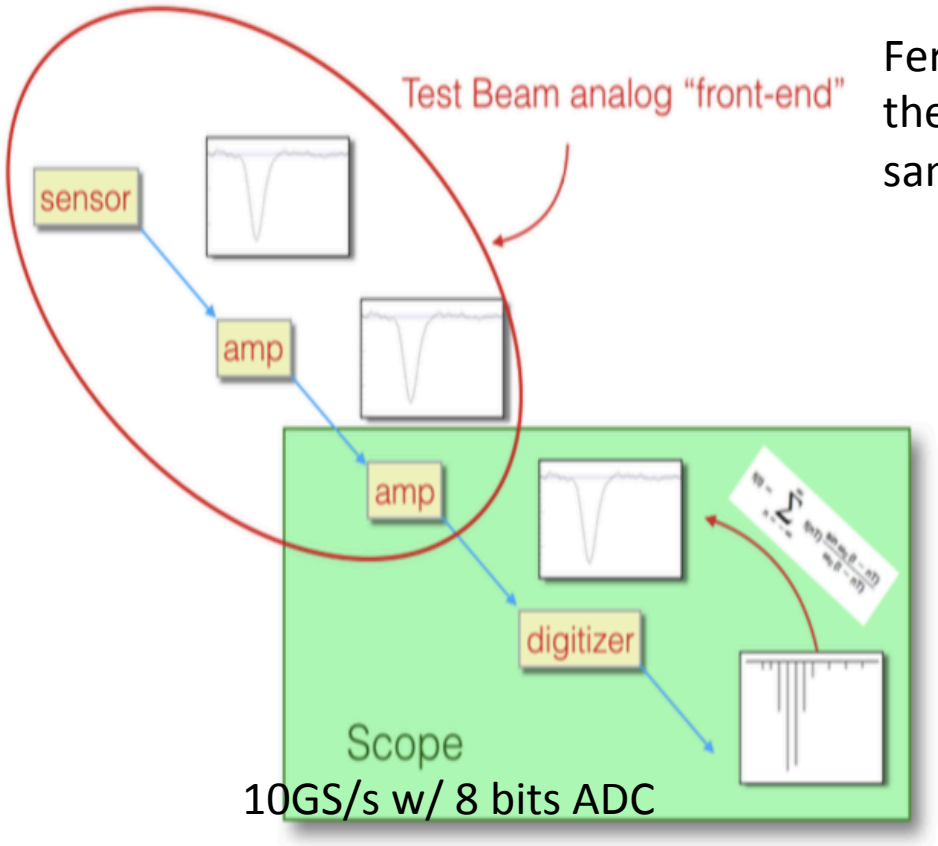
Rapid progress since June 2018, with a productive design team:
ETROC0 chips will be delivered next week
ETROC1 design in full speed, to be ready for submission June 2019

Our Methodology to approach the design

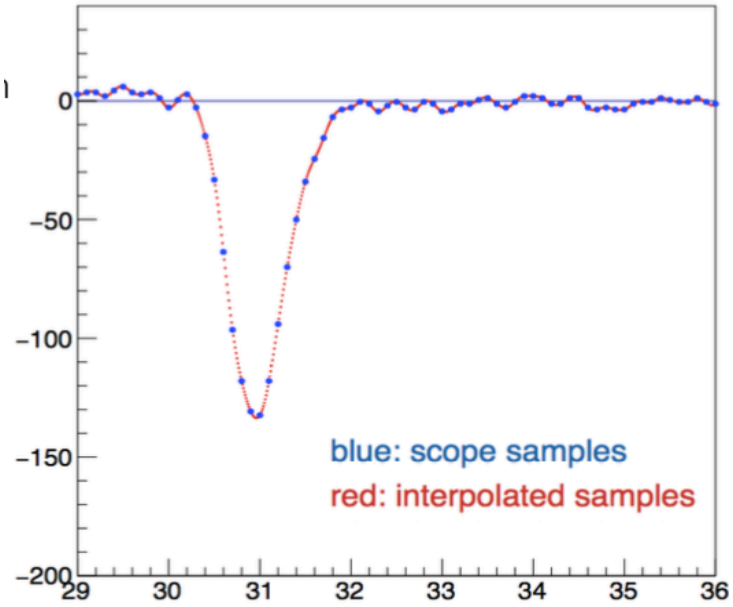
- A three pronged approach is taken to consider the ASIC and the sensor together from the start to ***optimize the front-end design for LGAD behavior at end of operations*** (low signal size etc)
  1. Use the ***LGAD beam test data*** as input , to study different timing algorithms (Leading Edge vs Constant Fraction Discrimination or CFD)
  2. Use ***LGAD simulation as input***, ***simulating different front-end design concepts***
  3. Simulate and optimize the expected performance of the actual ASIC implementation ***with post-layout simulation, using LGAD simulation as input***

The three-pronged design approach has been highly effective making rapid progress since June 2018

Waveform analysis: LGAD Test beam data



Fermilab test beam data for LGAD: to guide the design of the front-end using sampled waveforms recorded with scope.

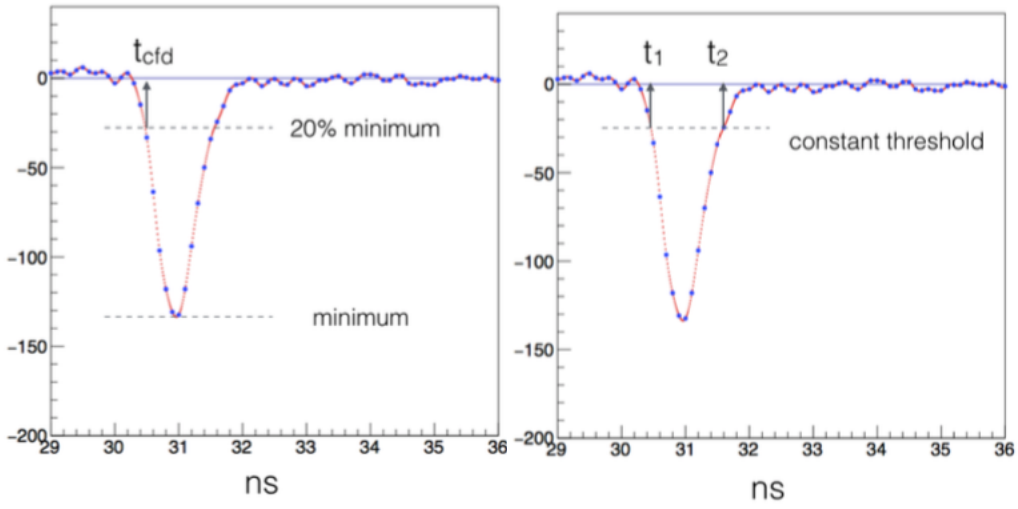


The red points: the interpolation performed using the Shannon-Nyquist formula. The functional interpolated signal is used to simulate the discriminator response and study timing algorithms

Use LGAD Test beam data: CFD vs LE/TOT

CONSTANT FRACTION VS. LEADING EDGE

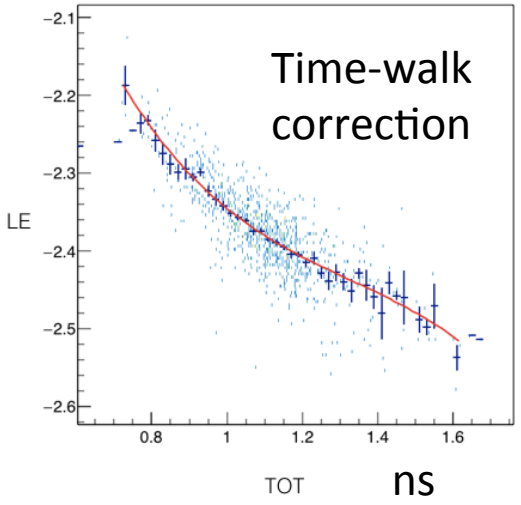
CFD LE



Careful study has shown that there is no obvious advantage of using CFD over LE+TOT.

Given that CFD implementation is more involved, the LE+TOT approach is chosen

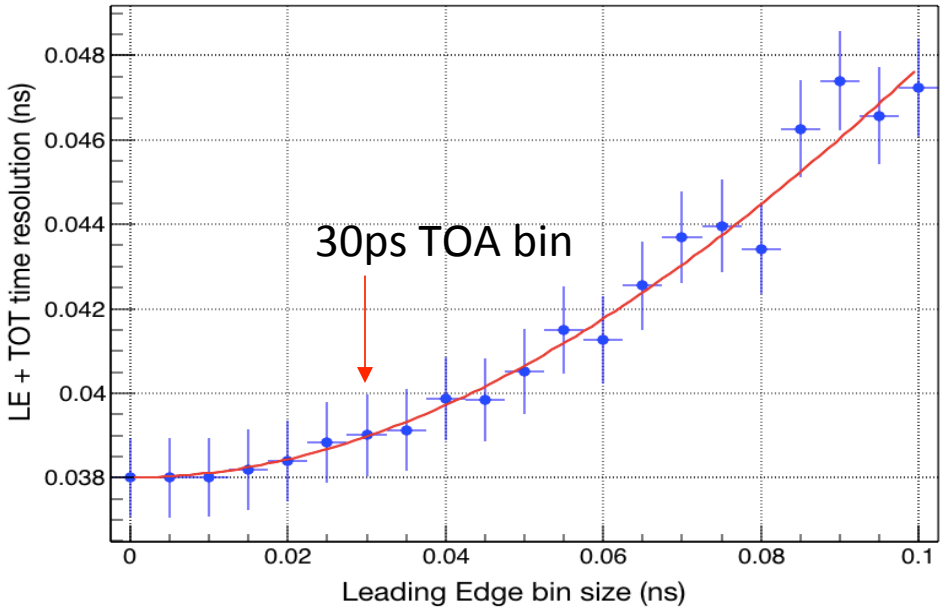
sensor type	CFD	LE+TOT
FBK W6 pre-irradiated	28 ps	30 ps
FBK W6 8.0x10^{14} n/cm^2	30 ps	32 ps
FBK W6 1.5x10^{15} n/cm^2	42 ps	40 ps



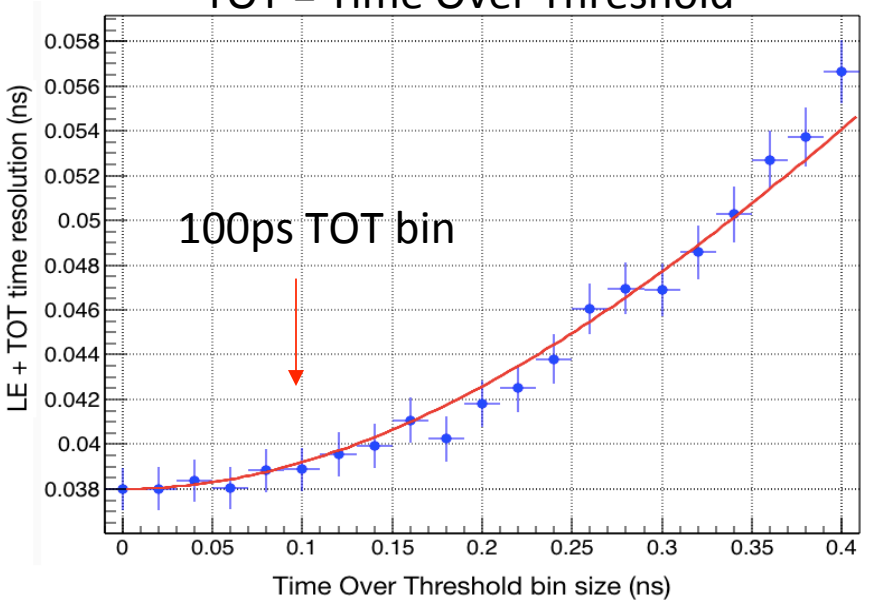
Use LGAD Test beam data: TOA/TOT bin

what is the coarsest quantization without affecting the final time resolution of the LE+TOT.

TOA = Time Of Arrival



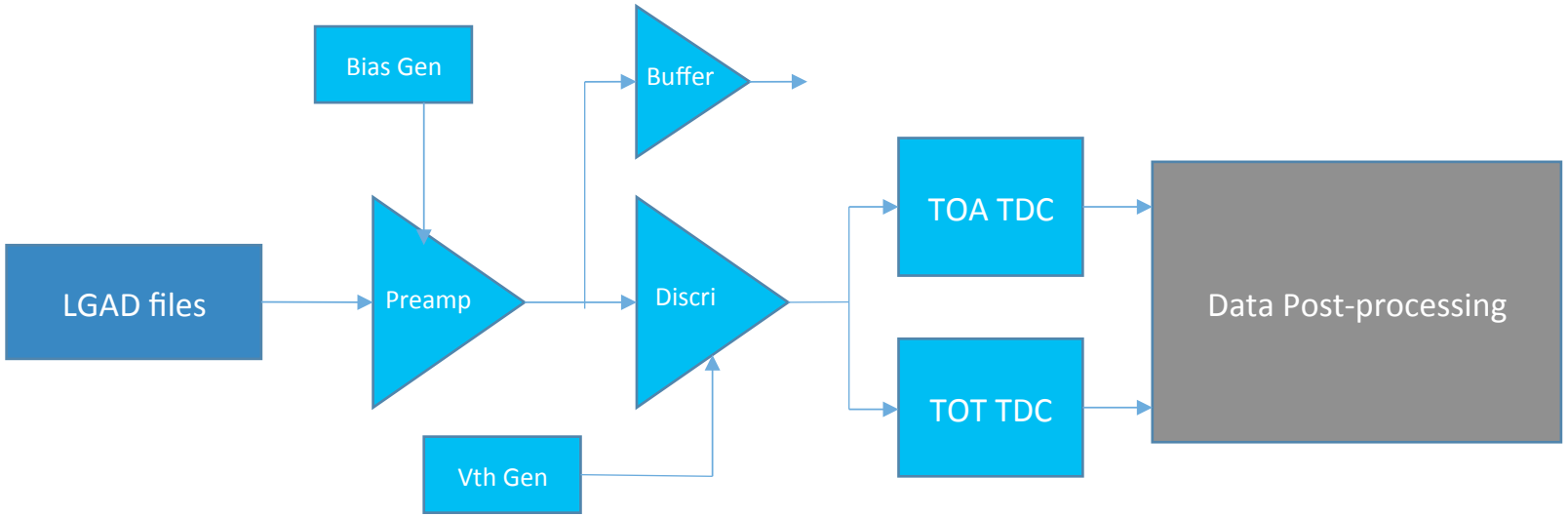
TOT = Time Over Threshold



A quantization bin size of up to ~30ps for LE (TOA) and ~100ps for TOT are good enough

Knowing the design target well has allowed us to arrive at optimal TDC design quickly

How we approach the front-end design



- ***Optimize the frontend circuits with LGAD simulation as input***
  - ***With three cases: Pre-irrad, 5E14, 1E15***
- The preamp:
  - ***optimized for low signal size at realistic sensor bias voltage.***
- The discriminator and its threshold voltage generator are designed to
  - ***match the preamp for low signal size***

Higher timing precision usually means higher power consumption

A good design is a balance between performance and power

→ Preamp bias current is configurable (four settings from low to high power)

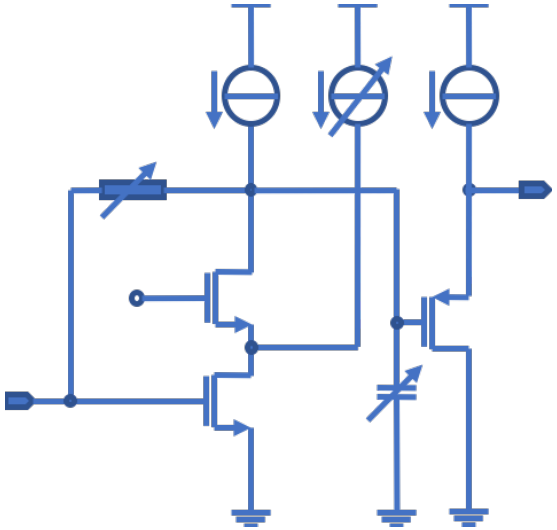
Preamp design

Preamp has been fully designed, implemented and optimized for low signal size

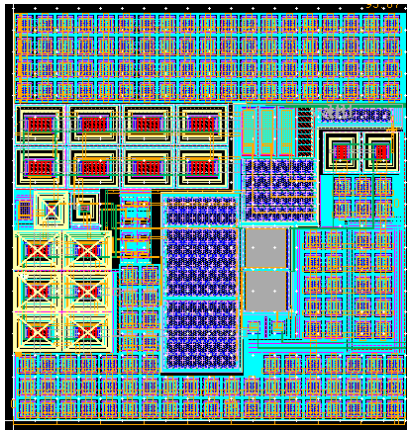
Performance achieved with post layout simulation:

LE jitter at 28 ps for the 6fC signal size with 1.3 fC threshold

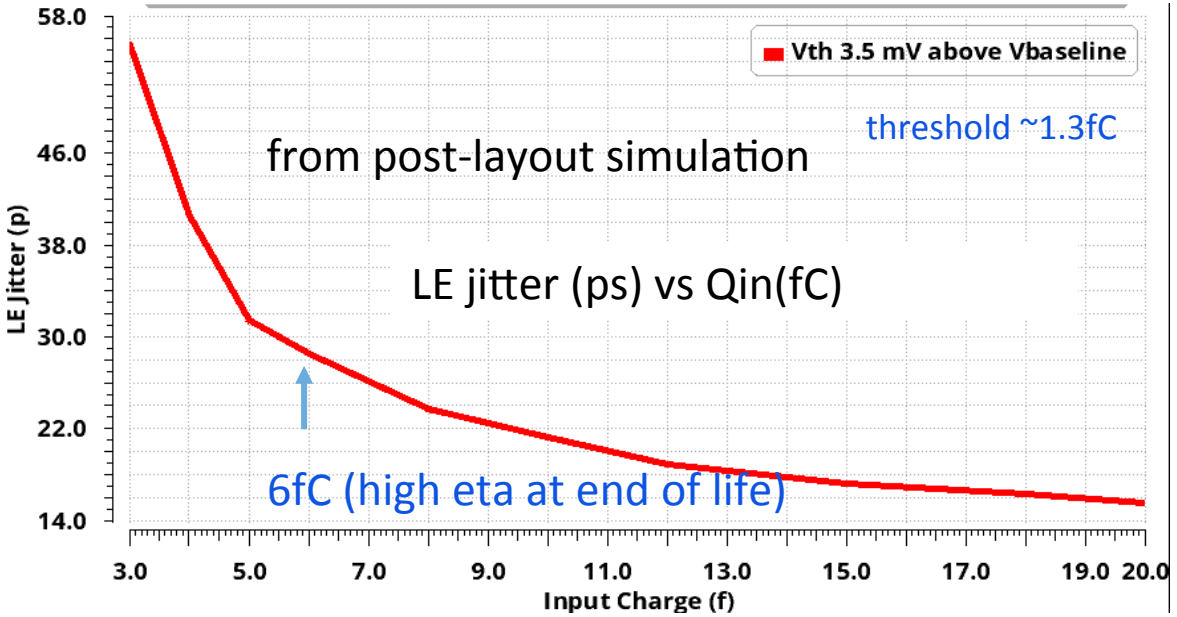
low threshold → critical for maintaining resolution/efficiency for small signals after irradiation at end of operation



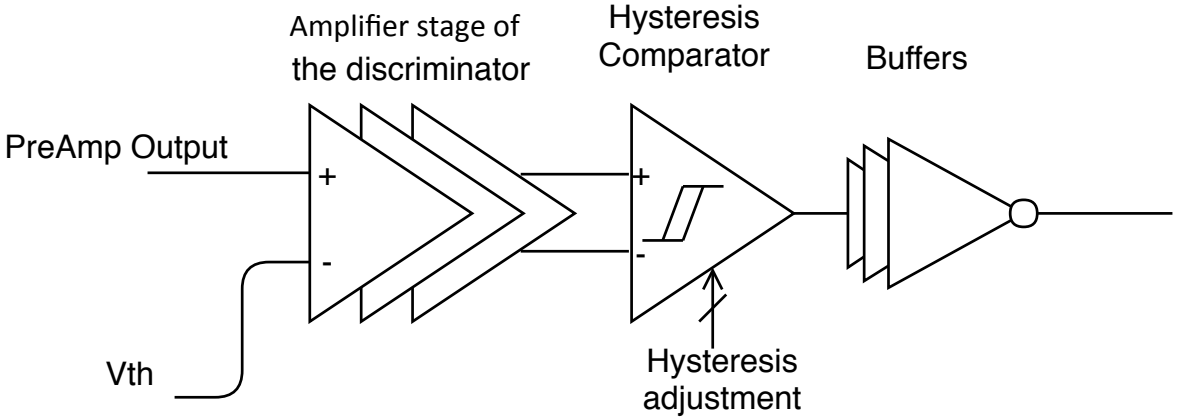
90 um X 94 um



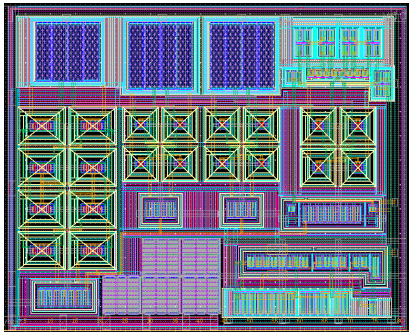
A cascode amplifier + source follower.



Discriminator Design



81 um X 67 um



0.71 - 0.78 mW @
1% - 10% occupancy

The discriminator is designed to match with the small signal size from the preamp

Fully implemented and optimized the full chain for low signal size while keeping the power consumption low

Full-chain: LGAD + Preamp + disc

- Three irradiation levels for LGAD Sensor simulation: pre-irrad, 5E14, 1E15
- @ temperature: -20 degree
- Two preamp power settings studied (low and high)
  - 0.67 mW, 1.25 mW

The time resolution includes:

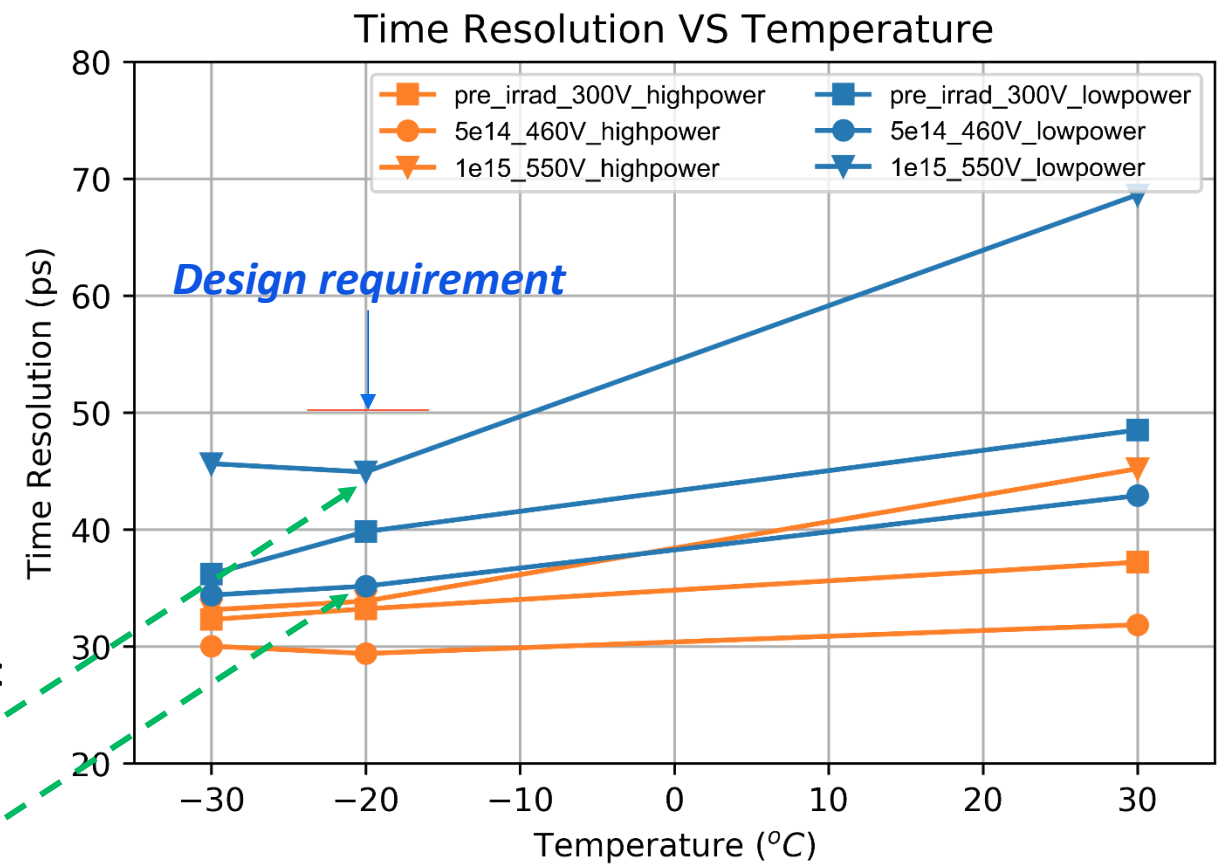
LGAD contribution
Preamp + Discriminator
TDC bin size (20ps)

Using TOA/TOT approach

Even with preamp @ low power:

Worst case: ~ 45ps (1E15)

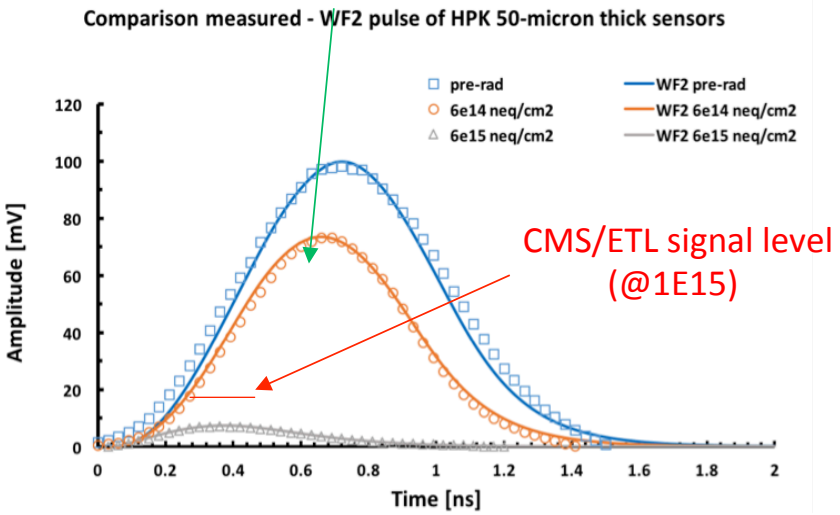
Typical case: ~ 35ps (5E14)



Post layout simulation result good,
to be validated by ETROC0 chip testing result soon

ETL Timing resolution contribution estimate

- (1) Landau noise (LGAD sensor) + preamp/discriminator + TDC bin: 35ps (5E14) to 45ps (1E15)
- (2) TDC measurement due to clock etc <~10ps
  - Clock/timing distribution within chip, etc.
- (3) Time-walk correction residual <~10ps
- (4) Clock distribution at system level <~15p



For typical cases with ~ 5E14 irradiation

(1) (2) (3) (4)

Total = sqrt (35^2 + 10^2 + 10^2 + 15^2) = 41 ps per hit, with 2 hits per track, 41/sqrt(2) = 29 ps per track

(extra margin for 50 ps per track goal)

For worst case with ~1E15 irradiation, for modules around highest eta

(1) (2) (3) (4)

Total = sqrt (45^2 + 10^2 + 10^2 + 15^2) = 50 ps per hit, with 2 hits per track, 41/sqrt(2) = 35 ps per track

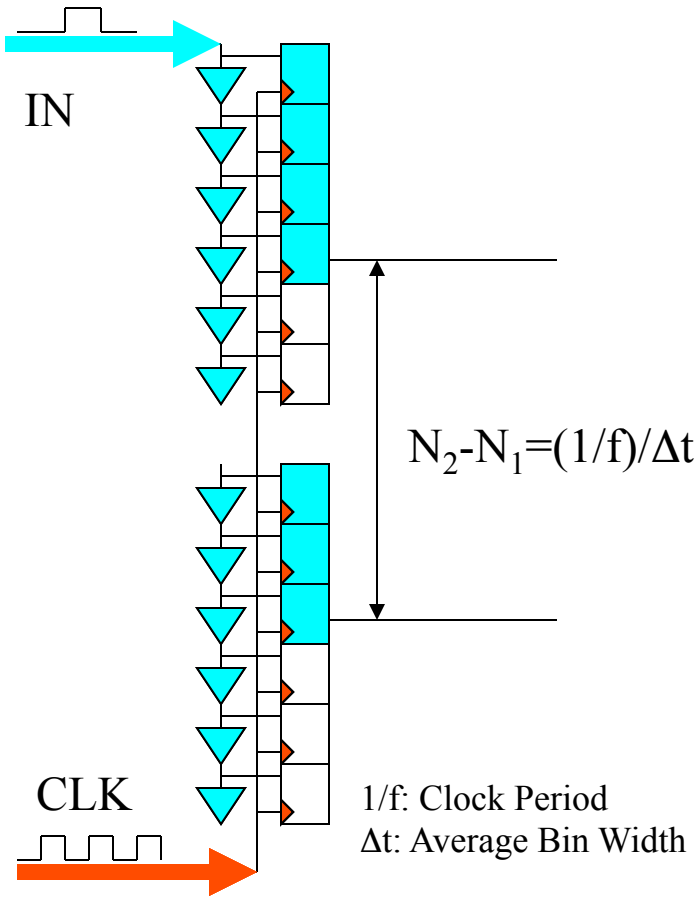
(extra margin: highest eta modules can run at higher preamp power)

This front-end design provides a solution tuned to ETL specific needs for resolution, power budget, and radiation profile

TDC Design

- TDC requirements
  - TOA bin size < ~30ps, TOT bin size < ~100ps
  - Lower power highly desirable
    - ***ETROC TDC design goal: < 0.2mW per pixel***
- ETROC TDC design optimized for low power
  - A simple delay line without the need for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- ***In-situ delay cell self-calibration technique***
  - For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
  - Crucial to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)

Self-Calibration: Twice-Recording Method



- **Each hit registered twice at two consecutive clock edges**
- **Use known clock period for "on the fly" self-calibration of delay line**

The two measurements can be used:

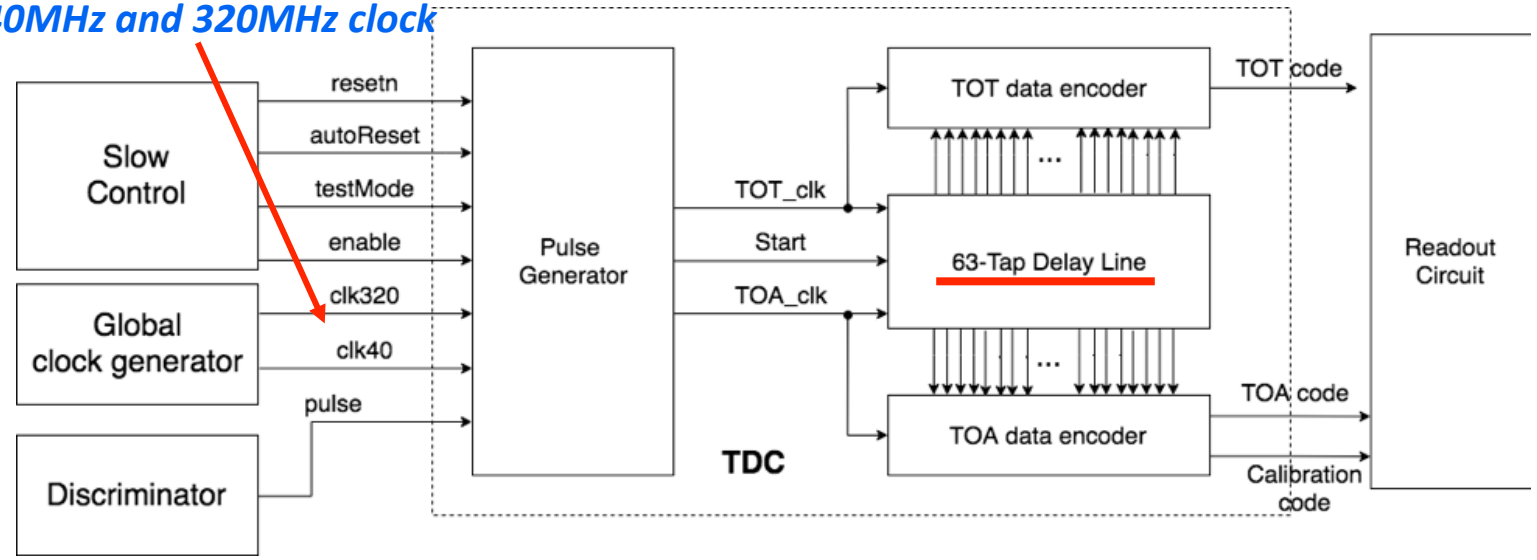
- to calibrate the delay.
- to reduce digitization errors.

Animation by Jin-yuan Wu (FNAL EE Engineer)

ETROC TDC Design

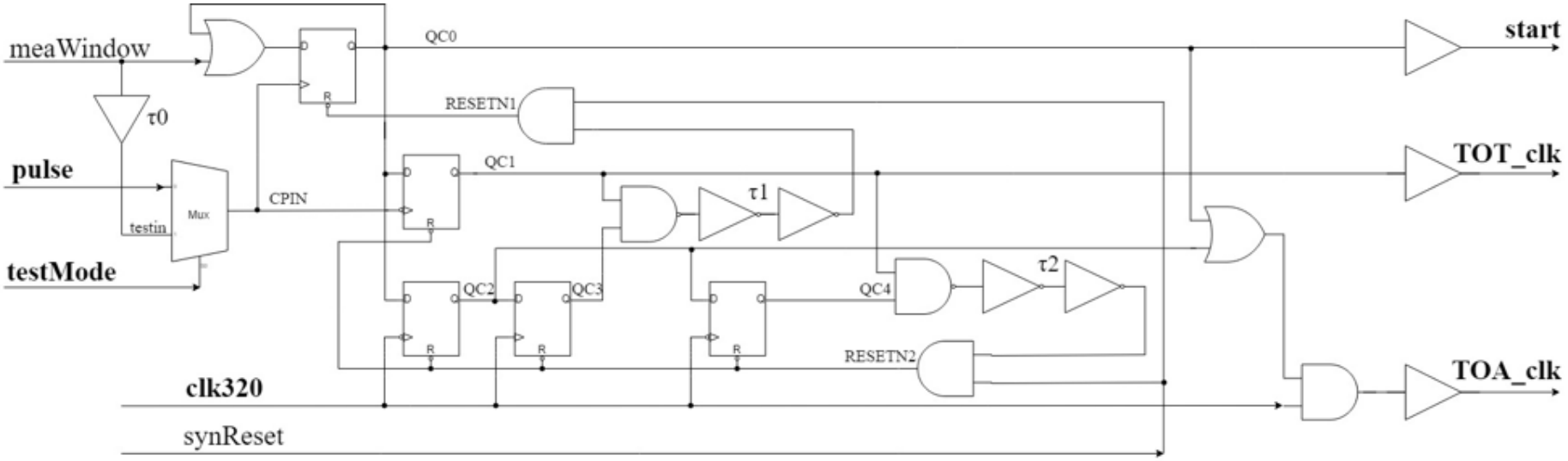
Use the same simple delay line to measure both TOA and TOT, with self-calibration. ***Total power: < 0.2mW per pixel @ 10% occupancy***

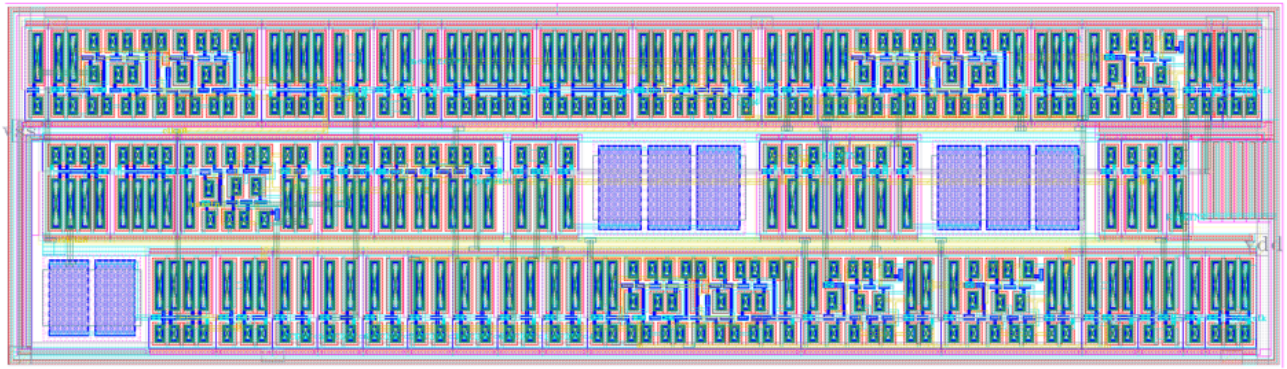
Each TDC expects 40MHz and 320MHz clock



This approach deviates from ATLAS ALTIROC TDC design, with the goal to reduce power consumption.
ALTIROC uses the more traditional Vernier-based dual delay lines, with each delay cell dynamically adjusted using DLL. One set of delay lines for TOA and another set for TOT, total of four delay lines per pixel.

TDC Pulse Generator or Controller

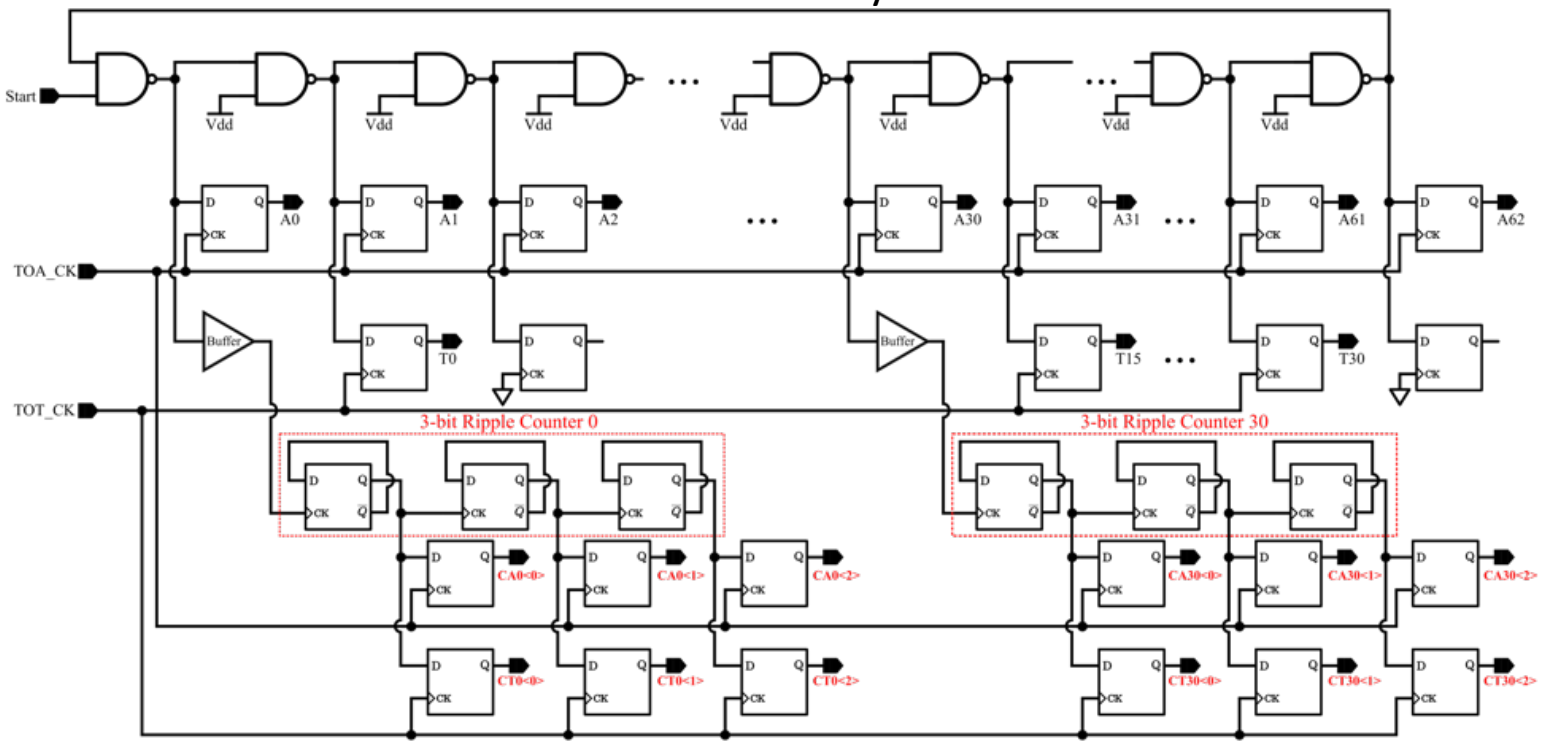


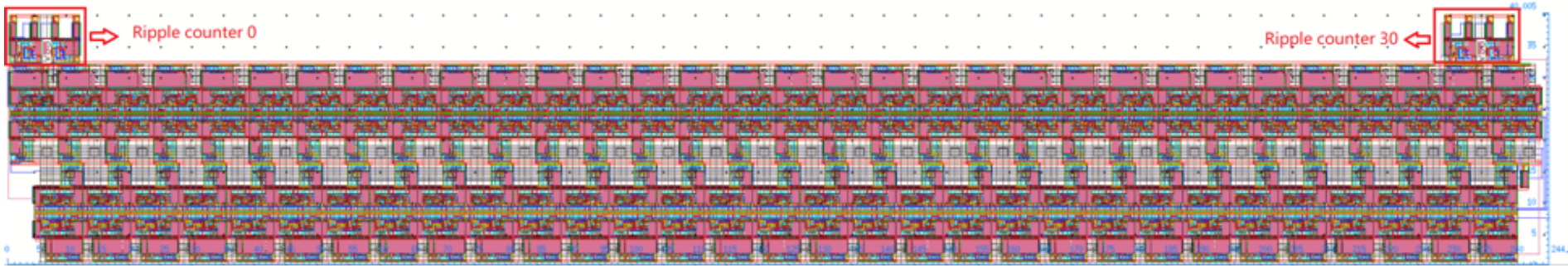


Preliminary layout: 45 um x 13 um

TDC delay line implementation

Cyclic structure



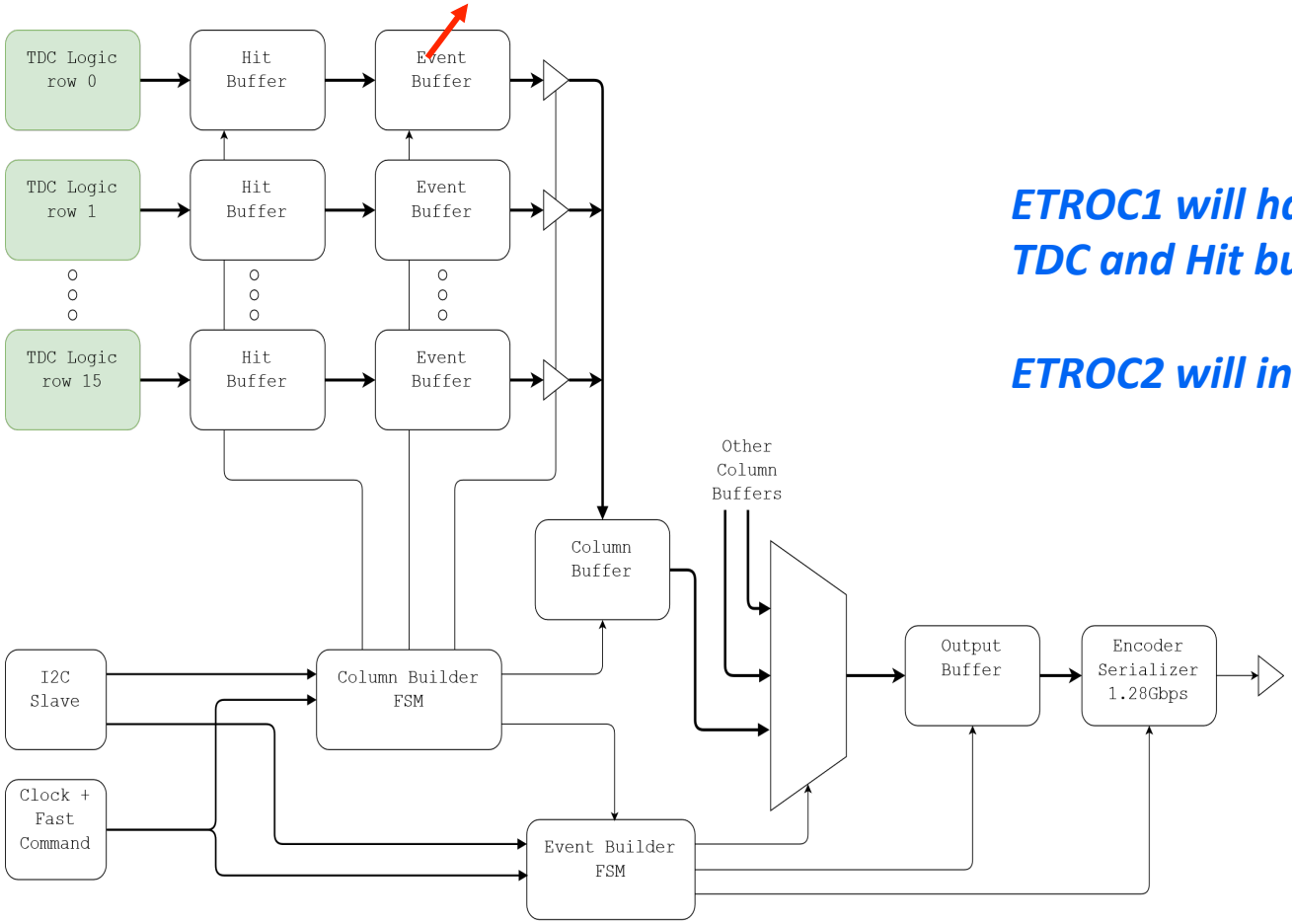


Preliminary layout of the 63-tap delay line. 245 um x 40 um. Delay cell ~ 22ps

ETROC L1 buffer and Data Readout

Data format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	V	CAL [5..0]						BCID								TOA [8..0]									TOT [6..0]						



Elink output
(320Mbps good enough)

ETROC1 will have both TDC and Hit buffer implemented

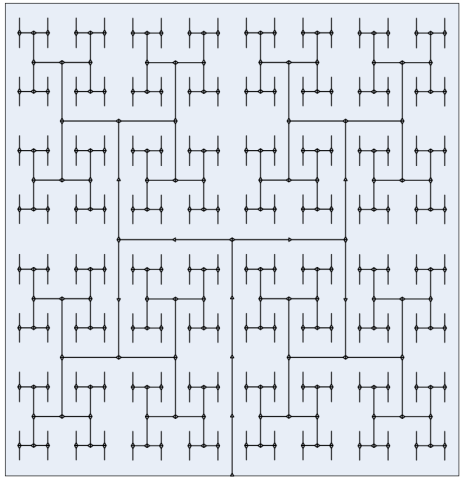
ETROC2 will include all the rest

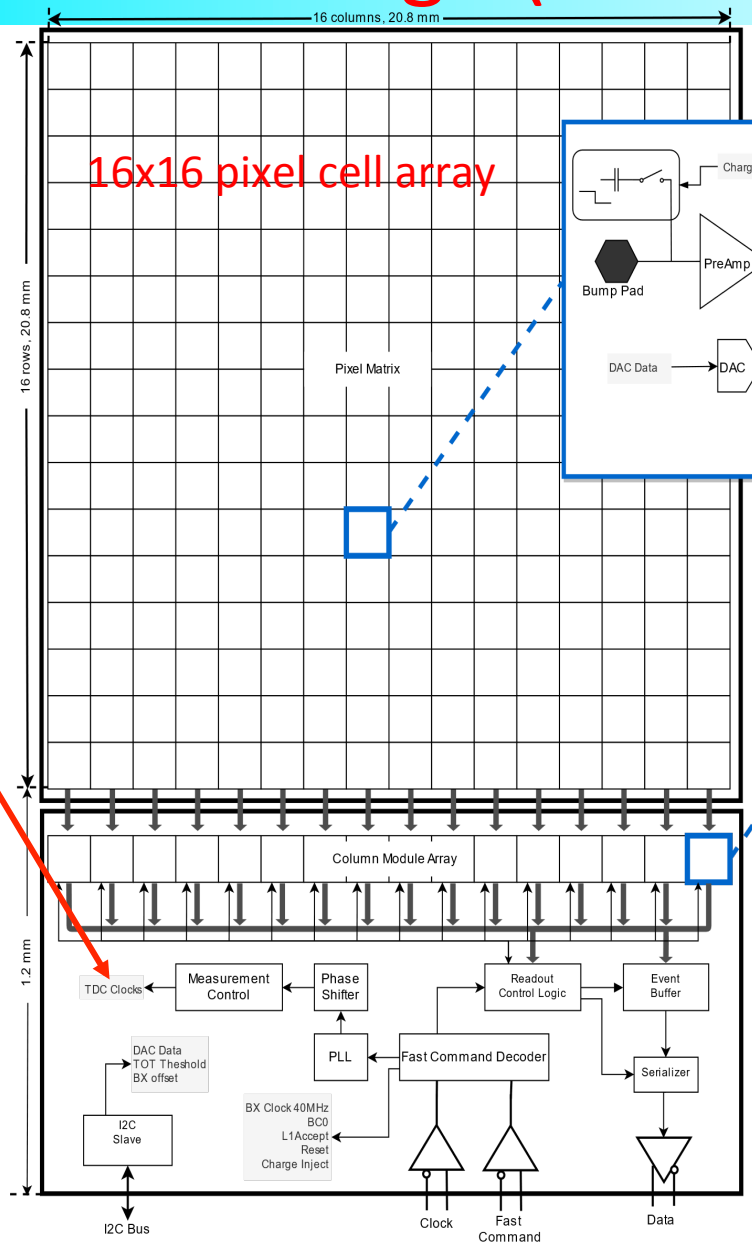
The readout of ETROC is much simpler than typical pixel detector ASIC. Only 256 channels per chip for ETROC (RD53: > 100k channels per chip)

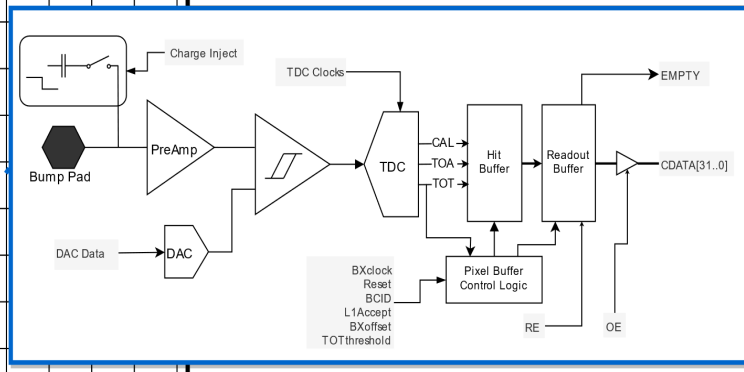
Final ETROC Design (details in CDR)

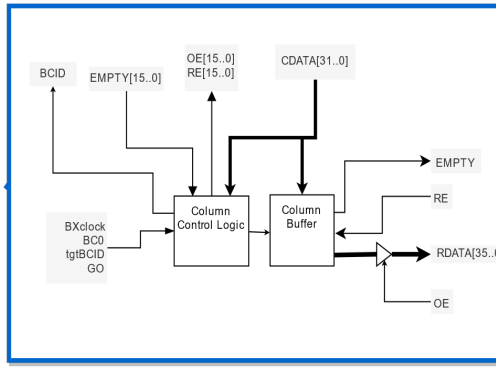
Each TDC expects 40MHz and 320MHz clock. The next important aspect is the clock distribution into each pixel

16x16 clock H tree

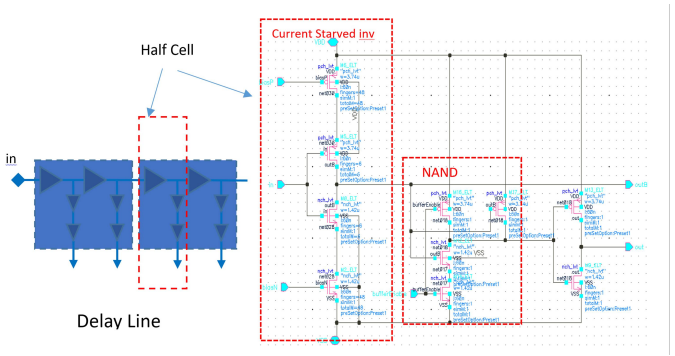




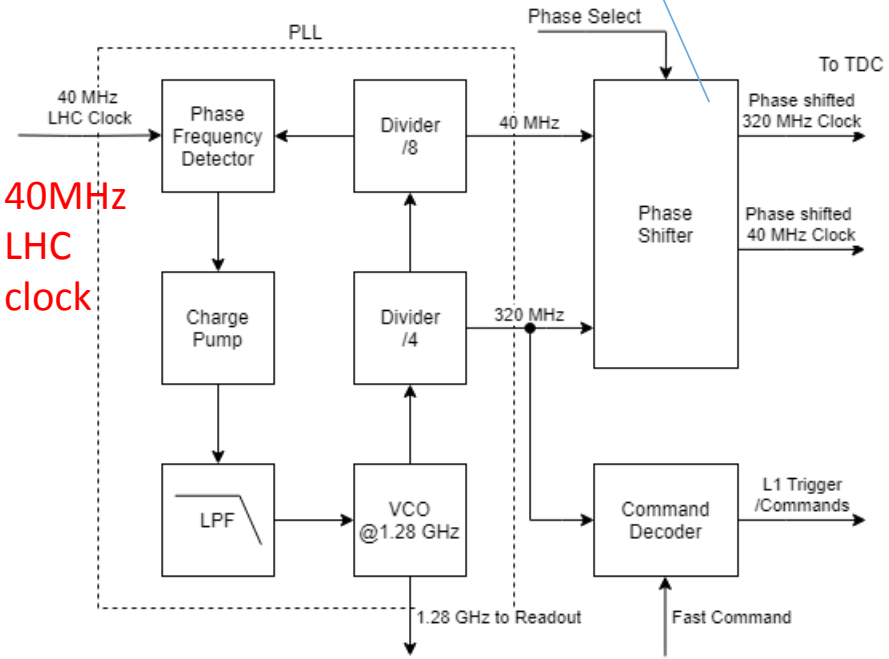




ETROC Clock Distribution

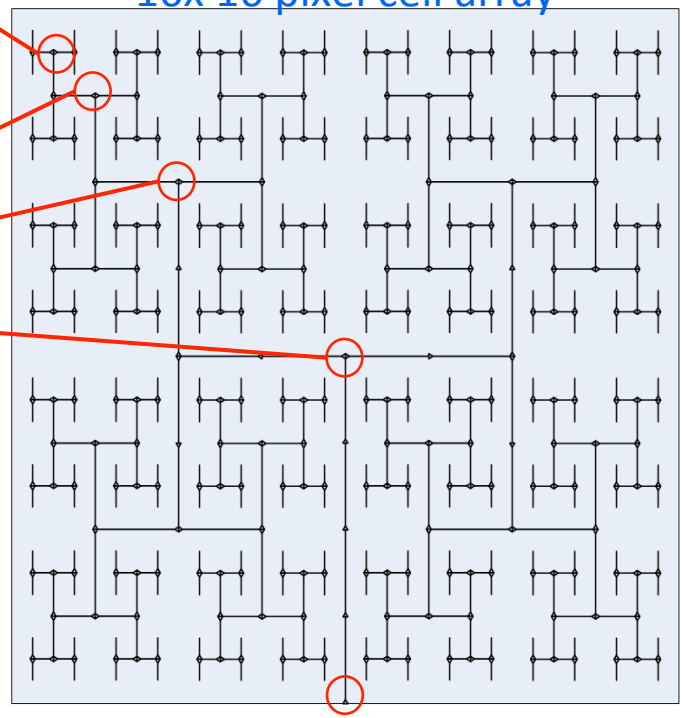


Phase shifter based
on existing design for lpGBT in 65nm



40MHz
LHC
clock

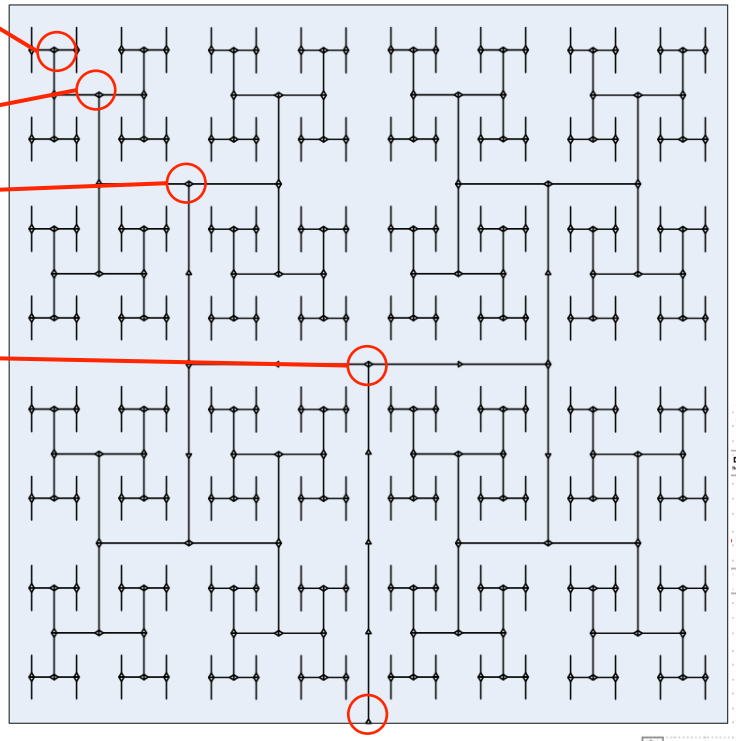
16x 16 pixel cell array



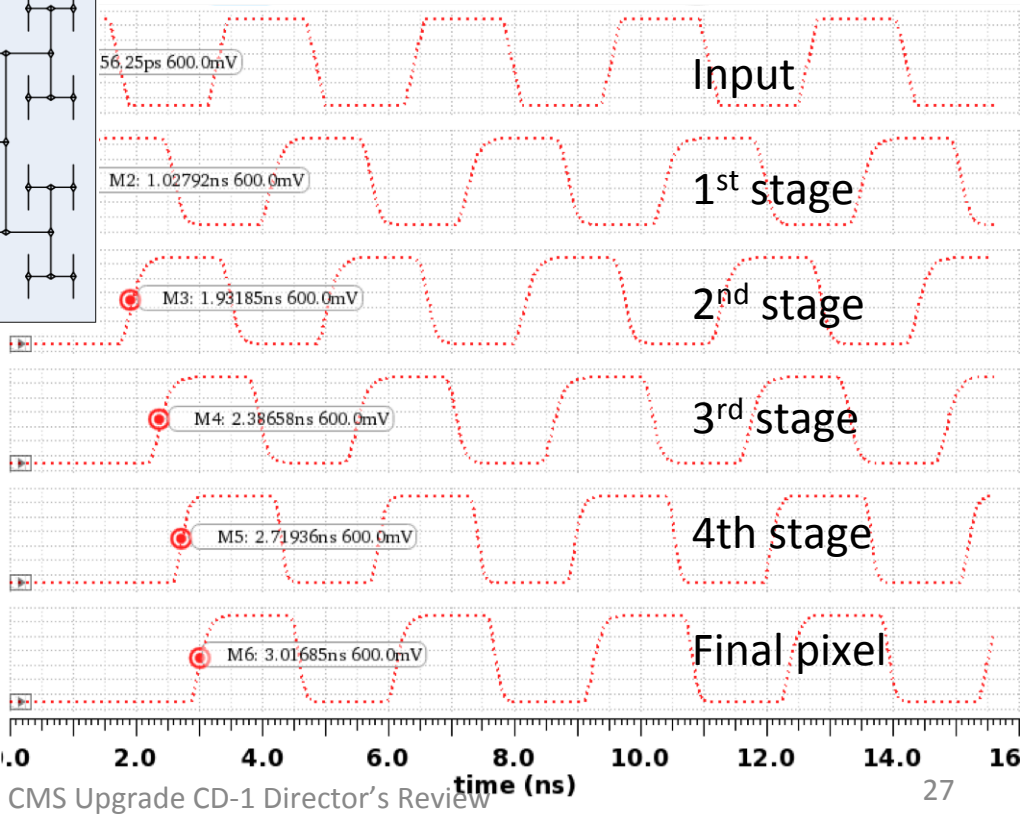
40MHz and 320MHz clock

16 x 16 Pixel array
Each pixel: 1.3mm x 1.3mm
Chip size: ~ 21 mm x 22mm

16X16 Clock Distribution Study



Clock jitter ~ 5ps



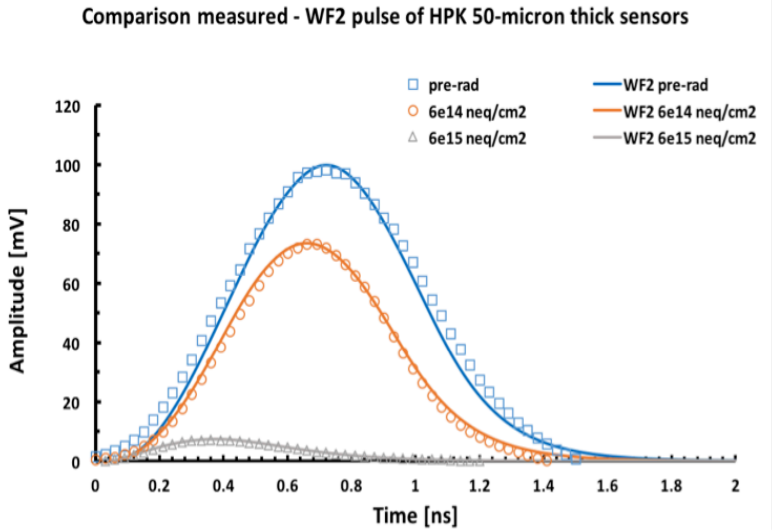
16 x 16 Pixels
Each pixel: 1.3mm x 1.3mm.

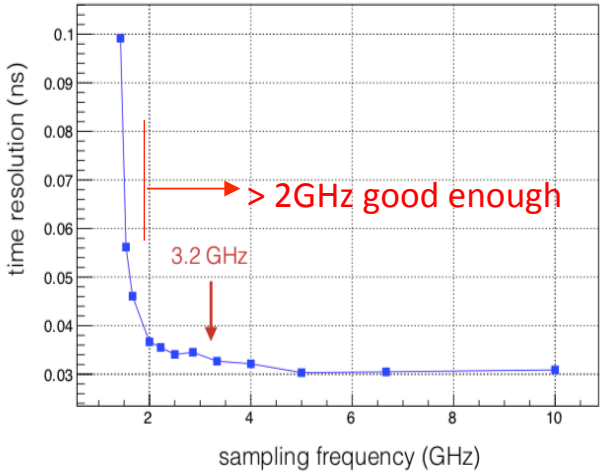
Input Clock Signal:
320MHz (Period = 3.125ns)

Power consumption ~ 20mW

ETROC on chip waveform sampling

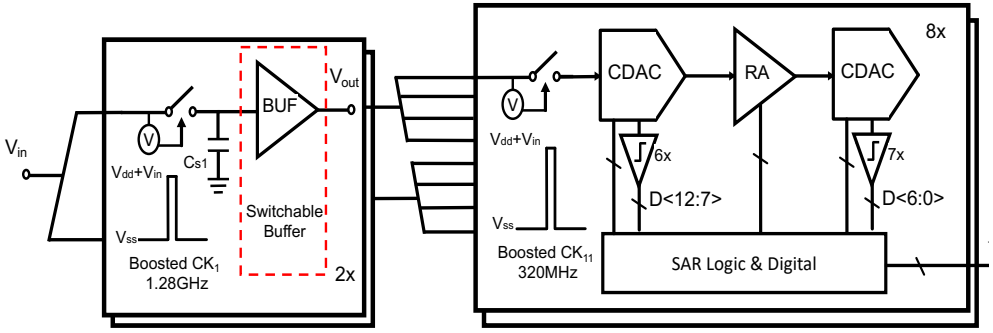
- Allow waveform analysis to derive optimal thresholds and correction algorithms during operation (few pixels)

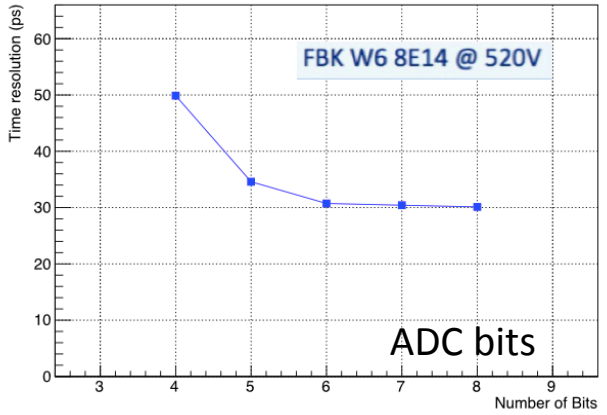




Design spec from Test Beam data analysis

Preamp output





ETROC waveform sampling using existing ADC design in 65nm. Being implemented by SMU EE (details see backup slides)

ETROC power estimates

Putting all of this design work together, here are the post-design power estimates.

Table 3.7: A summary of ETROC power consumption for each circuit component. The preamplifier, discriminator, and TDC values are obtained from post-layout simulation with conservative assumptions about occupancy and operating temperature. The SRAM and global circuitry power consumptions are conservative extrapolations from similar circuits used in the Altiroc.

Circuit component	Power per channel [mW]	Power per ASIC [mW]
Preamplifier (low-setting)	0.67	171.5
Preamplifier (high-setting)	1.25	320
Discriminator	0.71	181.8
TDC	0.2	51.2
SRAM	0.35	89.6
Supporting circuitry	0.2	51.2
Global circuitry		200
Total (low-setting)	2.13	745
Total (high-setting)	2.71	894

The estimated total power is less than 1W/chip spec, even for the worst case, for inner modules at 10% occupancy, and with preamp running at high power. → due to the low power feature of ETROC TDC design

Overall, the ETROC design provides a solution tuned to ETL specific needs for resolution, power budget, and radiation profile

Radiation Mitigation for ETL ASIC

- Radiation mitigation strategies in 65nm have been developed and extensively studied by RD53 for ATLAS and CMS tracking systems
  - TID/dose for inner and outer CMS trackers: 500 and 200Mrad
  - ETL TID/dose spec is: up to 100Mrad (highest eta modules)
- The radiation mitigation for ETROC: adopting the established techniques by RD53 and lpGBT
  - TID: overall follow the strategies developed by RD53
    - To minimize the TDC delay cell time spread and drifts, the ELT (Enclosed Layout Transistor) technique is used for ETROC TDC
  - SEE: TMR, and follow the RD53 "trickle configuration" method to minimize any residual effects

For details, see MTD/ETL CDR

Schedule and Cost

ETROC Development Plan & Schedule

ETROC0: **1x1 pixel channel with preamp + discriminator (submitted Dec 2018, chip in March 2019)**

Goal: core front-end analog performance

Chips shipping from CERN next week (backup slides)

ETROC1: **4x4 clock tree, preamp + discriminator + TDC. (ready June 2019)**

Goal: full chain front-end + TDC, 4x4 clock tree

ETROC2: **8x8, full functionality, and ¼ clock tree. (Q3 2020)**

Goal: supporting circuitries, 8x8 clock tree

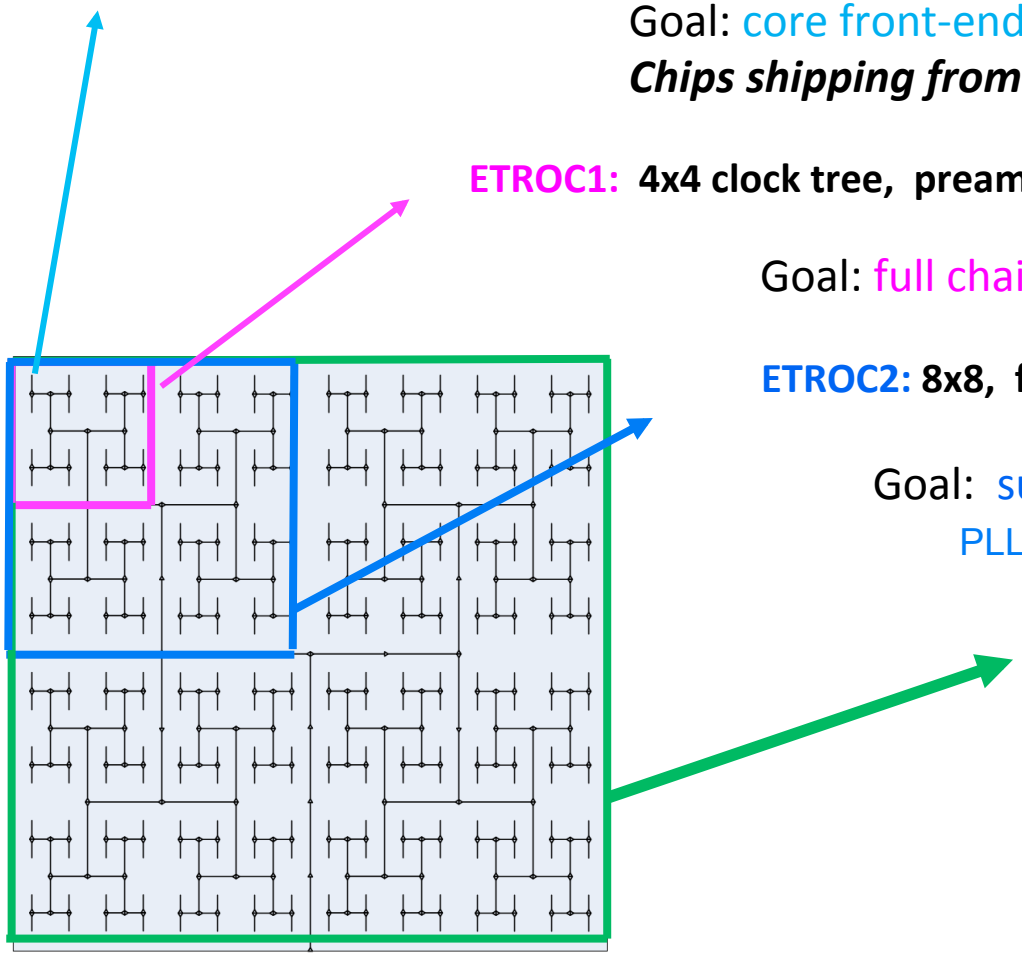
PLL, phase shifter, fast/slow control, I/O, L1 buffer…

ETROC3: **16x16 (full size): (Q1 2022)**

Goal: full size with full clock tree intended as pre-production ASIC

Production Q4 2022

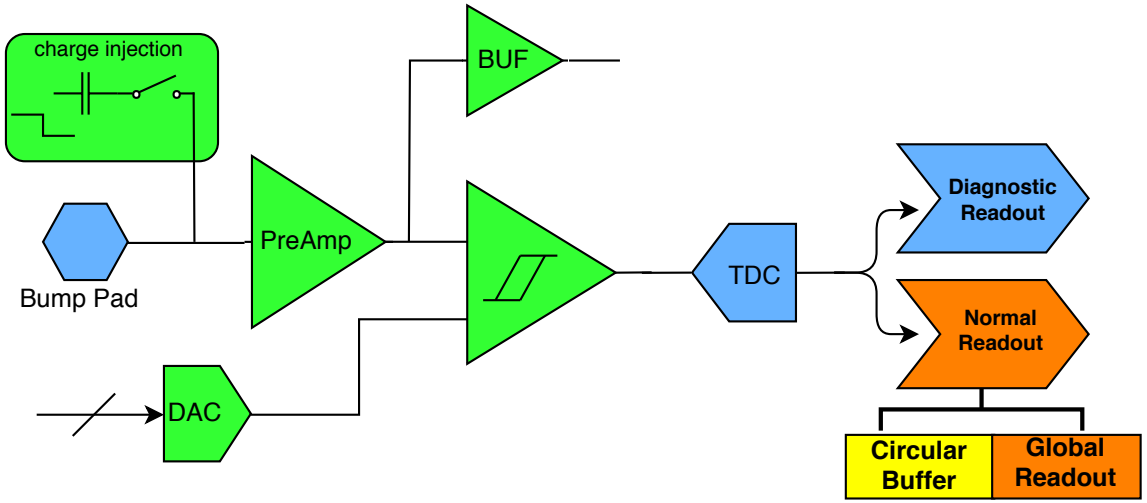
Two more revisions reserved in risk register (more on this later)

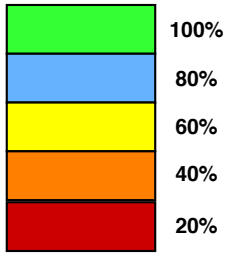


16 x 16 clock H-Tree

ETROC1 Building Blocks Status

Goal: design completion by June 2019





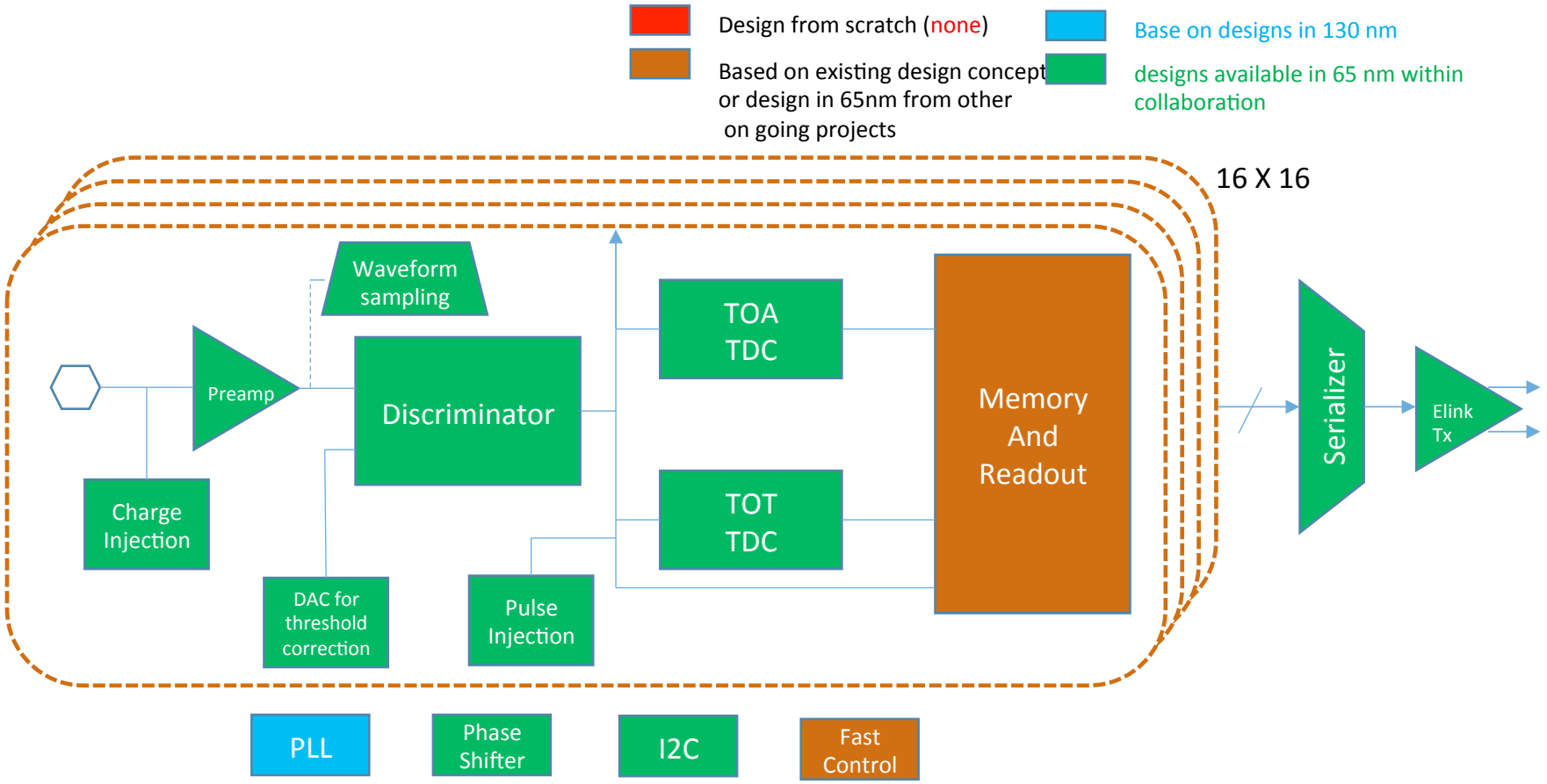
Reference Generation	eLinkTx	eLink Rx	Phase Shifter
PLL	Clock Generation	Clock Distribution	I2C

PLL/Phase shifter are optional test blocks for ETROC1

Most critical design blocks are implemented in ETROC1

Main design work after ETROC1

- Most of the critical design blocks are implemented in ETROC0 and ETROC1
  - The main tasks left after ETROC1: ***optimization and some supporting circuits***
- Most of supporting circuits are based on existing design concepts or designs
  - In fact, some common design blocks already available in 65nm (RD53, lp-GBT etc)



Costs: Endcap Timing Layer CMS-doc-13215

ETROC2 ETROC3

WBS	Direct M&S ($)	Labor (Hours)	FTE	Direct + Indirect + Esc. ($)	Estimate Uncertainty ($)	Total Cost ($)
CD1-v2-DR-402.8 402.8 TL - Timing Layer	**6,561,457**	**161764**	**91.50**	**11,364,763**	**3,026,706**	**14,391,469**
CD1-v2-DR-402.8.2 TL - Management	**433,000**	**26520**	**15.00**	**568,714**	**144,562**	**713,276**
CD1-v2-DR-402.8.3 BTL - Barrel Timing Layer	**3,352,236**	**49800**	**28.17**	**5,410,860**	**1,318,476**	**6,729,336**
CD1-v2-DR-402.8.4 ETL - Endcap Timing Layer	**2,776,221**	**85444**	**48.33**	**5,385,188**	**1,563,669**	**6,948,857**
CD1-v2-DR-402.8.4.1 ETL - LGAD Sensors	**0**	**3872**	**2.19**	**0**	**0**	**0**
CD1-v2-DR-402.8.4.1.1 ETL - LGAD Sensors - R&D and Prototypes	**0**	**2400**	**1.36**	**0**	**0**	**0**
CD1-v2-DR-402.8.4.1.2 ETL - LGAD Sensors - Pre-Production and Production	**0**	**1472**	**0.83**	**0**	**0**	**0**
CD1-v2-DR-402.8.4.2 ETL - Frontend ASICs	**1,922,500**	**22588**	**12.78**	**3,874,081**	**1,039,579**	**4,913,660**
CD1-v2-DR-402.8.4.2.3 ETL - Frontend ASICs v2 development	**256,000**	**14634**	**8.28**	**1,474,236**	**556,360**	**2,030,596**
CD1-v2-DR-402.8.4.2.4 ETL - Frontend ASICs v3 development	**1,666,500**	**7954**	**4.50**	**2,399,845**	**483,219**	**2,883,064**
CD1-v2-DR-402.8.4.3 ETL - Assembly	**680,860**	**30088**	**17.02**	**1,145,013**	**397,283**	**1,542,296**
CD1-v2-DR-402.8.4.3.1 ETL - Assembly R&D and Prototypes	**268,660**	**19164**	**10.84**	**488,722**	**152,824**	**641,546**
CD1-v2-DR-402.8.4.3.2 ETL - Module Assembly Pre-production	**62,000**	**626**	**0.35**	**91,721**	**25,958**	**117,679**
CD1-v2-DR-402.8.4.3.3 ETL - Module Assembly Production	**350,200**	**10298**	**5.82**	**564,569**	**218,501**	**783,070**
CD1-v2-DR-402.8.4.4 ETL - System Testing	**79,561**	**6322**	**3.58**	**103,418**	**38,340**	**141,759**
CD1-v2-DR-402.8.4.4.1 ETL - System Testing - Prototyping	**60,448**	**1898**	**1.07**	**79,459**	**30,061**	**109,520**
CD1-v2-DR-402.8.4.4.2 ETL - System Testing - Preproduction	**9,584**	**1878**	**1.06**	**12,004**	**4,154**	**16,158**
CD1-v2-DR-402.8.4.4.3 ETL - System Testing - Production	**9,529**	**2546**	**1.44**	**11,955**	**4,125**	**16,080**
CD1-v2-DR-402.8.4.5 ETL - Integration and Commissioning	**93,300**	**22574**	**12.77**	**262,676**	**88,467**	**351,143**
CD1-v2-DR-402.8.4.5.1 ETL - I&C - Assembly Setup	**0**	**1768**	**1.00**	**0**	**0**	**0**
CD1-v2-DR-402.8.4.5.2 ETL - I&C - Assembly	**93,300**	**14434**	**8.16**	**164,318**	**39,288**	**203,606**
CD1-v2-DR-402.8.4.5.3 ETL - I&C - Cold Testing	**0**	**1888**	**1.07**	**20,355**	**10,178**	**30,533**
CD1-v2-DR-402.8.4.5.4 ETL - I&C - Mount ETL on EC	**0**	**948**	**0.54**	**78,003**	**39,001**	**117,004**
CD1-v2-DR-402.8.4.5.5 ETL - I&C - Commissioning	**0**	**3536**	**2.00**	**0**	**0**	**0**

Note: ETROC0 & ETROC1 work are off project, supported by Ops-funded initial detector R&D

Cost Drivers: Timing Layer

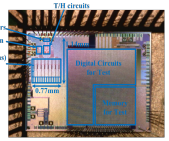
CMS Driver	Labor (FTE-yrs)	Labor (M$)	M&S (M$)	Labor + M&S (M$)	Estimate Uncertainty (M$)	Total (M$)	
TL - ETL frontend ASIC development (v3) - M&S	0.0	0.0	1.9	1.9	0.3	2.2	ETROC3
TL - ETL frontend ASIC prototyping (v2) - Labor	7.7	1.2	0.0	1.2	0.5	1.7	ETROC2
TL - ETL module assembly	11.3	0.3	0.8	1.1	0.4	1.5	
TL - BTL LYSO crystals [CORE]	0.0	0.0	1.2	1.2	0.2	1.4	
TL - BTL assembly	10.8	0.6	0.4	1.0	0.4	1.4	
TL - BTL SiPM production [CORE]	0.0	0.0	1.0	1.0	0.2	1.2	
TL - BTL Concentrator Cards - production	1.6	0.2	0.5	0.7	0.2	0.9	
TL - ETL frontend ASIC development (v3) - Labor	3.7	0.5	0.0	0.5	0.2	0.7	ETROC3
TL - BTL SiPM QC labor	3.0	0.5	0.0	0.5	0.1	0.6	
TL - BTL installation and commissioning	3.0	0.1	0.2	0.3	0.1	0.4	
TL - Management Travel and misc. support M&S	0.0	0.0	0.3	0.3	0.0	0.4	
TL - BTL Concentrator Cards - prototyping and preproduction	1.3	0.2	0.1	0.3	0.1	0.4	
TL - ETL installation and commissioning	1.1	0.2	0.1	0.3	0.1	0.4	
TL - ETL frontend ASIC prototyping (v2) - M&S	0.0	0.0	0.3	0.3	0.0	0.3	ETROC2
TL - iCMS common infrastructure [CORE]	0.0	0.0	0.2	0.2	0.1	0.3	
TL - BTL system testing	0.1	0.0	0.1	0.1	0.0	0.2	
TL - ETL system testing	0.0	0.0	0.1	0.1	0.0	0.1	
TL - BTL SiPM NRE and preproduction SiPMs [CORE]	0.0	0.0	0.1	0.1	0.0	0.1	
TL - BTL SiPM prototyping and preproduction - misc.	0.0	0.0	0.1	0.1	0.0	0.1	
TL - BTL LYSO travel and COLA	0.0	0.0	0.1	0.1	0.0	0.1	
TL - BTL SiPM travel and shipping	0.0	0.0	0.1	0.1	0.0	0.1	

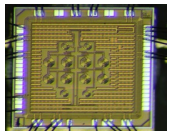
PM = Project Management **OT = Outer Tracker** **CE = Calorimeter Endcap** **TD = Trigger and DAQ** **TL = Timing Layer**

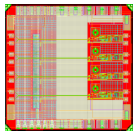
Contributing Institutions and Resource Optimization

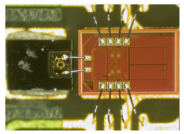
Contributing Institution: SMU EE

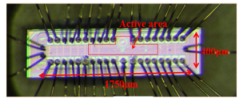
- Ping Gui's group: extensive experience on high-speed ADC design
  - Successfully demonstrated 56 GS/s & 1 GS/s 8-bit ADC using 28nm CMOS
- Experiences rad-hard design using 65nm and 28nm
- Extensive collaboration with HEP since 2007
  - FNAL: *ETROC*, DUNE, VIPRAM,
    - ColdPLL and serializer and line driver
    - *ETROC Waveform sampler, clock tree distribution etc*
  - CERN: GBT, LpGBT, and VL+ projects
    - Phase Shifter for GBT, 5Gbps GBTIA (optical receiver), 10Gbps GBLD10 and LDQ10 (4x10Gbps), *E-Links* for LpGBT
- Current graduate students experienced in *high-speed ADC and PLL* design (for *ETROC*)

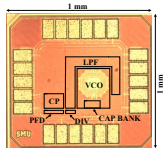

56GS/s ADC


GBLD10

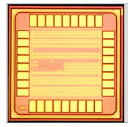

LDQ10


GBPTA


LpGBLD



COLD PLL


12-bit ADC for ETROC

Waveform sampler

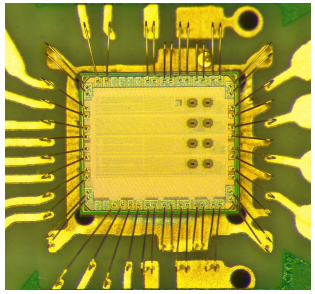
Contributing Institution: SMU Physics

- SMU Physics Electronics Group (Opto-electronics lab) past and current projects
  - The ATLAS LAr front-end-board (FEB). The whole system has 1,624 fiber channels, each for one FEB. Still in operation.
  - Optical links for LAr trigger upgrade in LS2 (phase-1).
    - Have developed two serializer ASICs (LOCx2 and LOCx2-130), one VCSEL driver (LOCld), two optical modules: MTx and MTRx, and two link systems, the data link based on LOCx2, MTx and the control link based on GBTx and MTRx. 40 fiber channels for each LTDB (the trigger board on detector front-end), and a total of 124 LTDB will be installed in ATLAS.
  - Optical link for LAr readout upgrade in LS3 (phase-2). This link will be lpGBT and VTRx+ based.
  - ATLAS ITK-pixel: developing a cable receiver ASIC with programmable equalization.
  - Contribute to the design of the Altiroc ASIC for ATLAS HGTD.
  - A member in the common projects of lpGBT, Versatile Link and VL+.
  - ***Collaboration in the design of ETROC ASIC for CMS ETL***
    - ***Front-end, TDC, phase shifter, supporting circuits, chip testing etc***

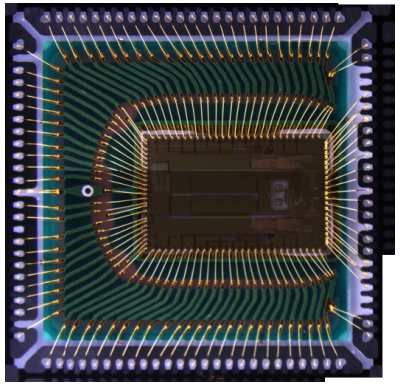
SMU Opto-electronics Lab (since 1998)

Charge #4

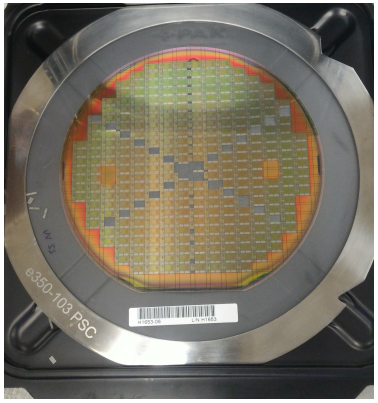
Some recent work

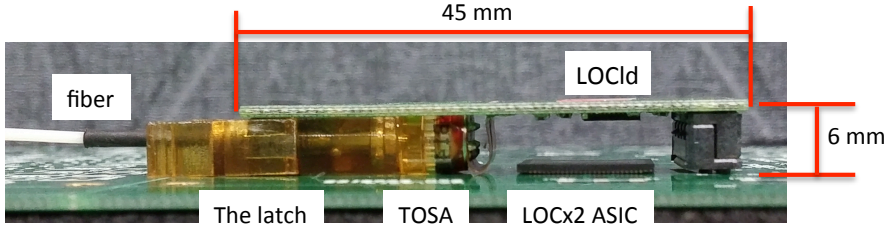


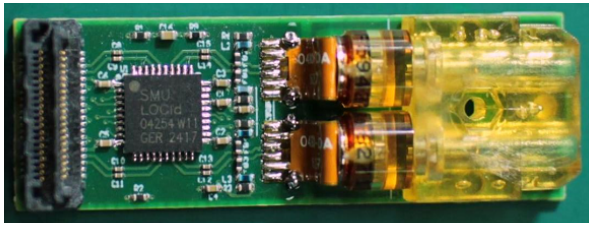
cpVLAD



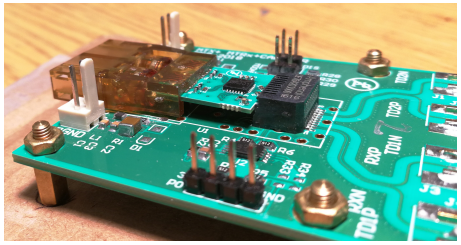
LOCx2

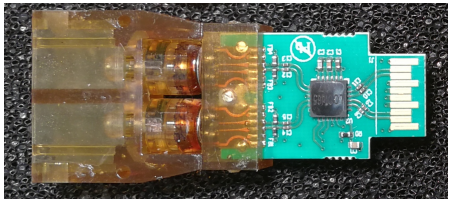


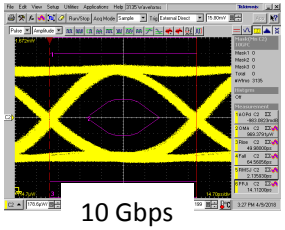


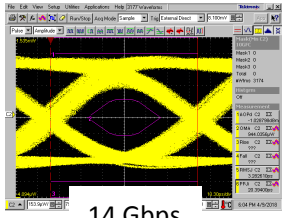


A photo of MTx.
The next version MTx+, coming out in 2 months, will triple the current speed.









Current ETL ASIC Team for ETROC

- FNAL Electrical Engineer Department (EED):
  - Quan Sun (Full time key designer for ETROC), with support from FNAL ASIC group
  - Support from FNAL EED
    - Jin-yuan Wu (TDC expert for FPGA with decade long experience in TDC)
    - Jamieson Olsen (expert in system/board/FPGA design)
- SMU.Physics (Opto-electronics Lab)*:*
  - Datao Gong (senior ASIC designer, analog & digital)
    - Designer of LOCx2, LOCld and GBCR. Involved in lpGBT and ALTIROC
    - ETROC: Front-end and supporting circuits
  - Four PhD EE students full time on ETROC
  - *Andy Liu (system/board designer), focus on chip testing*
- SMU.EE: 3 PhD students (full time) + professor (Ping Gui)
  - Extensive experiences in ADC/PLL design… collaboration with HEP
  - ETROC: Implementation of waveform sampling
  - ETROC: Clock distribution for full size chip
- ETROC project god-parent committee:
  - Carl Grace (LBNL, Chair), Fukun Tang/ Eric Oberla (UofChicago), Gary Varner (Hawaii), Christine Hu (Strasbourg/France), Ron Lipton/Dave Christian (FNAL)

A group of physicists (FNAL/Caltech/UCSB/Kansas) have been heavily involved in waveform analysis using LGAD beam test data as well as LGAD simulation data.

Crucial for developing the ETROC specification optimized for ETL.

Risk Register: CMS-doc-13480

- ETL-specific risks/threats:

Risk Type : Threat (11)						
3 (High)	RT-402-8-01-D	ETL - Additional FE ASIC prototype cycle is required	50 %	4 -- 5 -- 6 months	500 -- 600 -- 700 k$	300
2 (Medium)	RT-402-8-03-D	ETL - FE ASIC does not meet specs - needs another pre-prod run	10 %	6 -- 7.5 -- 9 months	914 -- 970 -- 1026 k$	97
2 (Medium)	RT-402-8-02-D	ETL - Problems with ETL module assembly facility	50 %	1 months	30 k$	15
2 (Medium)	RT-402-8-10-D	ETL - Sensor quality problem during production	15 %	2 -- 3 -- 6 months	28 -- 52 -- 109 k$	9
1 (Low)	RT-402-8-53-D	ETL - Integration facility at CERN runs out of components	25 %	3 months	21 k$	5
1 (Low)	RT-402-8-48-D	ETL - Delay in delivery of parts from iCMS	20 %	1 months	10 -- 20 -- 30 k$	4
1 (Low)	RT-402-8-31-D	ETL - Storage-related degradation of LGADs	10 %	3 months	18 k$	2
1 (Low)	RT-402-8-52-D	ETL - Module Radiation Tolerance	10 %	1 months	15 k$	2
1 (Low)	RT-402-8-49-D	ETL - Delays or damage in transport of ETL modules to CERN	5 %	1 months	10 k$	1
1 (Low)	RT-402-8-50-D	ETL - Module assembly yield is low	10 %	0 -- 0 -- 1 months	0 -- 5 -- 15 k$	1
1 (Low)	RT-402-8-51-D	ETL - Problem with AlN vendor	5 %	1 -- 2 -- 3 months	0 -- 15 -- 30 k$	1

Timing Layer Risks CMS-doc-13480

This example slide shows the risk data for one single risk, copy-pasted from the PDF risk register:
CMS-doc-13480 https://cms-docdb.cern.ch/cgi-bin/DocDB/ShowDocument?docid=13480

Use this slide template to create more slides for relevant high/medium rank risks

RT-402-8-01-D ETL - Additional FE ASIC prototype cycle is required

Risk Rank:	3 (High) **Scores:** Probability : 4 (H) ; Cost: 2 (M) Schedule: 2 (M))	**Risk Status:**	Open
Summary:	This risk can have multiple causes. 1) If the necessary performance (precision vs power consumption) is not achieved during the last prototype cycle, an additional prototype cycle may be necessary causing a delay and incurring a cost increase. 2) ASIC specification has changed due to external reasons, such as lpGBT clock distribtution does not meet specifications.		
Risk Type:	Threat	**Owner:**	Tiehui Liu
WBS:	402.8.4 ETL - Endcap Timing Layer	**Risk Area:**	Technical Risk / Reliability or Performance
Probability (P):	50%	**Technical Impact:**	0 (N) - negligible technical impact
Cost Impact:	PDF = 3-point - triangular Minimum = 500 k$ Most likely = 600 k$ Maximum = 700 k$ Mean = 600 k$ P * <Impact> = 300 k$	**Schedule Impact:**	PDF = 3-point - triangular Minimum = 4 months Most likely = 5 months Maximum = 6 months Mean = 5 months P * <Impact> = 2.5 months
Basis of Estimate:	The cost for a MPW run is 400k, and we include 100-300k for additional engineering.		
Cause or Trigger:	Prototype 2 does not meet requirements and we cannot include changes in the preproduction submission.	**Impacted Activities:**	Risk could delay completion of ASIC prototyping
Start date:	1/Mar/2020	**End date:**	1/Jan/2022
Risk Mitigations:	We have increased the effort for the design simulation and verification.		
Risk Responses:	We include an additional prototype cycle.		
More details:			

Summary of ETL ASIC (ETROC)

- The challenge of small signal size after irradiation for high eta
  - This is accomplished with a mix of the 2 hit detector layout optimization and the targeted design optimization for the ASIC
- Have built a strong design team that is making rapid technical progress, using beam test and LGAD simulation inputs for design and performance optimization, reducing the design cycles
  - ASIC specification extensively studied and developed
  - Front-end design is advanced with good performance
  - Will test the first prototype chip (ETROC0) over next few weeks
  - Well on the way to complete the design of ETROC1
- R&D achieved
  - Critical front-end design optimized and implemented
  - Clock tree distribution advanced
  - Full chip design developed and documented
- R&D needed to be done before production
  - Validate/improve the front-end design with prototype chips
  - Implement the rest of supporting circuits

Concluding remark: rapid progress made since June 2018, with a strong design team, on the way for ETROC production Q4 2022

Quality Assurance and Quality Control

- The testing of ETROC design involves
  - ASIC standalone functional testing of prototype chips
  - Extensive irradiation campaign: TID and SEE tests
  - Testing with LGAD sensors
- ASIC standalone functional testing
  - Use internal charge injection method
  - Parameters to be measured includes:
    - PLL (jitter), phase shifter (nonlinearity)
    - TOA and TOT calibration
    - Maximal trigger rate
    - TOA/TOT precision versus input signal size and discriminator threshold, ENC
    - Power consumption etc
  - Define the QC selection criteria based on the results above
- TID test
  - Irradiate over a few steps, from 1Mrad to 100 Mrad
- SEE test in a beam setup (such as FNAL ITA: Irradiation Test Area)
  - Monitor the ASIC output, to measure the SEE rates
  - Study how the chip recovers with reset
  - Study how the minimize the SEE effects via trickle configuration
  - Make sure the design meet the requirements
- Testing with LGAD sensor in beam
- Production QA/QC

Quality Assurance and Quality Control

- Quality Assurance & Control plan documented in cms-doc-13093
- Quality Assurance: prevention of issues prior to the production of the final ETROC
  - Several prototype rounds are planned to identify potential problems and minimize the impact to cost or schedule
  - Progress is monitored by the iCMS through CMS Annual Reviews.
  - Test-beams, integration tests, radiation testing including operation of systems under irradiation and thermal cycling tests.
    - Achieved performance, in terms of the radiation tolerance, and achieved performance metrics are presented and agreed upon with the iCMS.
  - The decision and validation activities are discussed in weekly meetings within the US-CMS Electronics meeting among the US collaborators, and discussed with the iCMS colleagues in bi-weekly general MTD organization meeting.
- Quality control : Identification of issues
  - Before being diced into individual dyes, the ASIC will be probe-tested on wafers
  - Use databases to track all components through the assembly and testing processes
  - Verify that only good quality components (sensors, power and readout boards, and ASICs) are assembled into modules.

Slide form Artur Apresyan (L3 talk)

Responses to Previous Reviews

- R37: MIP: ETL—Allocate sufficient expert ASIC design engineering resources to ensure meeting the requirements on the ASIC design schedule.

A redesign of the ETL FE ASIC workplan and schedule has been completed. The engineering resources are understood and mapped to **identified individuals with appropriate expertise and bandwidth** to complete this project in the coming years. An **external review team** has being assembled to focus specifically on the ETL FE ASIC.

  - Status: Closed 15 February 2019

From the Technical Review closeout:
"...the ASICS team is world class, and as capable to succeed as any assembled."

Slide from
Chris Neu
(L2 talk)

Responses to Previous Reviews

- R34: MIP: ASIC design for the ETL system is at an early stage.... A strategy for the delivery of a baseline design has to be developed. In case of delays in the final design that require additional ASIC submissions the float can be utilized or installation can be delayed beyond LS3 and the impact on the cost of this part of the project would need to be assessed.

  A redesign of the ETL FE ASIC workplan and schedule has been completed. The strategy for prototyping and providing a **baseline functional prototype by the time of CD-2 is now defined**. Updated milestones are defined and an external review team has been assembled to focus specifically on the ETL FE ASIC and participate in a series of dedicated focused reviews. **The milestones for the ASIC design have been discussed and decided by the MTD project.** They are documented in the Technical Design Report that is now under internal review within the collaboration and will be reviewed by the LHCC in April. The development milestones are:

  - submission in summer 2019 of a 16 channel prototype (ETROCv1), with the core components impacting timing resolution;
  - submission in October 2020 of a 64 channel prototype (ETROCv2) with full functionality;
  - submission in February 2022 of a pre-production ASIC.

  The baseline installation schedule of the project contains 6 months of float beyond these ASIC milestones, and additional float is afforded by the detector's design **allowing installation even during a later year-end technical stop**. In case of functionality problems identified in the pre-production ASIC, an additional mask set could be required for the production run. The cost impact of this possibility **is included in the project's risk calculation**.

  - Status: Closed 30 October 2018

Slide
from Chris Neu
(L2 talk)

Responses to Previous Reviews

- ETL-R1: It is crucial to follow the schedule of beam test and/or system integration tests to verify functionality of the LGAD/ ROC/Back-end systems
  - A series of systems tests at each major stage of development for the ETL (final engineering prototype, pre-production prototype, and production modules) are being developed. The mechanical, thermal, electrical, and data integrity of ETL sensor modules affixed to their expected mechanical structures will be examined at each of these stages and then validated to the furthest extent possible. The results will be reported as recommendations for the next stage of ETL prototyping. Realistic backend electronics for read out and slow control will be used as soon as they are available in the testing procedures. Specific attention will be paid to developing a full sensor-to-DAQ chain of ETL with multiple modules using lpGBTs as soon as possible to identify scaling issues. This series of systems test will culminate in beam testing of the production modules to verify module timing performance before and after burn-in, in addition to other stress tests of the system.

Slide
from David Stuart' talk

Responses to Previous Reviews

- ETL-R2: Identify alternative ASIC solutions from existing or potentially viable prototypes of other systems, and create a decision matrix for breakpoints in the ETLROC development in case that device falls behind in the development schedule or fails to function as required.
  - The potential use of alternative ASIC solutions comes into play in two ways: (1) as a ROC to use for early sensor and module prototyping over the next two years, and (2) as a ROC to use for production of the final detector. For the early prototyping phase, we have designed test boards using the SKIROC2 ASIC to read out large prototype LGAD sensors and test bump-bonding performance with sensors bonded to interposers. These boards are now being manufactured and provide a flexible suite of beam and bench test capabilities, including compatibility with previously used discrete component electronics. A second option for these tests is to use recent, early prototypes of the ALTIROC ASIC being designed for the ATLAS High Granularity Timing Detector (HGTD). We have discussed plans for shared testing of these prototypes with the HGTD project management and there is close collaboration on beam tests at Fermilab. (continued…)

Slide from David Stuart' talk

Responses to Previous Reviews

- ETL-R2: Identify alternative ASIC solutions from existing or potentially viable prototypes of other systems, and create a decision matrix for breakpoints in the ETLROC development in case that device falls behind in the development schedule or fails to function as required.
  - For the final detector production phase, the ALTIROC ASIC could be a viable alternative if it achieves sufficiently low power and time resolution for small amplitude signals but it turns out that the ETROC does not. Discussions between the ALTIROC and ETROC design teams have shared the designs and the performance results from post-layout simulation and from beam and test bench measurements. The results from the first ALTIROC prototype have informed improvements implemented in the preamp design of the ETROC, and results of the first ETROC prototype will be fed back to the ALTIROC designers. This collaboration will help each ASIC optimize for the respective detector needs and mitigate the risk of delays from design errors. If either ASIC project encounters fundamental functional problems, this collaboration will ease adoption of aspects from the other project, including the possibility of adopting the other ASIC, or a small modification thereof. The breakpoints for such a decision are set by the prototyping schedule. For ETROC, prototypes of the pre-amp and discriminator stage will be available in summer 2019. A 1/16th scale prototype is expected in 2020, including all stages critical to the timing resolution performance. A 1/4 scale prototype is planned for early 2021 with full functionality. Each of these prototyping steps provides a breakpoint for cross-adoption of designs or components between the ALTIROC and ETROC ASICs.

Slide from David Stuart' talk

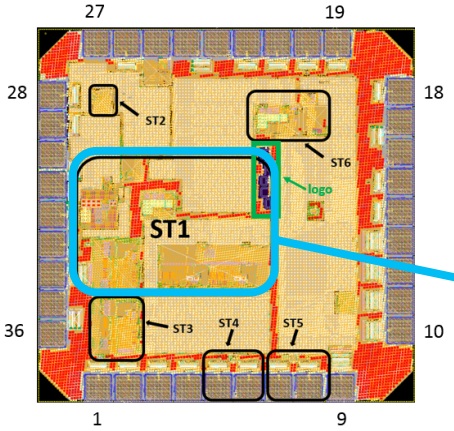
Responses to Previous Reviews

- ETL-R3: Identify criteria for acceptable SEE rates in the ETLROC and possible error mitigation schemes.
  - The criteria for acceptable SEE rates differs for effects corrupting data bits and configuration bits, where the former is expected to be negligible. Mitigation of SEE effects on configuration bits is being incorporated in the ETROC design using the standard Triple Modular Redundancy approach, with majority logic. The design takes care to spatially separate the replicas to reduce correlated effects, and the use of a time delay between replicas is being investigated to further reduce correlated effects. To reduce the impact of SEE events that do affect the configuration bits, the approach taken in the RD53 chip design will be used, which implements a “trickle reconfiguration” to frequently refresh the configuration memory during data taking. The efficiency impact from SEE-based memory corruption will be simulated to define criteria for acceptable SEE rates, and ion beam facilities will be considered as a way to measure the rates.

Slide
from David Stuart’ talk

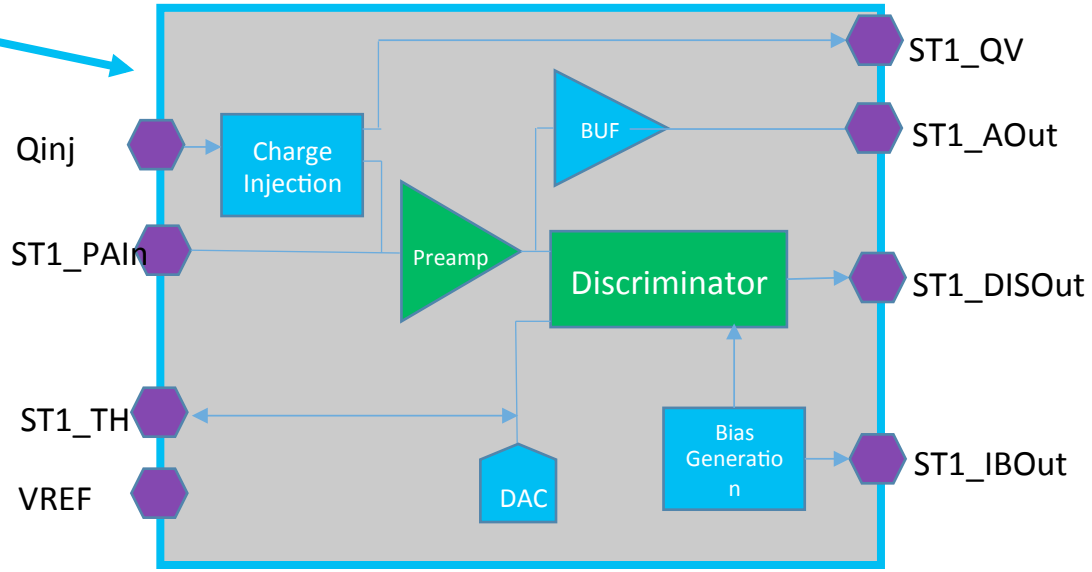
ETROC0: the First Prototype Chip

ETROC0 chip

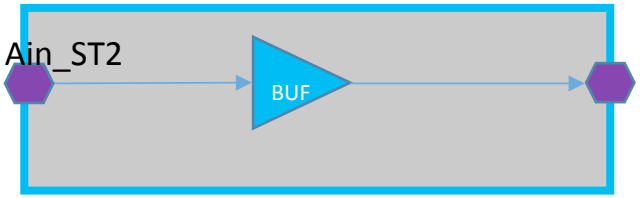


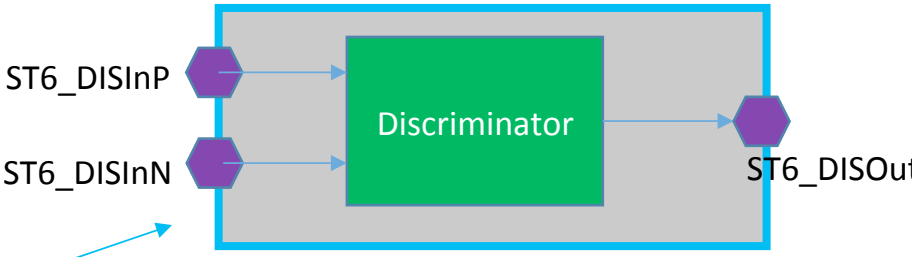
Submitted Dec 2018
Chip delivery next week

Test structure ST1: the full chain

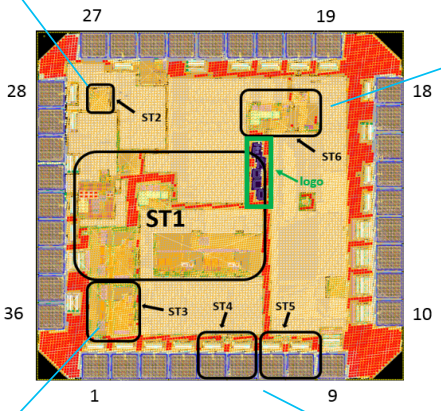


ETROC0: Designed for full testability

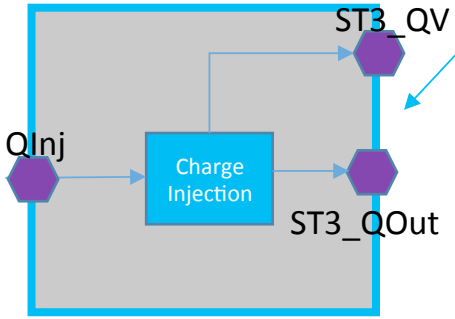




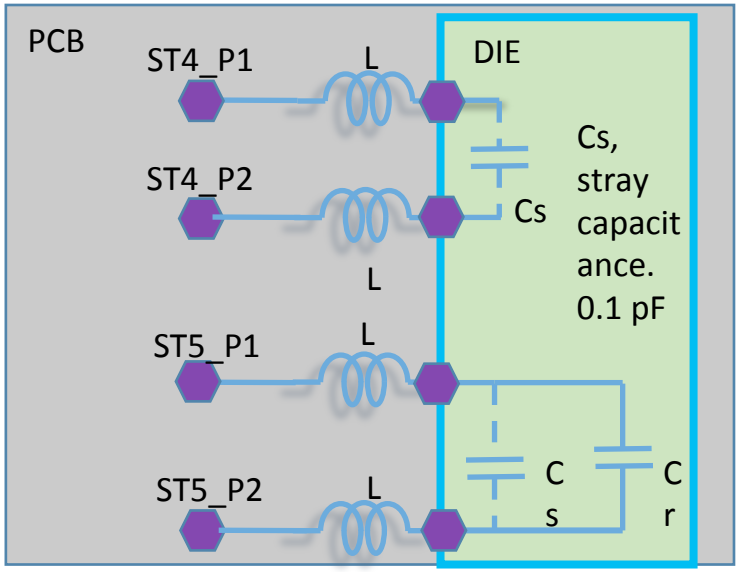
All individual blocks can be tested separately



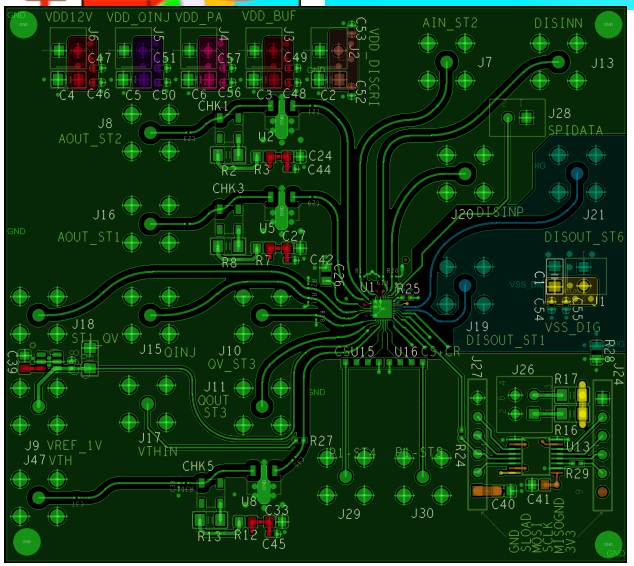
ETROC0



Cr, replica capacitor, a copy of the capacitor for charge injection.

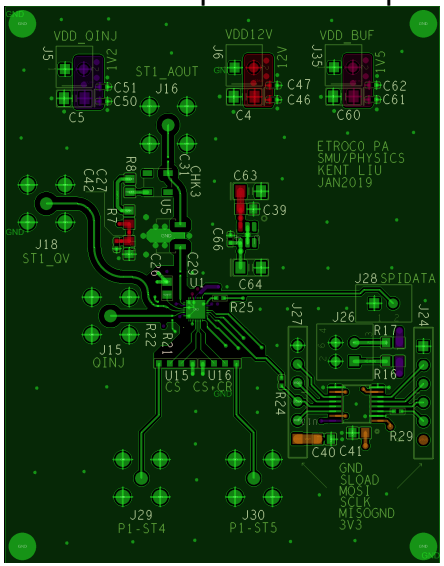


ETROC0 testing boards design

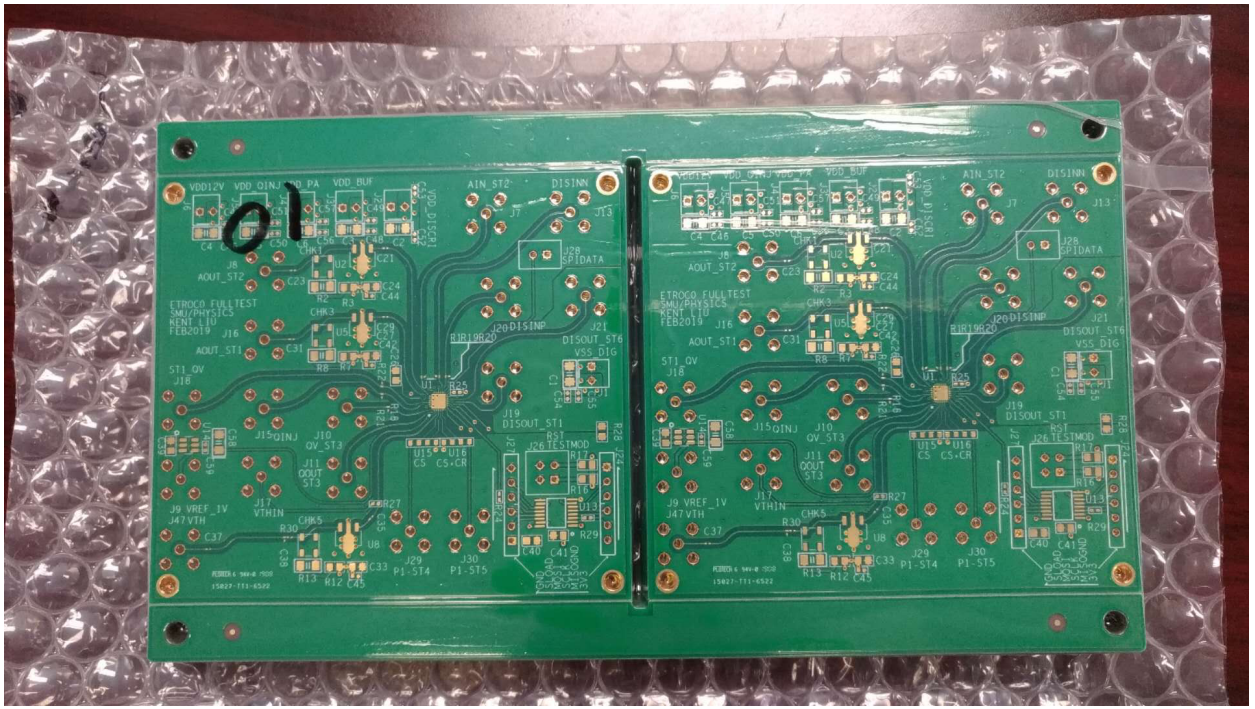


Test board with full test functionalities

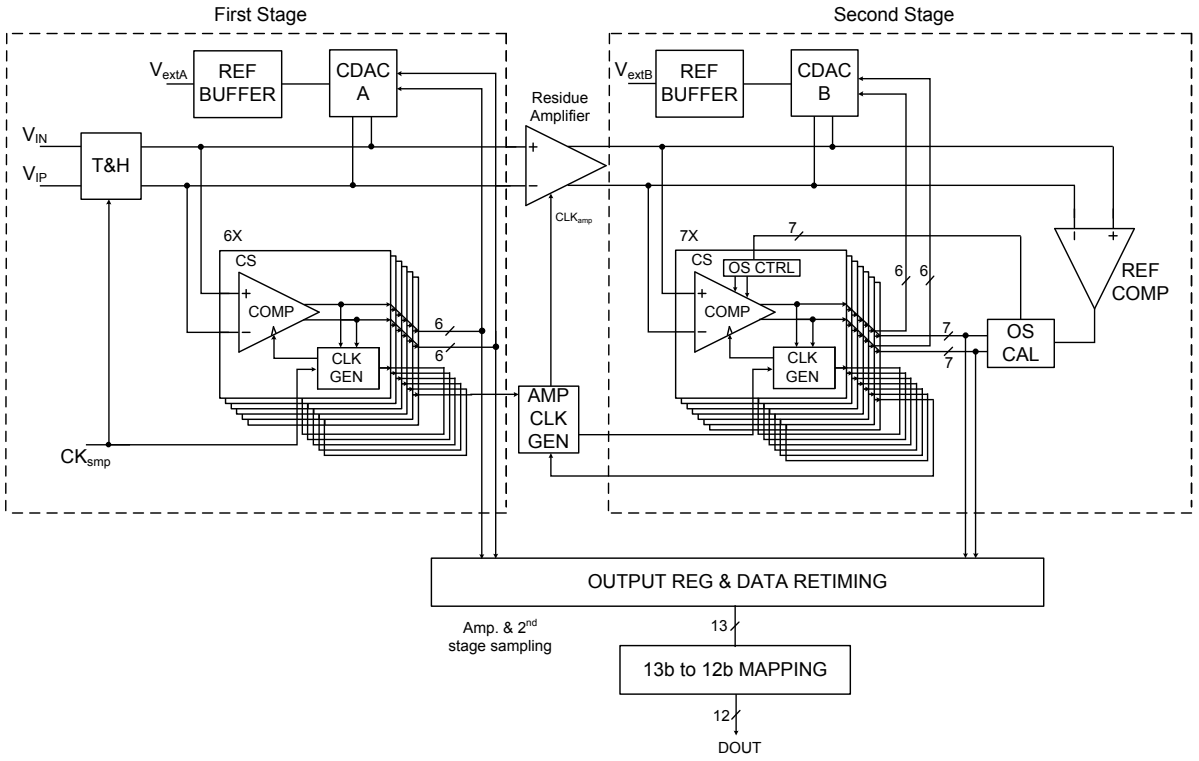
Test board optimized for preamp testing



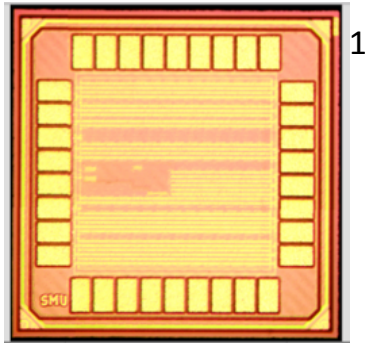
ETROC0 test boards arrived early March 2019



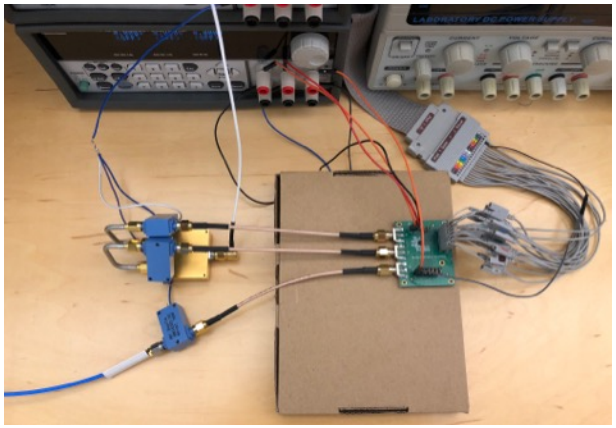
ADC originally designed by SMU/EE for 5G communication → ultra low power



Mini-ASIC ADC prototype designed and tested by SMU EE (2018)

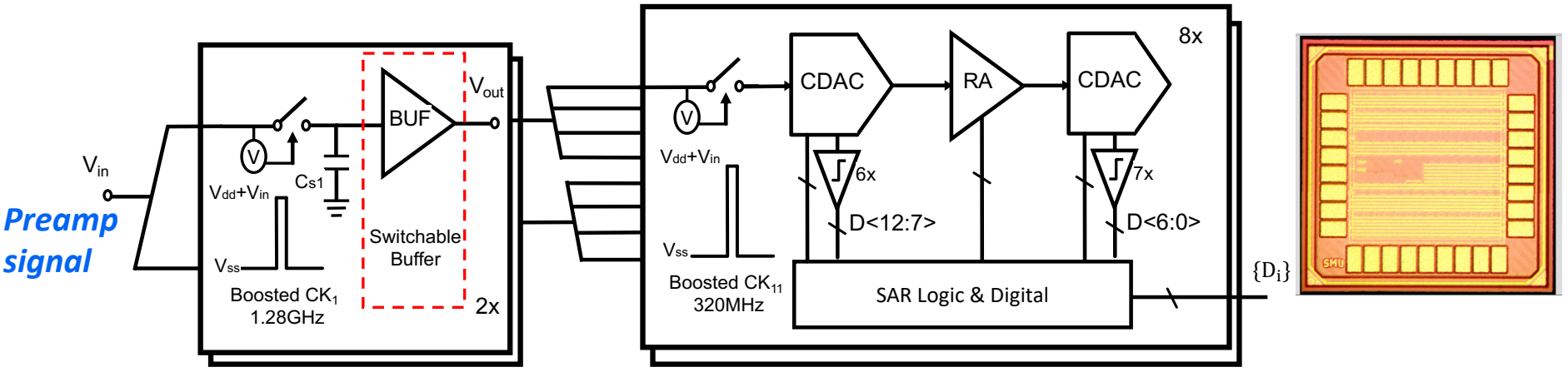


1mm x 1mm



The ETROC waveform sampler is based on the ADC design in 65nm by SMU EE

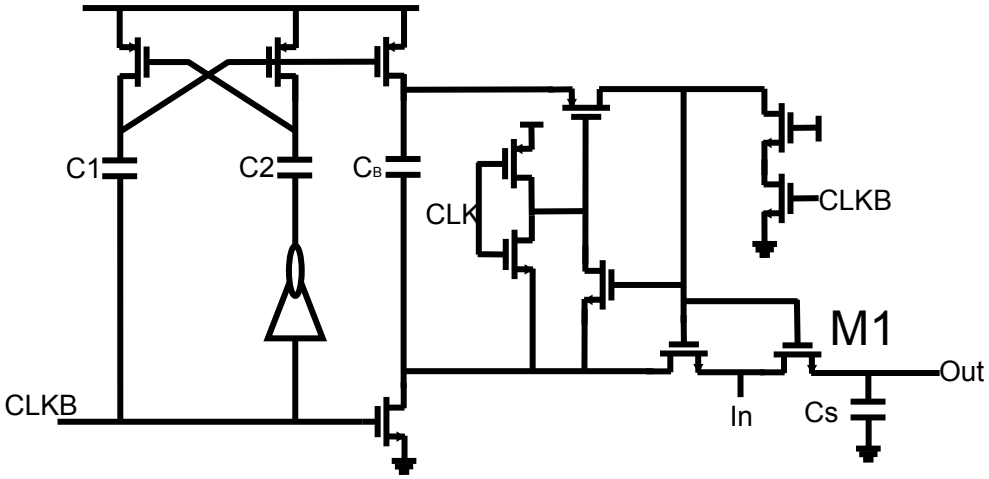
ETROC Waveform Sampler –- Overall Architecture



2.56GS/s 12-bit waveform sampler (WS) interleaving 8 ADC channels

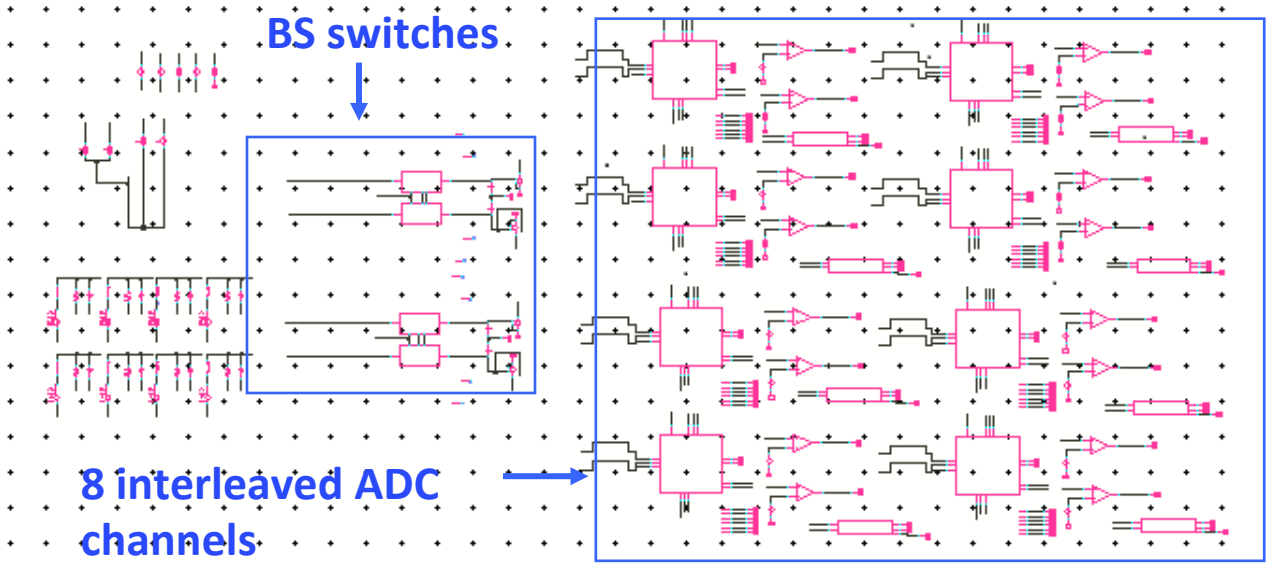
- ***Overall architecture studied and finalized***
- **Two-stage sampling structure to achieve both high sampling rate (2.56GS/s) and high-resolution (12-bit)**
- **Each channel using pipelined SAR for optimized resolution and sampling rate**
- ***Single-channel design measured on silicon***

Waveform Sampler Design –- Bootstrapped Sampling Switch

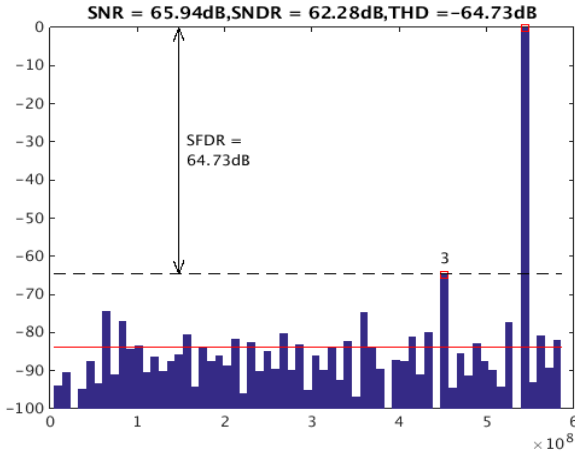


- Sampling switches are critical in determining the overall WS resolution and speed
- 12-bit resolution is in part limited by the linearity of the sampling switches
- Bootstrap (BS) circuit is designed in the two-stage sampler to improve linearity of sampling switch M1
- BS reduces the signal-depend nonlinearity of the switches by keeping the turn-on voltage constant as Vdd
- Vgs being kept as Vdd also ensures high sampling speed

Waveform Sampler Design –- Overall WS Design & Simulations



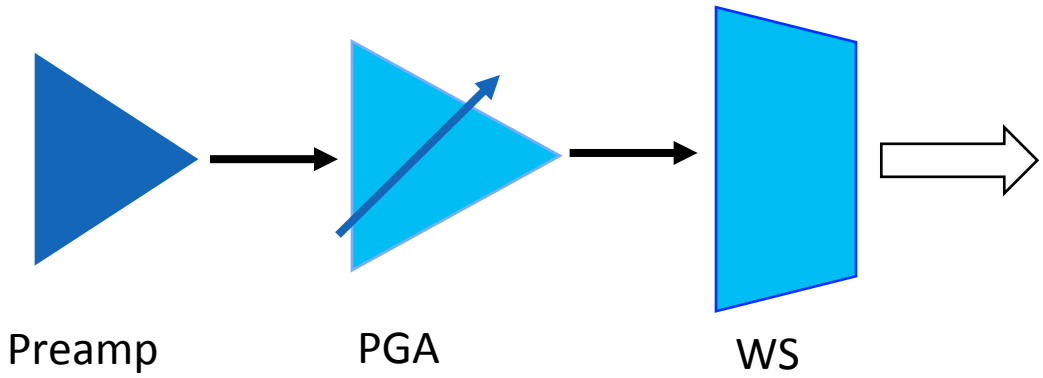
Overall design of the WS consisting of sampling stages and interleaving 8 channels



Simulated SNDR for 2.56GS/s

- WS interleaving 8 of 12-bit pipelined SAR channels with bootstrap switches in the sampling stages has been simulated
- Simulation of the WS shows 62dB SNDR (ENOB of 10bit) at 2.56GS/s

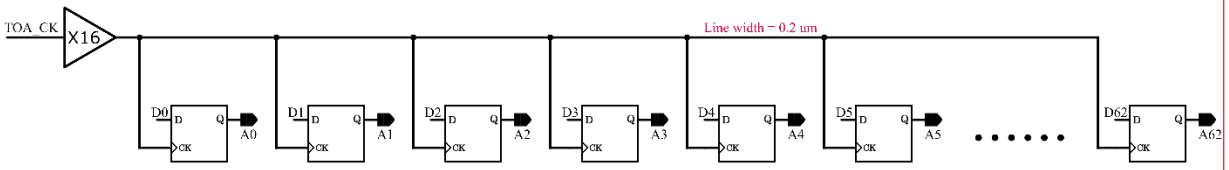
Waveform Sampler Design –- Other On-going Design

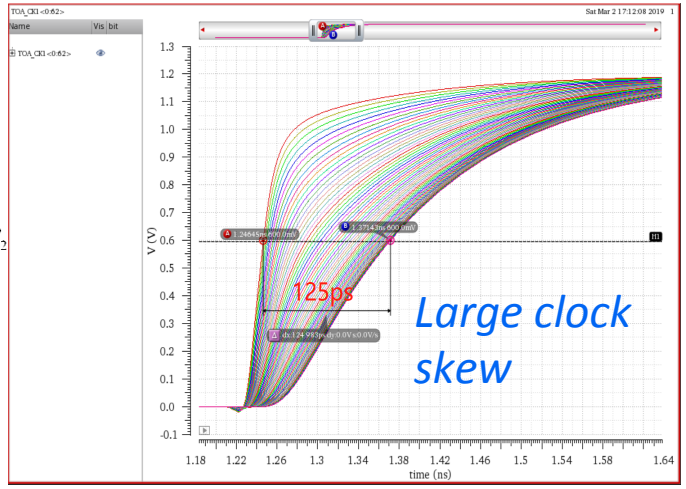


- **To interface with the preamplifier, a programmable gain amplifier (PGA) is currently being designed to amplify signals on the level of tens of mVs from the preamp to the full scale range of ADC**
- **Reference buffers are being designed to provide steady reference voltages for each of the 8 ADC channels**
- ***WS is currently being optimized and laid out***
- ***Expected a taped-out (mini-ASIC) in June 2019 for the waveform sampler block***

TDC delay line optimization

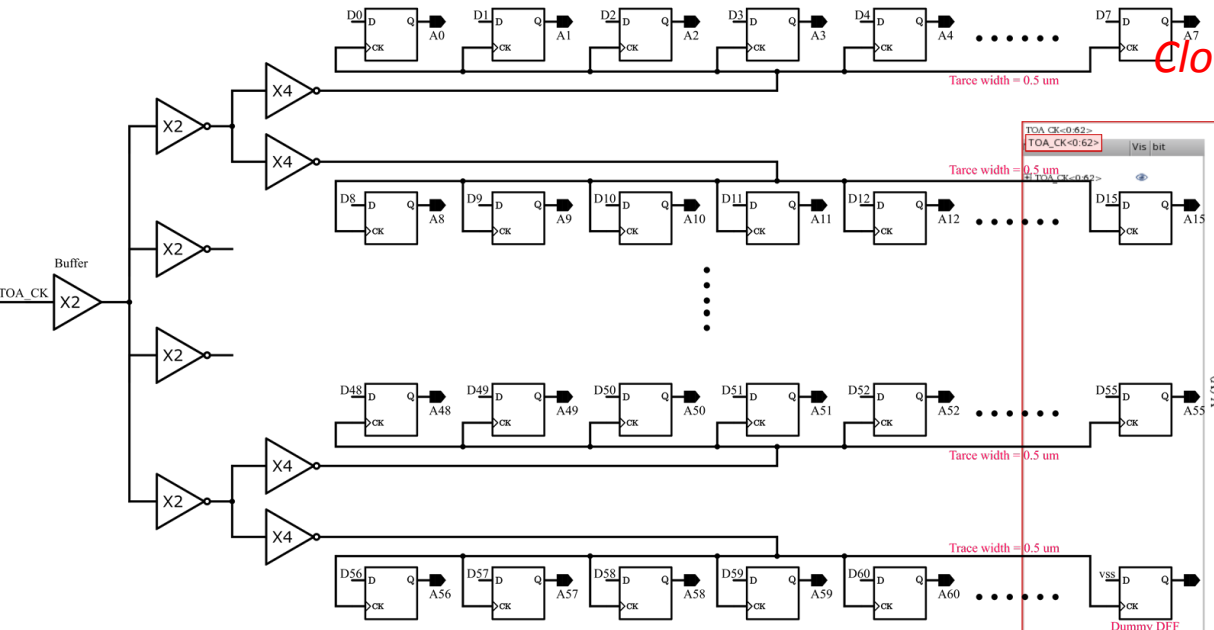
One clock driver for all TOA DFFs with single trace at 0.2um width

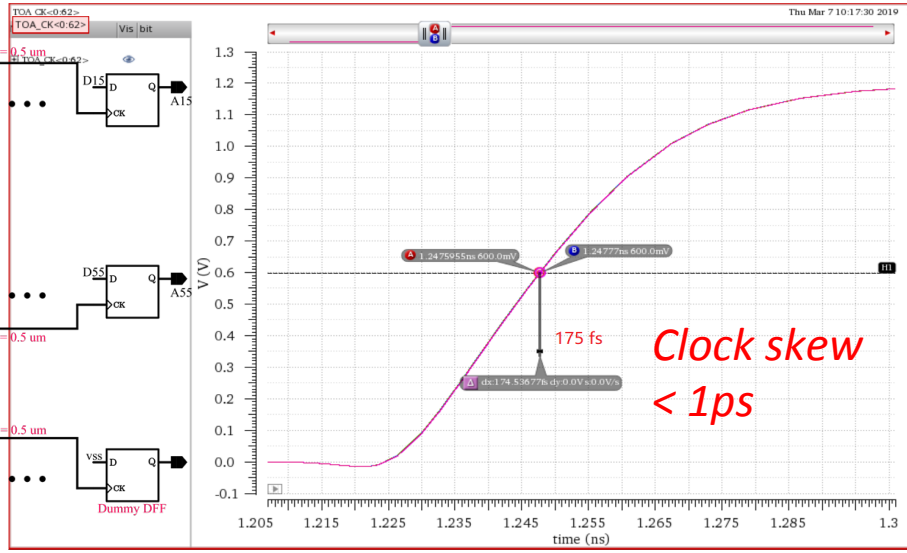




A balanced clock driver tree with 0.5um trace width (below):

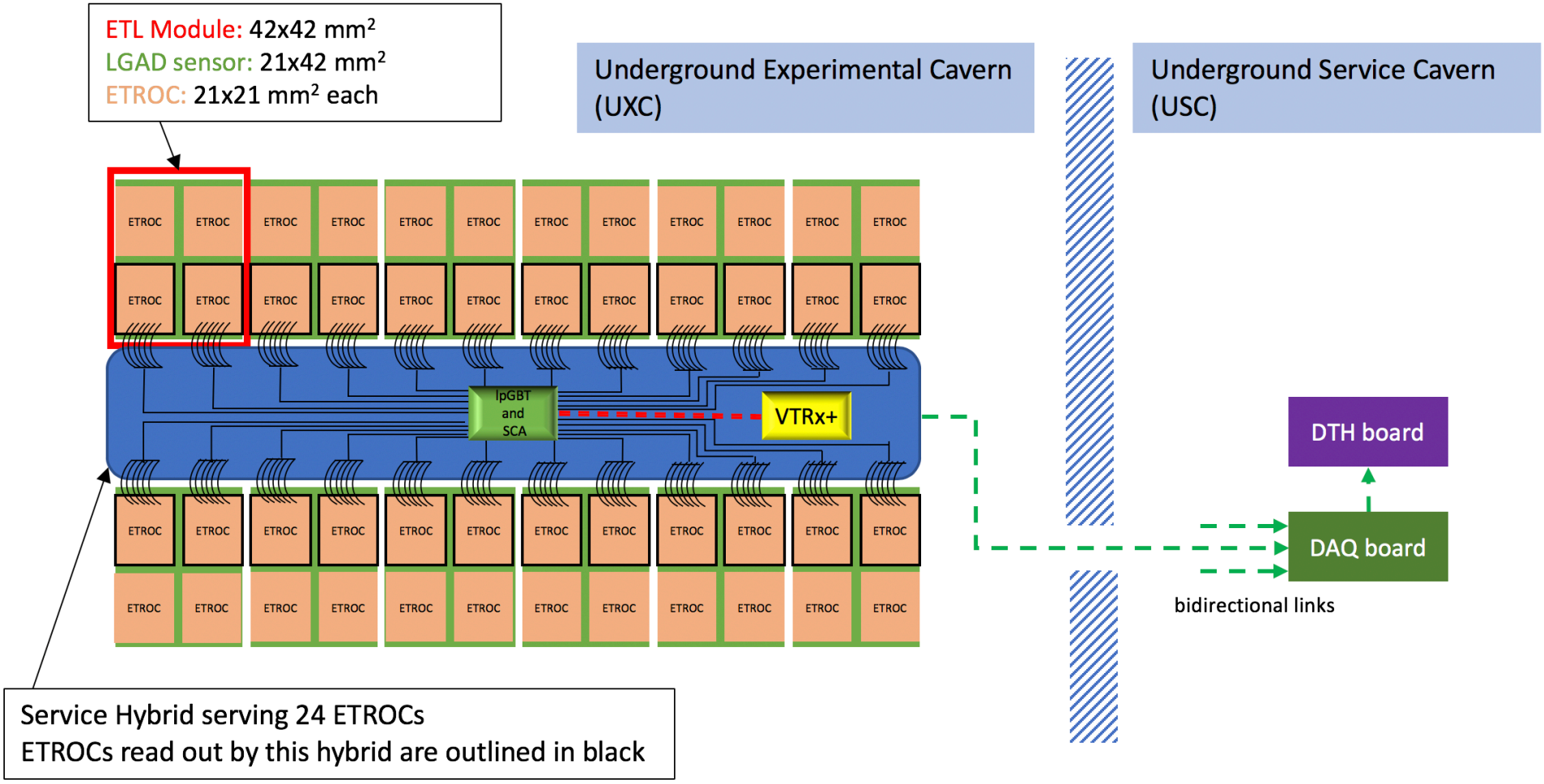
Clock skew with post layout simulation





The clock skew to the DFF array has been minimized to below 1ps.

System interface



ETL ASIC meetings/workshops

- ETL ASIC mini-workshop (June 12, 2018): ***FNAL/SMU*** collaboration started
  - https://indico.cern.ch/event/733937
- ETL ASIC meeting (July 12, 2018): design methodology and studies
  - https://indico.cern.ch/event/743235/
- ETL ASIC meeting (today, Aug 7th, 2018): chip specification
  - https://indico.cern.ch/event/747185
- Pre-TWEPP meeting (Aug 29th) with ATLAS/ALTIROC experts (with Abe Seiden visit FNAL)
- ETL ASIC meeting (Sept 6th, 2018): approach and plan review by GP
  - https://indico.cern.ch/event/754339/
- Joint-workshop with ATLAS on LGAD timing ASIC at TWEPP (Sept 18, 2018)
- ETL ASIC meeting (Nov 8th, 2018):
  - ***https://indico.cern.ch/event/771369/***

ETL ASIC project God Parent (GP) committee:
Carl Grace (LBNL, Chair), Fukun Tang/ Eric Oberla (UofC), Gary Varner (Hawaii), Christine Hu (Strasbourg/France), Ron Lipton/Dave Christian (FNAL)

ES&H

- All ES&H aspects of the HL LHC CMS Detector Upgrade Project will be handled in accordance with the Fermilab Integrated Safety Management approach, and the rules and procedures laid out in the Fermilab ES&H Manual (FESHM)
- We are following our Integrated Safety Management Plan (cms-doc-13395) and have documented our hazards in the preliminary Hazard Awareness Report (cms-doc-13394)
- All R&D and construction era work will be performed at existing facilities, and all materials are benign and commonly used in industry.
  - R&D and some production testing of ETROC will involve the use of gamma, neutron, and proton radiation.
    - These tests will be performed at commonly-used radiation facilities and will follow the standard operational procedures defined at each facility
  - No new environmental impact studies are needed beyond those that have already been performed for these sites.

Threshold and Objective KPPs

CMS-doc-13237

Updated 5 Mar 2019

- Endcap Timing Layer

WBS	Threshold KPP	Objective KPP
402.8 Timing Layer	**T-KPP-TL-2: ENDCAP TIMING LAYER CONSTRUCTION COMPLETE** The project shall provide and qualify the front-end ASIC design for the ETL. The project shall construct and qualify modules for the ETL. The project shall deliver to CERN at least 50% of the ETL modules. ASIC and module performance will match the specification of production prototypes, whose sensor components and associated front-end readout electronics have been demonstrated in cosmic ray, source, and/or test beam exposures to be capable of measuring the arrival time of minimum-ionizing particles with a resolution of < 40ps per track, for most tracks, at the start of the HL-LHC run. The specification further states that the time resolution will remain < 60ps even after withstanding the radiation damage from fluences corresponding to an integrated 4000/fb of HL-LHC luminosity, as borne out in prototype testing of irradiated components.	**O-KPP-TL-2: ENDCAP TIMING LAYER INSTALLATION AND COMMISSIONING COMPLETE** The project shall provide and qualify the front-end ASIC design for the ETL. The project shall construct and qualify modules for the ETL. The project shall deliver to CERN at least 50% of the ETL modules. ASIC and module performance will match the specification of production prototypes, whose sensor components and associated front-end readout electronics have been demonstrated in cosmic ray, source, and/or test beam exposures to be capable of measuring the arrival time of minimum-ionizing particles with a resolution of < 40ps per track, for most tracks, at the start of the HL-LHC run. The specification further states that the time resolution will remain < 60ps even after withstanding the radiation damage from fluences corresponding to an integrated 4000/fb of HL-LHC luminosity, as borne out in prototype testing of irradiated components. The project shall participate in the integration of the ETL modules into the MTD detector at CERN. The project shall additionally participate in the installation, testing and calibration of the detector.