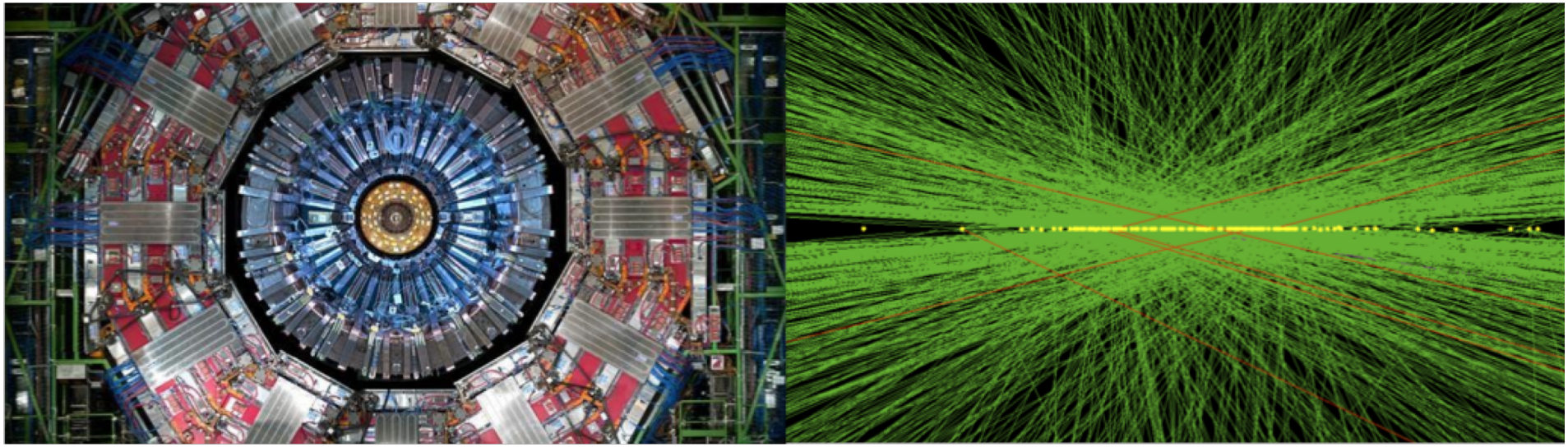
MTD-BO 3: In-depth: BTL Concentrator Card

Yurii Maravin, Kansas State University

Fermilab Director's Review
March 20, 2019



Biographical sketch

- Yurii Maravin, professor at Kansas State University
- Roles in USCMS MTD:
  - L4 US-CMS manager of the BTL Electronics Concentrator Card section: design, production and testing, as well as the delivery of the BTL Concentrator Cards
- Experience:
  - CMS since 2005
  - HCAL Calibration co-convener
  - ECAL Calibration co-convener, EGM POG co-convener
  - Physics: SMP, EXO, Higgs
  - Cosmic Ray Veto Front end board production and testing for mu2e experiment

Outline

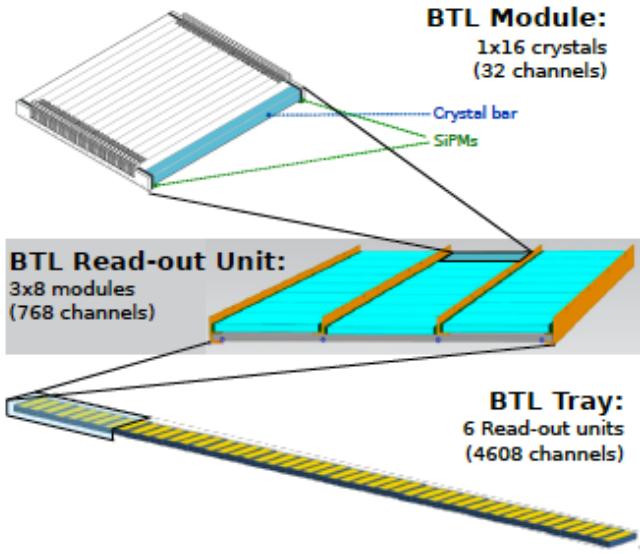
- Scope and Deliverables of 402.8.3.3
- Conceptual Design
- Cost
- Milestones
- Risks
- QA/QC
- Environmental, Safety and Health
- Responses to Previous Reviews
- Value Engineering/Resource Optimization
- Summary

Scope and Deliverables for 402.8.3.3

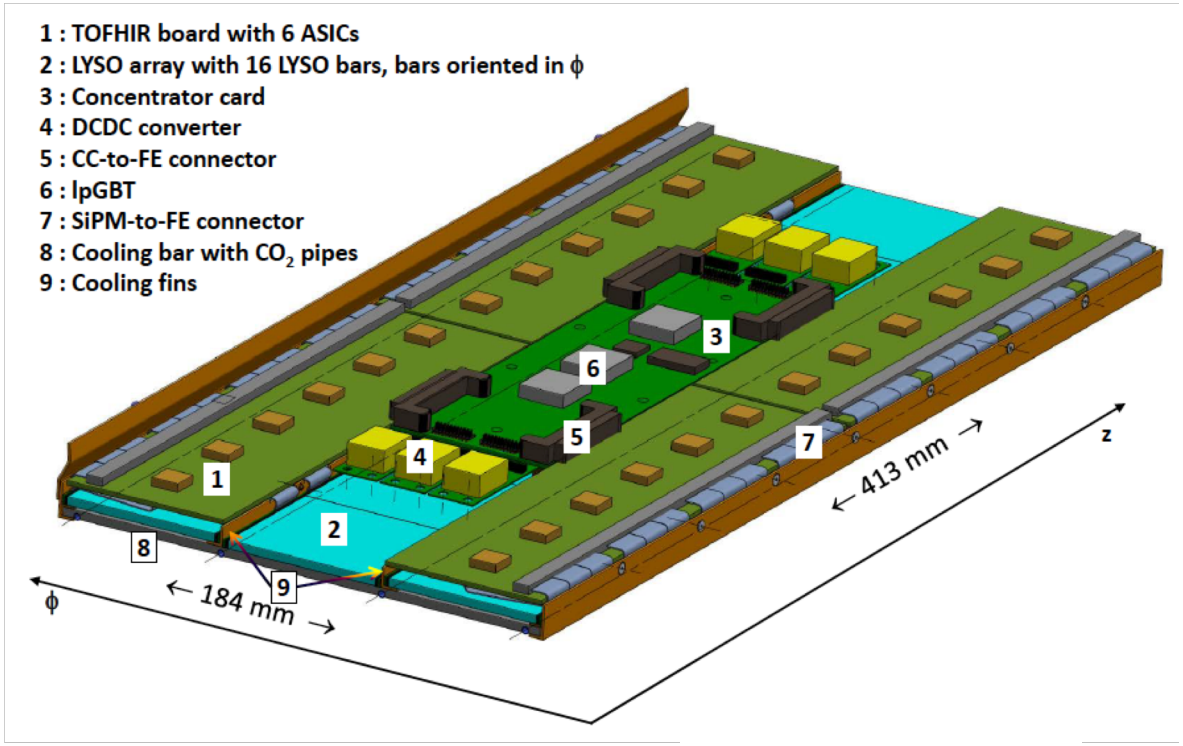
Charge #4

- Concentrator Card 402.8.3.3 :
  - Design the concentrator card
  - Procure necessary materials and assemble the boards
    - Split in three stages: prototype, pre-production, and production
  - Design both testing protocol and test bench to ensure functionality and quantify the effect of aging on the board performance (temperature, magnetic, and radiation)
- Deliver 100% of the Concentrator Card for the BTL project (436 boards + 10% spares)

BTL and Readout Unit

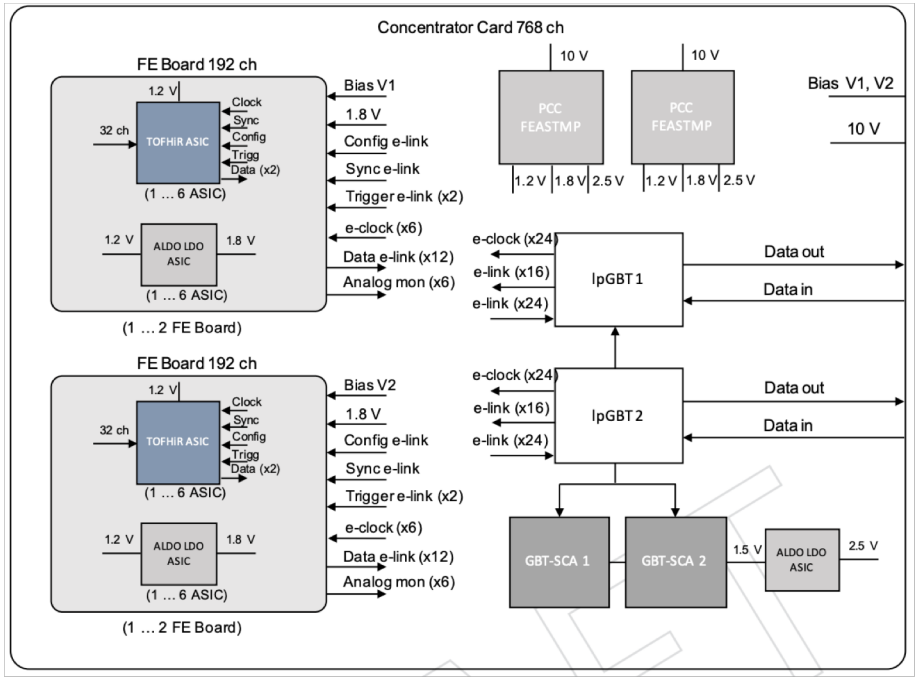


- BTL: 72 trays: 2 in z and 36 in ϕ
- Readout Unit: Front End electronics that process data from 1/6th of a tray
  - Total of 432 Readout Units are needed
- Readout Unit:
  - 4 Front End cards host TOFHIR ASICs to process SiPM signals
  - Concentrator card provides power, data i/o, control, slow monitoring



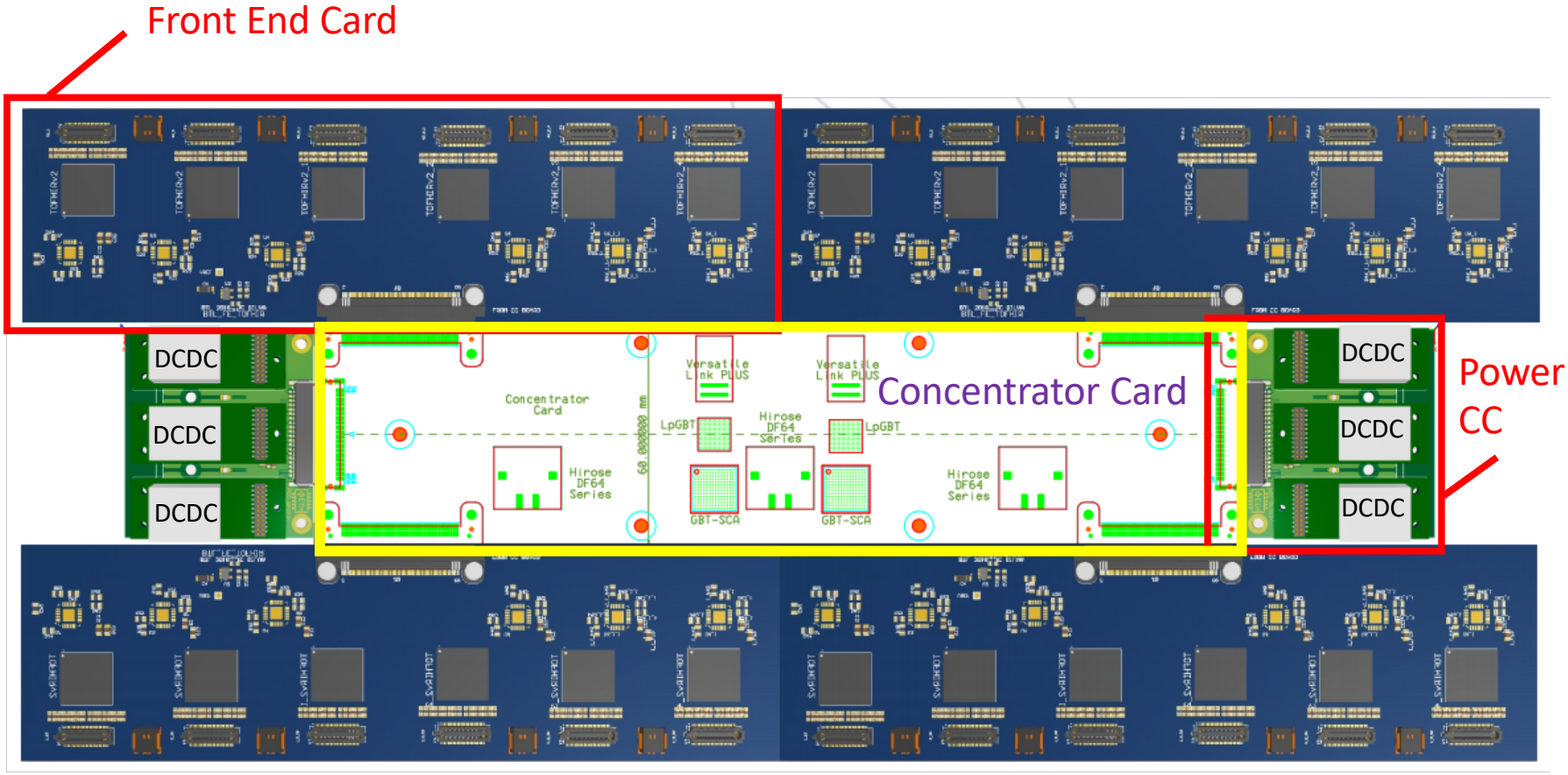
Concentrator Card functions

- Concentrator card is an integral part of the BTL electronics readout unit
  - Processes signals from 768 SiPMs via 4 Front End (FE) cards that host 6 TOFHiR2 ASIC chips
  - CC provides power to FE cards as well as power low-power Giga-Bit transceivers (lpGBT) and Versatile Link Plus (VL+) for data transfer via power concentrator cards (pCC)



  - Concentrator card provide temperature/bias monitoring via GBT-SCA ASICs
  - Overall 432 RU are needed to populate BTL

Conceptual design



- Current design: power is provided via separate cards (power CC). Considering an alternative to integrate with CC (decision in 2020)

Costs

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WBS	Labor (hours)	Labor (FTE-years)	Direct M&S $	Direct + Indirect + Escalation ($)	Estimate Uncertainty ($)	Total Cost ($)
Total	161764	91.50	6,561,457	11,364,763	3,026,706	14,391,469
402.8 TL - Timing Layer	161764	91.50	6,561,457	11,364,763	3,026,706	14,391,469
TL - Management	26520	15.00	433,000	568,714	144,562	713,276
BTL - Barrel Timing Layer	49800	28.17	3,352,236	5,410,860	1,318,476	6,729,336
California Institute of Technology	18405	10.41	315,763	658,694	227,484	886,178
Fermi National Accelerator Laboratory	0	0.00	12,849	14,271	7,135	21,406
University of Iowa	1326	0.75	0	111,794	55,897	167,692
Kansas State University	7559	4.28	497,396	954,567	318,404	1,272,971
Notre Dame	5384	3.05	1,135,400	1,740,686	296,166	2,036,852
University of Virginia	17126	9.69	1,390,828	1,930,848	413,389	2,344,237
ETL - Endcap Timing Layer	85444	48.33	2,776,221	5,385,188	1,563,669	6,948,857
Fermi National Accelerator Laboratory	16171	9.15	2,073,661	3,895,006	1,057,971	4,952,977
University of Kansas	6228	3.52	4,500	7,429	743	8,172
University of Nebraska	29066	16.44	445,540	671,092	258,358	929,450
Southern Methodist University	11425	6.46	0	334,655	106,705	441,360
University of California - Santa Barbara	22402	12.67	159,220	364,879	127,183	492,061
Generic University ("UN" is a place Holder f	152	0.09	93,300	112,127	12,709	124,837

Risks

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Risk Rank	RI-ID	Title	Probability	Schedule Impact	Cost Impact	P * Impact (k$)
Risk Rank : 3 (High) (1)						
Risk Type : Threat (1)						
3 (High)	RT-402-8-01-D	ETL - Additional FE ASIC prototype cycle is required	50 %	4 -- 5 -- 6 months	500 -- 600 -- 700 k$	300
Risk Rank : 2 (Medium) (12)						
Risk Type : Opportunity (1)						
2 (Medium)	RO-402-8-01-D	ETL - Use AltiROC	10 %	-8 months	-760 k$	-76
Risk Type : Threat (11)						
2 (Medium)	RT-402-8-03-D	ETL - FE ASIC does not meet specs - needs another pre-prod run	10 %	6 -- 7.5 -- 9 months	914 -- 970 -- 1026 k$	97
2 (Medium)	RT-402-8-05-D	BTL - Change in interfaces of tray assembly components	20 %	3 months	150 -- 250 -- 350 k$	50
2 (Medium)	RT-402-8-33-D	BTL - Difficulties procuring LYSO from international suppliers	10 %	3 -- 6 -- 9 months	200 -- 450 -- 700 k$	45
2 (Medium)	RT-402-8-91-D	TL - Shortfall in Timing Layer scientific labor	30 %	0 months	0 -- 0 -- 421 k$	42
2 (Medium)	RT-402-8-90-D	TL - Key Timing Layer personnel need to be replaced	25 %	0 -- 0 -- 3 months	45 -- 135 -- 261 k$	37
2 (Medium)	RT-402-8-14-D	BTL - Problems with SiPM vendor	20 %	2 -- 6 -- 8 months	32 -- 96 -- 128 k$	17
2 (Medium)	RT-402-8-02-D	ETL - Problems with ETL module assembly facility	50 %	1 months	30 k$	15
2 (Medium)	RT-402-8-10-D	ETL - Sensor quality problem during production	15 %	2 -- 3 -- 6 months	28 -- 52 -- 109 k$	9
2 (Medium)	RT-402-8-30-D	BTL - Concentrator Card requires significant design changes	10 %	1 -- 3 -- 6 months	1 -- 50 -- 100 k$	5
2 (Medium)	RT-402-8-43-D	TL - System Testing - components late for system test	30 %	4 months	0 -- 10 -- 20 k$	3
2 (Medium)	RT-402-8-07-D	BTL - Concentrator Card delay in external component deliveries	20 %	1 -- 3 -- 6 months	0 k$	0
Risk Rank : 1 (Low) (17)						

- RT-402-8-30-D: BTL – Concentrator card requires significant design changes
  - Can impact the completion of the CC R&D and prototyping
  - Close contact with international BTL effort to ensure timely response to potential changes in the scope
- RT-402-8-07-D: BTL – Concentrator card delay in external component deliveries
  - Medium risk: can delay any batch of CCs during production

Risks

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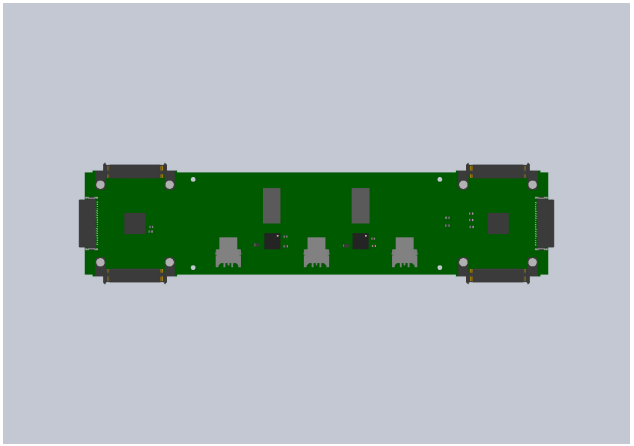
Risk Rank	RI-ID	Title	Probability	Schedule Impact	Cost Impact	P * Impact (k$)
WBS / Ops Lab Activity : 402.8 TL - Timing Layer (general risks) (3)						
WBS / Ops Lab Activity : 402.8.3 BTL - Barrel Timing Layer (15)						
Risk Type : Threat (15)						
2 (Medium)	RT-402-8-05-D	BTL - Change in interfaces of tray assembly components	20 %	3 months	150 -- 250 -- 350 k$	50
2 (Medium)	RT-402-8-33-D	BTL - Difficulties procuring LYSO from international suppliers	10 %	3 -- 6 -- 9 months	200 -- 450 -- 700 k$	45
2 (Medium)	RT-402-8-14-D	BTL - Problems with SiPM vendor	20 %	2 -- 6 -- 8 months	32 -- 96 -- 128 k$	17
2 (Medium)	RT-402-8-30-D	BTL - Concentrator Card requires significant design changes	10 %	1 -- 3 -- 6 months	1 -- 50 -- 100 k$	5
2 (Medium)	RT-402-8-07-D	BTL - Concentrator Card delay in external component deliveries	20 %	1 -- 3 -- 6 months	0 k$	0
1 (Low)	RT-402-8-15-D	BTL - Batch shipment of SiPMs lost in transport	5 %	1 months	224 k$	11
1 (Low)	RT-402-8-35-D	BTL - Delays or damage of tray in transport to CERN	5 %	1 months	220 k$	11
1 (Low)	RT-402-8-04-D	BTL - LYSO matrices not meeting specifications	10 %	1 -- 2 -- 3 months	100 k$	10
1 (Low)	RT-402-8-36-D	BTL - Interface to iCMS changes	20 %	1 -- 2 -- 3 months	30 k$	6
1 (Low)	RT-402-8-34-D	BTL - Delay in delivery of components from iCMS	20 %	1 -- 2 -- 3 months	10 -- 20 -- 30 k$	4
1 (Low)	RT-402-8-08-D	BTL - Delay in cooling plate delivery	10 %	1 -- 2 -- 3 months	10 -- 20 -- 30 k$	2
1 (Low)	RT-402-8-18-D	BTL - Concentrator card production & testing facility problem	20 %	0.5 -- 1 -- 2 months	10 k$	2
1 (Low)	RT-402-8-42-D	BTL - Problems with module assembly site	10 %	1 -- 2 -- 3 months	10 -- 20 -- 30 k$	2
1 (Low)	RT-402-8-16-D	BTL - Problems with SiPM QC test site	20 %	0.25 -- 0.5 -- 1 months	2 -- 5 -- 10 k$	1
1 (Low)	RT-402-8-44-D	BTL - Concentrator Card batch shipment lost/damaged/delayed	5 %	0 -- 0.5 -- 1 months	0 -- 3 -- 9 k$	0
WBS / Ops Lab Activity : 402.8.4 ETL - Endcap Timing Layer (12)						

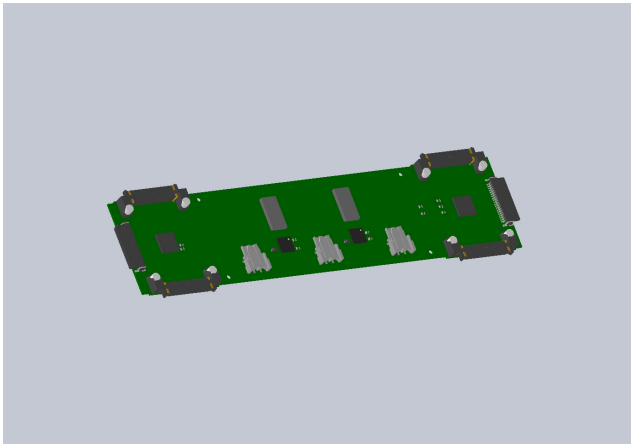
- RT-402-8-18-D: BTL – Concentrator card production and testing facility problem
  - Could delay batch of CC during production
  - Maintain components, order spare items for critical components, implement manual testing protocol
- RT-402-8-44-D: BTL – Concentrator card batch shipment lost/damaged/delayed
  - Does not delay production as delivery will outpace the assembly speed
  - Perform fast QA/QC of the first batch of the CCs to estimate the fraction of the spare CCs that would satisfy quality requirement and could be used if a shipment batch is lost

Schedule and milestones

Charge #10

- Tier 4 Milestones:
  - Produce 6 prototype boards with full functionality in March 2020 but with fewer component quantities
  - Start procuring components for CC pre-production: July 2020
  - CC is ready for production readiness review: April 2021
  - Production concentrator card complete: May 2022



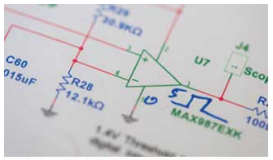


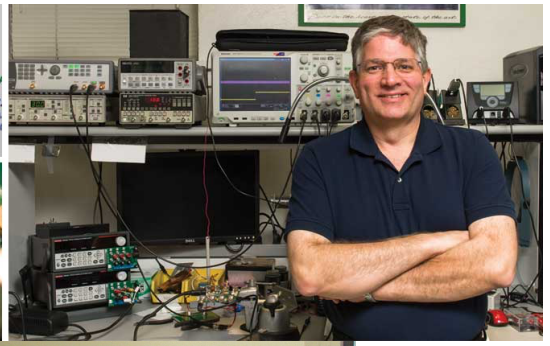
Collaborating institutions

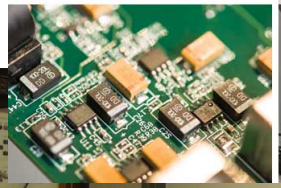
- CMS (US-CMS)
  - Kansas-State University (KSU Electronic design laboratory)
    - Russell Taylor: two decade long experience in designing, producing, testing HEP hardware (D0 silicon detector, CMS Pixel phase 1 and 2 upgrade, CMS HCAL phase 1 upgrade, mu2e CRV FEB production and testing)
    - David Huddlestone: experience with vendors, procuring components
  - Interface very close to non-US collaborations (ETH, CERN, Milano)

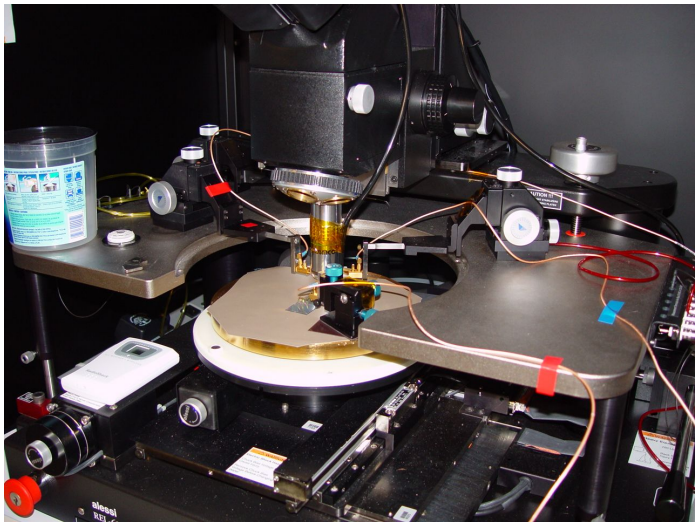
QA and QC Testing

- The QC facility in the US at Kansas State University
  - Testing facility: 50 m^2 class 10000 (ISO 7) clean room
  - Batch testing of the CCs by undergraduates
- QA/QC Validation
  - Functionality
  - Thermal, radiation, magnetic









Summary

- The project depends on a few external components that are essential for the whole LHC Phase 2 upgrade
- The first power-only prototype has already been built and used in TOFHiR tests in LIP
- Prototyping will ensure ensure good mechanical integrity and longevity of the components
- Expect no delays with the milestones given relative simplicity of the CC design

Backup

Environmental, Safety and Health

Charge #9

- All ES&H aspects of the HL LHC CMS Detector Upgrade Project will be handled in accordance with the Fermilab Integrated Safety Management approach, and the rules and procedures laid out in the Fermilab ES&H Manual
- We are following our Integrated Safety Management Plan (cms-doc-13395) and have documented our hazards in the preliminary Hazard Awareness Report (cms-doc-13394)
- In General Safety is achieved through standard Lab/Institute practices
  - No construction, accelerator operation, or exotic fabrication
  - No imminent peril situations or unusual hazards
  - Items comply with local safety standards in site of fabrication and operation
  - Site Safety officers at Institutes identified in the SOW
- There are no Specific Hazards for 402.8.3.3
  - No high voltage/radiation risks are present in QC/QA program at K-State laboratory
  - No heavy objects are associated with the CC production and QC/QA
  - Risks associated with this project are typical to those found in labs pursuing electronic design

Opportunities for Value Engineering

Charge #5

- Experienced engineer with several decades of work for HEP experiments
  - D0 SMT, CMS Pixel phase 1 and 2 upgrade work, CMS HCAL phase 1 upgrade work, mu2e CRV FEB production and testing, Double Chooz, protoDUNE, DUNE 35t
- Vendor experience

Responses to Previous Reviews p1

- BTL-R3: Consider setting granularity of number of chips/card so that one DC-DC converter is matched to a single TOFHIR readout card
  - The current design takes this suggestion into account by assigning a single DC-DC converter per single TOFHIR readout card. Thus, four DC-DC converters serve four TOFHIR card, and the remaining two are used to power the Concentrator Card
- BTL-R4: Develop a plan for powering up the ASICs card connected to the concentrator card and for exploiting the lpGBT capabilities for control and environmental monitoring

Responses to Previous Reviews p2

- BTL-R4: Develop a plan for powering up the ASICs card connected to the concentrator card and for exploiting the lpGBT capabilities for control and environmental monitoring
  - The capabilities for powering up/down, control, and environmental monitoring are given below. They allow full control to implement powering up/powering down scheme that will be designed together with the detector control specialists and MTD teams. Each FE board DC-DC converter enable will be controlled from a GBT-SCA GPIO pin. The PGood signal from each DC-DC converter will be monitored by a GBT-SCA GPIO pin. Each DC-DC converter output voltage will be monitored by a GBT-SCA analog input. The board input voltage will be monitored by a GBT-SCA analog input. The temperature of the PCC and FE boards will be monitored by a GBT-SCA analog input. Four SiPM temperature sensors will be monitored by the LpGBT analog inputs. Total bias current for every 16 SiPM's will be monitored by GBT-SCA analog inputs (12 from each FE board). Internal temperature sensors in each GBT-SCA (2) and each LpGBT (2) will monitor temperature of the CC.