ECAL Readout Electronics Using the VMM3 ASIC

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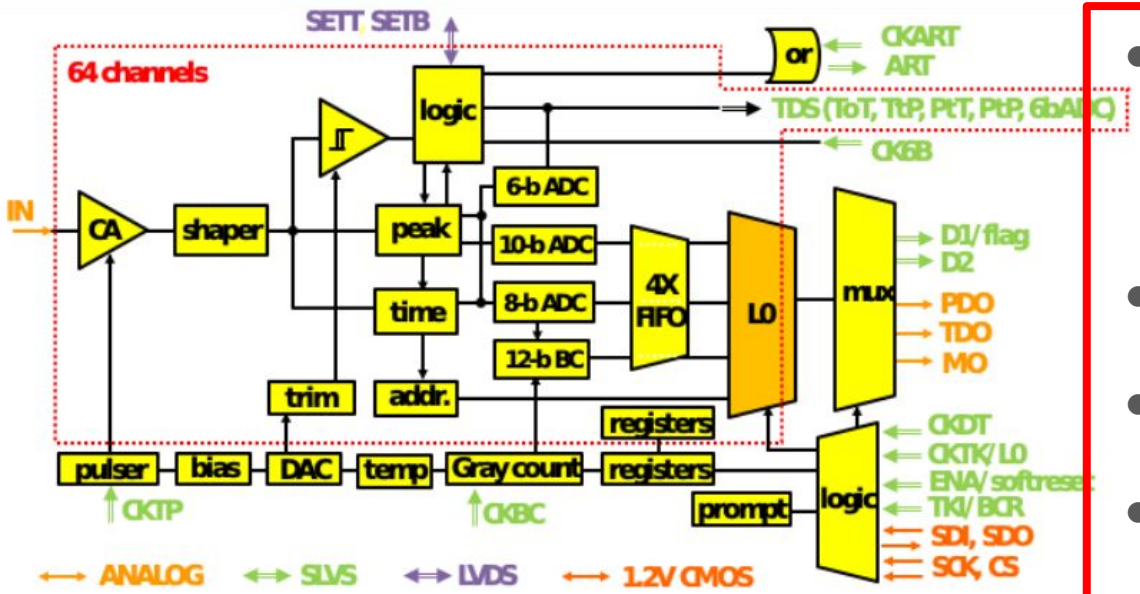
VMM3 ASIC in STT Readout Overview

- The VMM3 ASIC is mature, widely used in HEP readout electronics
  - What is the VMM3 ASIC?
  - The VMM3 ASIC is well suited to the near detector STT readout
- VMM3 experience
  - ATLAS
  - Test Beams
  - Mu2e CRV CSC
- VMM3 readout R&D plan for the STT

VMM Architecture & highlights

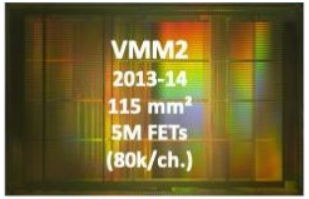


- peaktime (200, 100, 50, 25 ns)
- gain (0.5, 1, 3, 4.5, 6, 9, 12, 16 mV/fC)
- neighbor logic
- timing outputs
- both input charge polarity
- ~1700 bits of configuration with SPI
- digitisation time ~220ns - if only 6-bit then 40ns
- large sensor capacitance mode control
- monitor multiplexing
- TAC slope adjustment (60, 100, 350, 650 ns)
- buffering latency FIFO up to 64 events, 16 deep fifo in readout (8b/10b encoding)

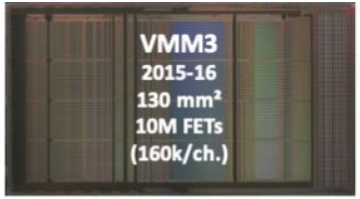
- VMM3 is a “Swiss-Army” ASIC for a wide-variety of applications
- 64 input ch / ASIC
- Outputs: digital Q+T
- Low power: < 10mW / ch
- **Compact readout replaces a crate of electronics**

VMM Development

- mixed-signal
- 2-phase readout
- peak and timing
- neighbouring
- sub-hysteresis
- few timing outputs



- mixed signal
- continuous fully-digital readout
- current-output peak detector
- increased range of gains
- three ADCs per channel
- FIFOs, serialized data with DDR
- serialized ART with DDR
- additional timing modes
- 64 timing outputs
- ITAR
- additional functions and fixes



- mixed signal + digital
- continuous simultaneous readout
- SEU-tolerant logic
- Deeply revised front-end for TGC (2nF, 50pC, fast recovery, ...)
- L0 handling digital core
- SLVS and new config. interface
- new reset control and fast reset
- timing at threshold
- timing ramp optimisation
- pulser range extension
- ART synchronisation
- 32-channel skip
- additional functions and fixes

- Adjustable feedback currents
- Additional bug fixes
- Yield issues addressed

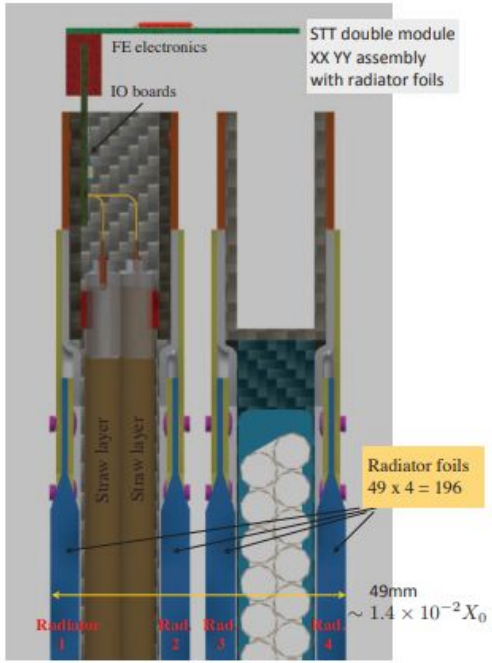
VMM3, the first prototype!
VMM3a - Production prototype, bug fixing

G. Iakovidis, BNL

Focus on the Near Detector ECAL STT

- *Precision EW & QCD measurements require control of ν-target(s) as in $e^{\pm}$ DIS:*
  - *Massive ν detectors intrinsically limited by the knowledge of the target composition & materials;*
  - *Possible accurate control of target(s) by separating target(s) from active detector(s);*
  - *Thin targets spread out uniformly within tracker by keeping low density* $\rho \sim 0.16\ g/cm^3$.

$\Longrightarrow$ *Straw Tube Tracker (STT) in $B \sim 0.6T$ with 4π electromagnetic calorimeter*

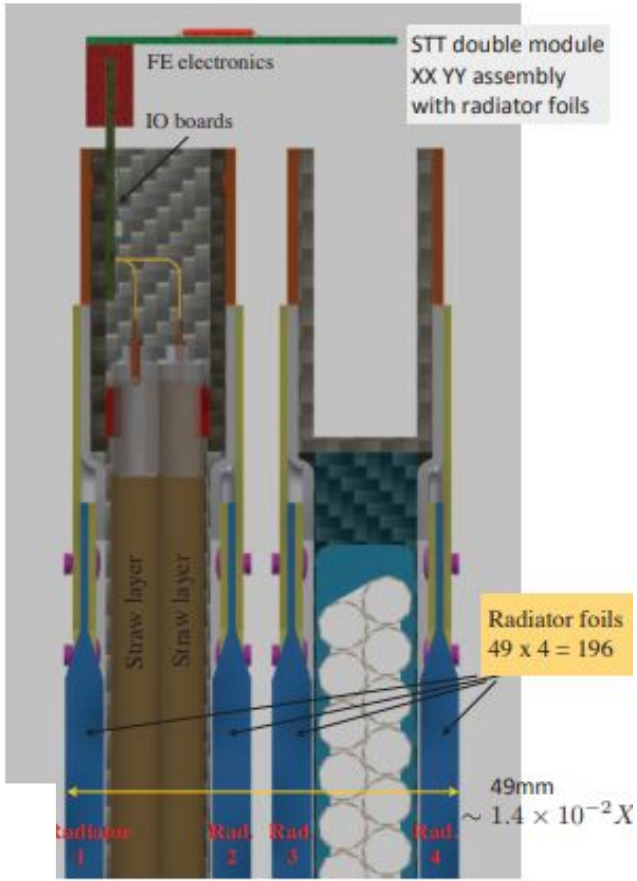


- *Radiator targets (100% purity) account for $> 95\%$ of STT mass and can be tuned to achieve desired statistics & resolutions.*
- *Separation from excellent vertex, angular & timing resolutions.*
- *Radiators can be replaced by thin nuclear targets: C, Ca, Ar, Fe, etc.*

Can the VMM3 read out this detector?

R. Petti, USC

Near Detector ECAL STT Readout Requirements



- Operating parameters:
  - Gas Xe/CO2 & Ar/CO2 (70/30), gain ~2x10^4;
  - Straw diameter 5mm, max drift time ~60 ns;
  - Max straw length 4m, wire 20 um diameter Au plated W;
  - STT length 4m, tracking volume ~45m^3;
  - Common trigger: t=drift time+time of flight+propagation along wire.

- Readout requirements:
  - Measure deposited charge & time t;
  - Timing resolution << 1ns;
  - Low threshold: charge from single ion pair;
  - Dynamic range > 1000 on charge;
  - Max width of readout board: 5cm;
  - Max length of readout board: 16 cm every 64 channels for double readout

VMM3 ASIC is a good readout solution for this detector!

- Double readout at both ends of straws:
  - Measure longitudinal hit position along wire from direct time measureme
  - Time difference between signals at 2 ends: time resolution < 250 ps.

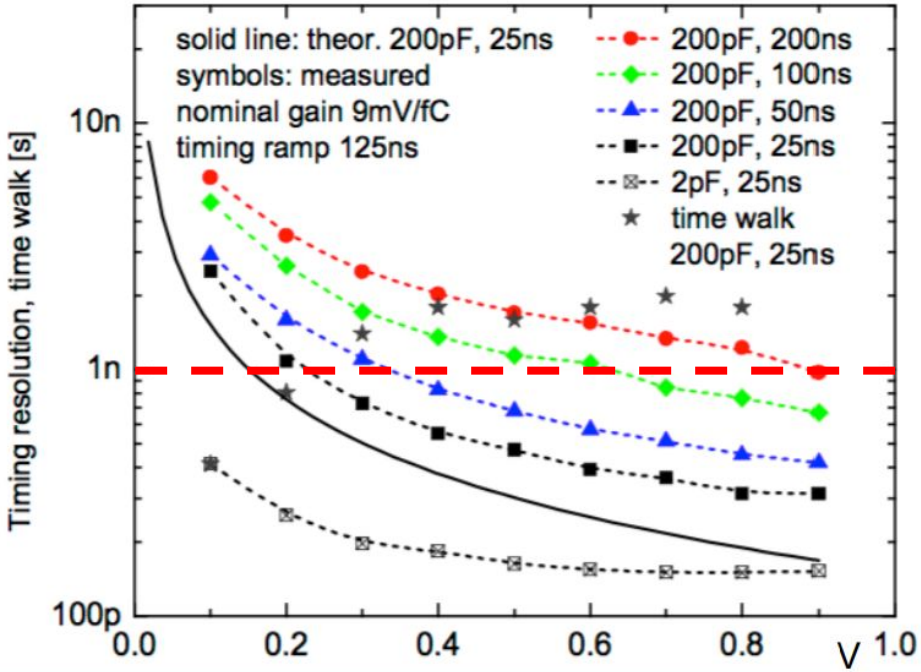
R. Petti, USC

VMM3 Meets ND STT Readout Requirements

- Readout requirements:
  - Measure deposited charge & time t;
  - Timing resolution << 1ns;
  - Low threshold: charge from single ion pair;
  - Dynamic range > 1000 on charge;
  - Max width of readout board: 5cm;
  - Max length of readout board: 16 cm every 64 channels for double readout

- VMM3 satisfies required <1ns timing
- Measures Q + T for each input
- Compact 64-ch ASIC well suited to ND spatial constraints inside magnet
  - Can satisfy STT readout width and length constraints

VMM3 Time Resolution



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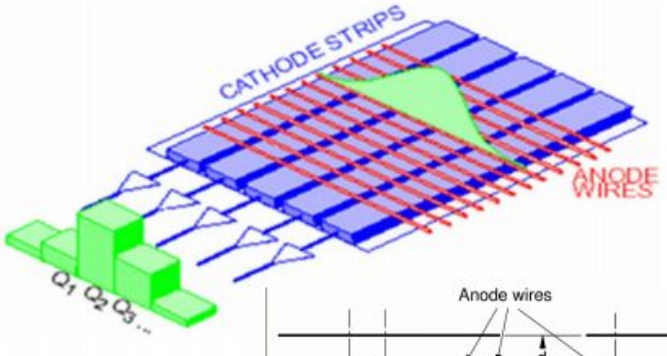
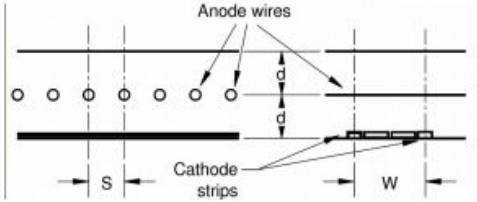
VMM ASIC and the ATLAS CSC



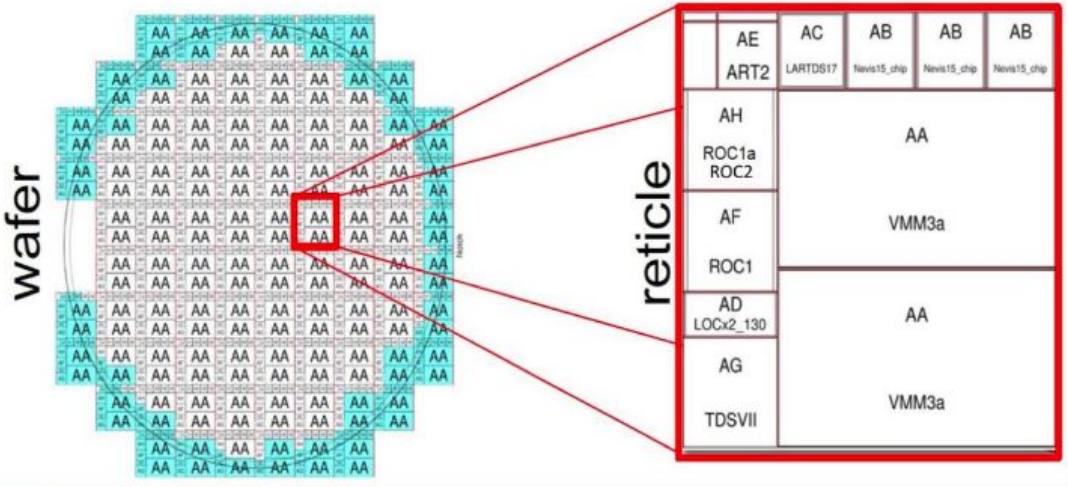


- four-layer chamber
- anode wire pitch: 2.54 mm
- cathode readout pitch: 5.08 mm
- position measurement based on charge interpolation
- rms resolution: up to 60 um
- time resolution: 7ns
- gas mixture: Ar-CO_2
- gas gain: 10^4
- number of chambers: 32
- number of readout channels: 67,000
- area covered: 27 m^2

Used VMM ASIC

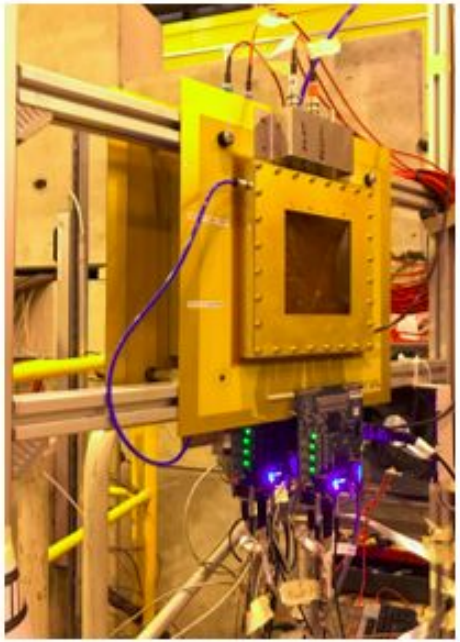
VMM3a ASIC and the ATLAS NSW Upgrade

- VMM3a passed successfully the ATLAS Production readiness review on the 29th of October 2018 fulfilling the requirements of the New Small Wheel upgrade
- Reminder: New Small Wheel is composed of 2.4M readout channels used for trigger as well
  - Two detector technologies, Micromegas and sTGC, largest Phase I upgrade
- Production submitted beginning of 2019
  - 625 wafers which contains 113 chips per wafer - Total production of 70625 VMMs !
  - Current yield of 72% on which the designing team is working with Global Foundries to optimise
- Production with leading 50 wafers starts delivery on May 2019

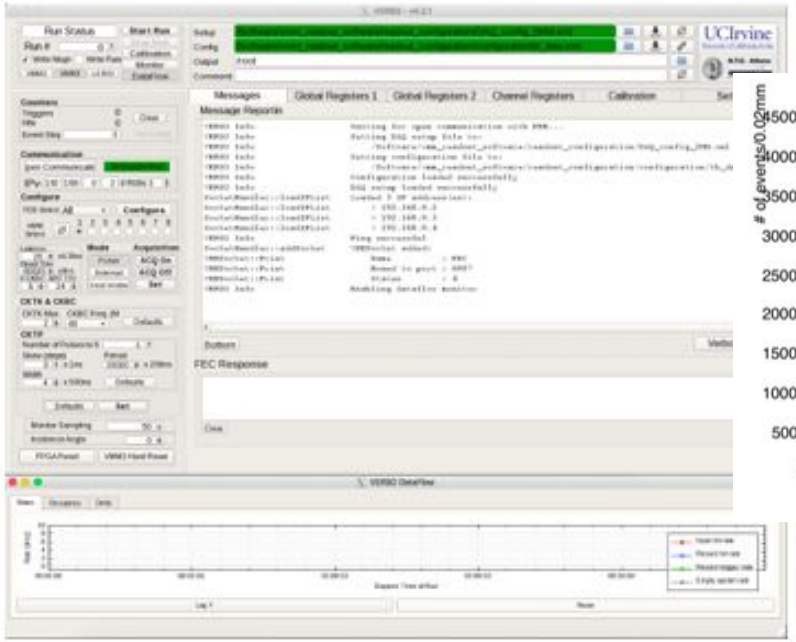


VMM3 ASIC and Micromegas Test Beam

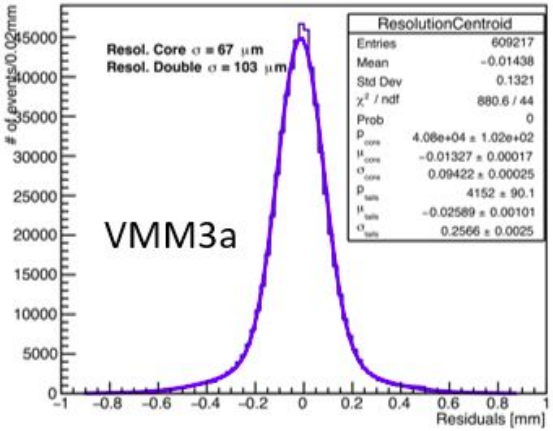
- VERSO (UCI/BNL) was used to readout the data and to control the frontends.
- Firmware was developed by BNL/NTUA, version to control the CKBC which allowed precise timing measurements along with ART measurements.
- Common trigger to all the system provided by scintillators. This is a control signal for the VMM TAC.
- On the VMM3a setup, data were taken on L0 mode as well, analysis is ongoing
- The trigger signal was readout by VMM3/3a on channel #63



DAQ Software Interface GUI



Perpendicular Track Residuals



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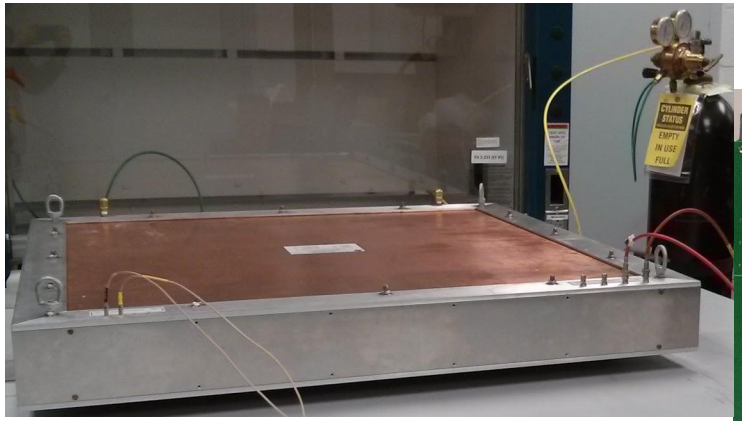
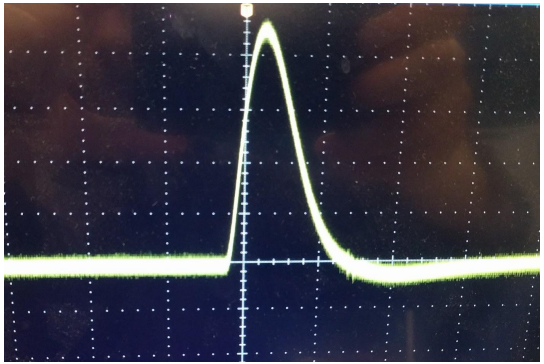
VMM3 Readout for the Mu2e CRV CSC Test Stand

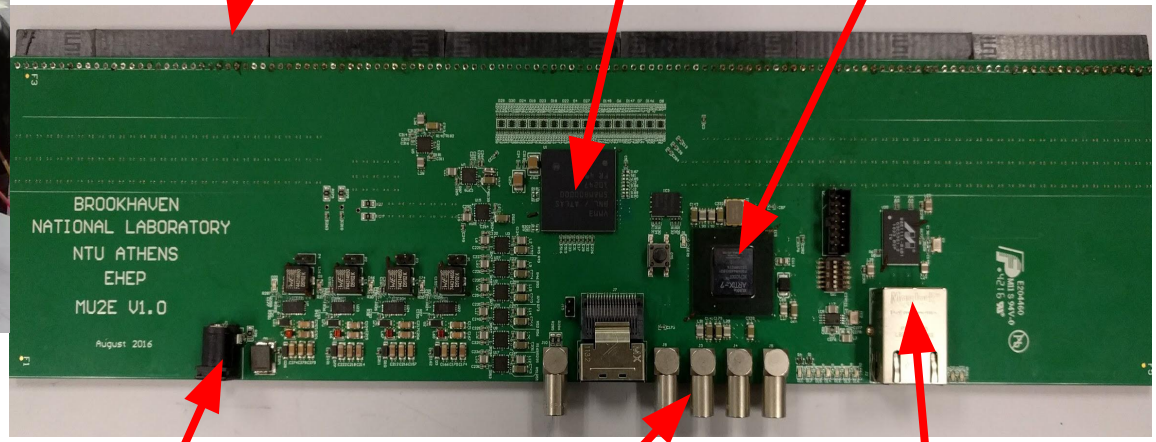
CSC at BNL



Example Calibration Pulse



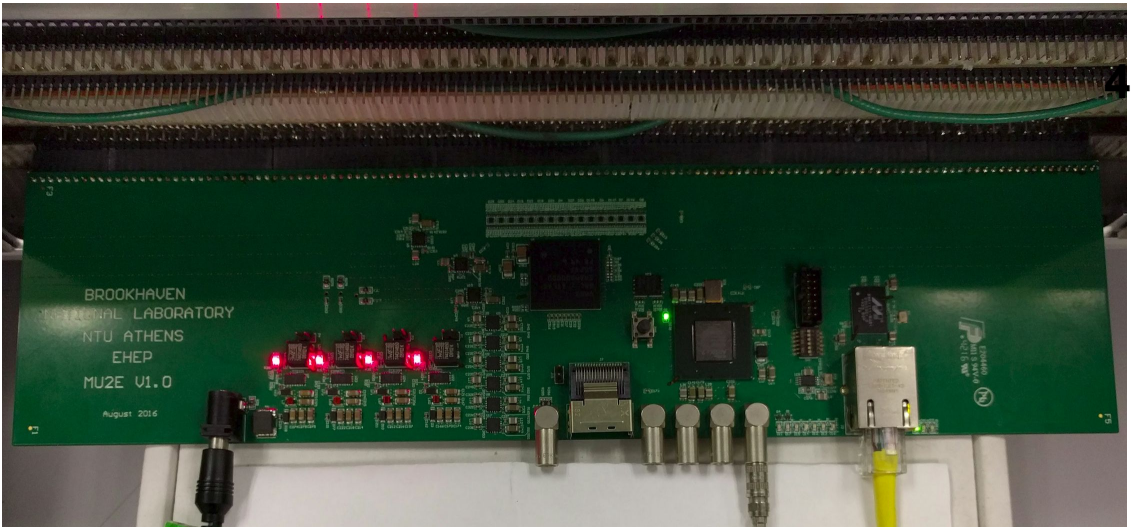
Prototype CSC VMM3 Readout Board



- Compact VMM3 based readout board developed for Mu2e Cathode Strip Chamber (CSC) test stand
- FPGA-based readout allows flexible DAQ integration

VMM3 Readout Board on Mu2e Test Stand CSC

VMM3 Board on CSC Top View



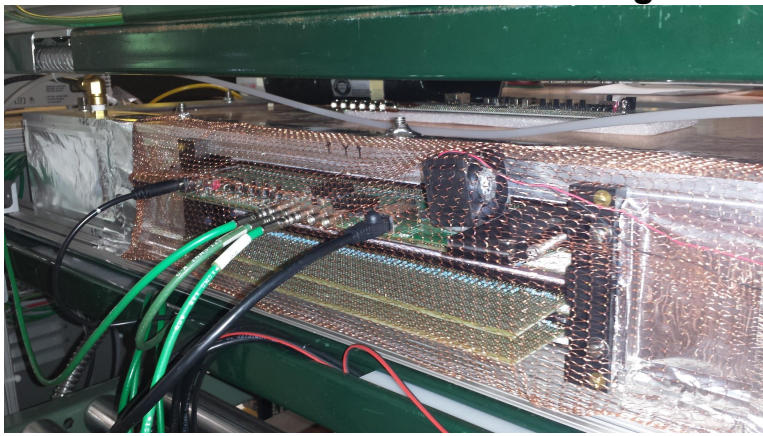
4 VMM3 Boards Mounted on CSC

- Each VMM3 board reads out one Mu2e CSC layer
  - Chamber has 8 layers total, 4 each for X+Y
  - 75-20 Ar-$C0_2$ gas mixture, ~3kV bias
- Row of 64 female sockets give good contact to cathode pins, reduces noise
- **Good starting point for STT readout, similar ~5cm spacing**

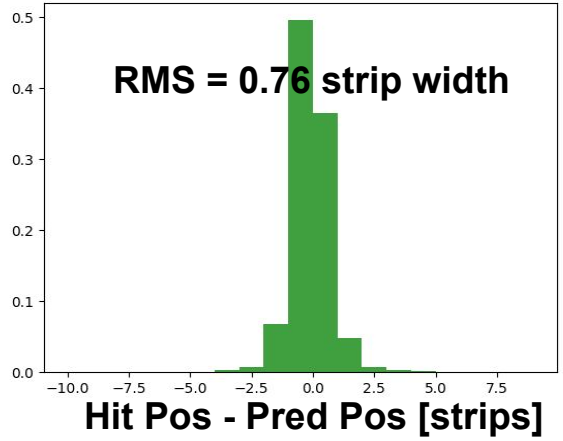
CSC Test Stand at UVa for Mu2e CRV Module Validation

UVa Mu2e CRV Test Setup, Three CSCs

Mounted Board with Shielding



CSC Hit Cluster Position - Prediction



- 32 VMM3 readout boards produced for Mu2e CRV scintillator module test stand
- Good test stand for VMM3-based readout
- Preliminary position resolution meets expectation

STT Readout Research and Development Plan

- Propose using VMM3a-based readout for STT
- Year 1:
  - Evaluate VMM3-based readout with straw tube tracker detector
    - Construct dedicated electronics test stand with straw tubes
  - Identify potential revisions to ASIC to improve performance
  - Initial design of prototype electronics based on Mu2e CSC boards
- Year 2:
  - Evaluate prototype electronics performance, identify any further ASIC or board revisions
  - Preliminary design of detector + readout integration in near detector
  - Technical design of detector electronics
- Year 3:
  - Demonstrate performance of VMM3 electronics and STT in low energy test beam (CERN)
  - Full technical design of STT detector + readout

Summary

- VMM3 is a compact, flexible ASIC well matched to frontend electronics requirements of near detector STT
  - Demonstrated time resolution better than 1ns and ability to measure energy deposit
  - Applied successfully in multiple detectors (ATLAS, Mu2e CRV test stand shown here)
  - Readout, DAQ and associated software already developed
  - **Costs understood from previous productions**
- Current CSC test stands at BNL+ UVa is excellent evaluation platform for VMM3 ASIC readout and potential improvements
  - Will evaluate performance of VMM3a with CSCs in near future
- Can adapt VMM3 readout to STT quickly
  - Proposed R&D plan including test beam to demonstrate readout meets requirements
- **VMM3a is flexible and can be used in other near detector readouts**