U.S. Contributions to the Upgrade of the CMS Experiment

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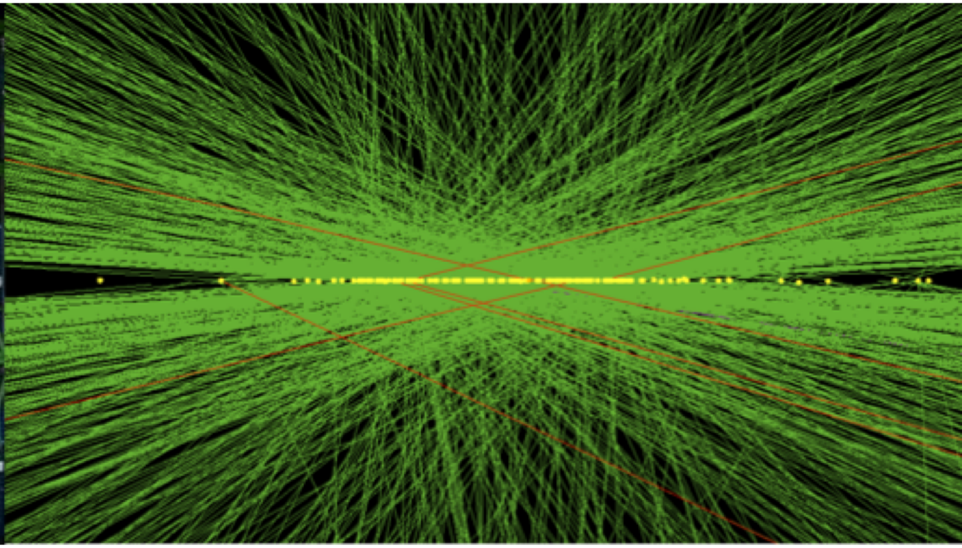
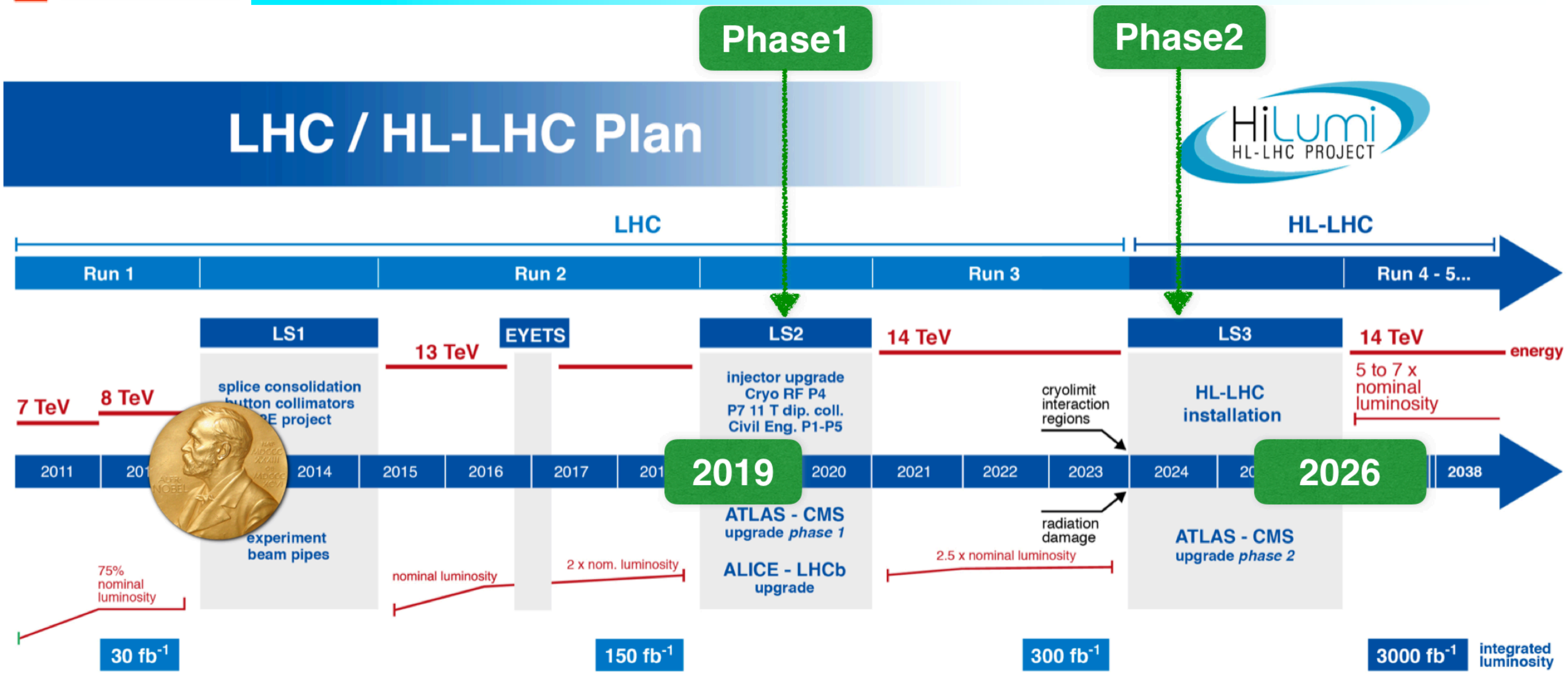
Fermilab

Fermilab Users Meeting, June 12th 2019

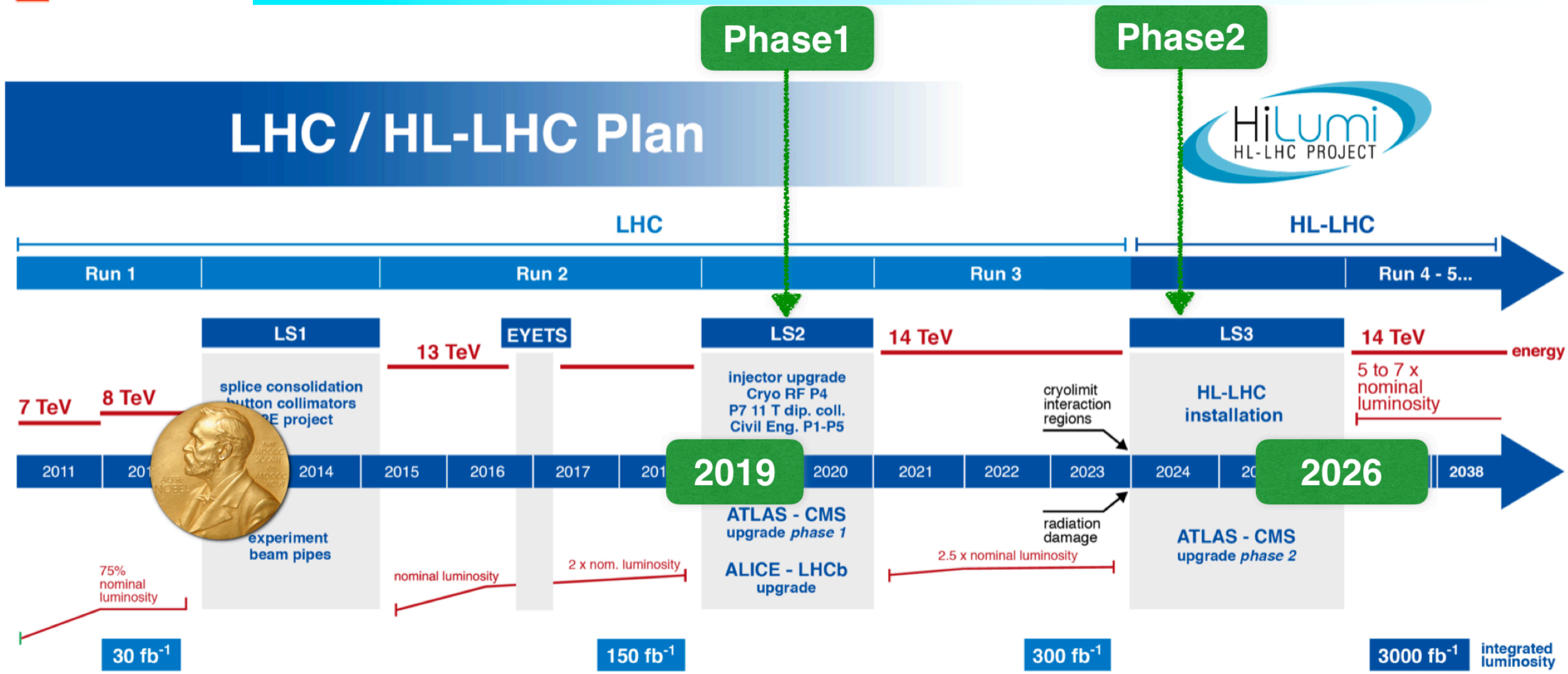


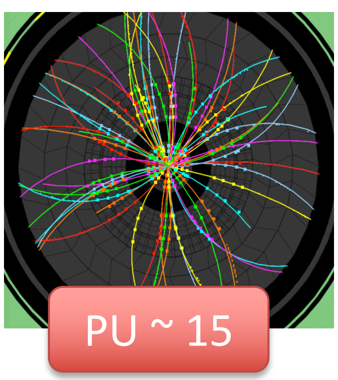
Upgrades to the CMS Experiment

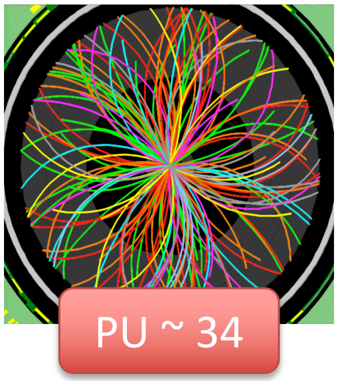


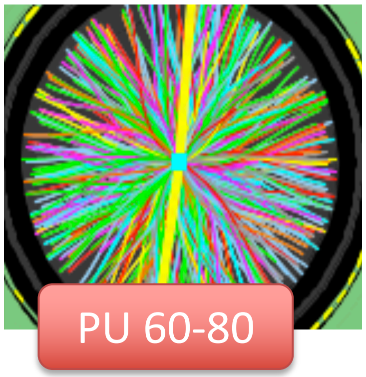
- Excellent performance of the LHC in Run2, exceeding planned luminosity with 160/fb delivered
- Just 5% of the entire LHC & HL-LHC dataset!
- Addressing three of the five P5 science drivers:
  - Higgs bosons as tool for discovery
    - O(1%) precision on SM couplings with HL-LHC, by collecting 10 time more Higgs bosons than at the LHC
  - Searches for DM and searches for the unknown

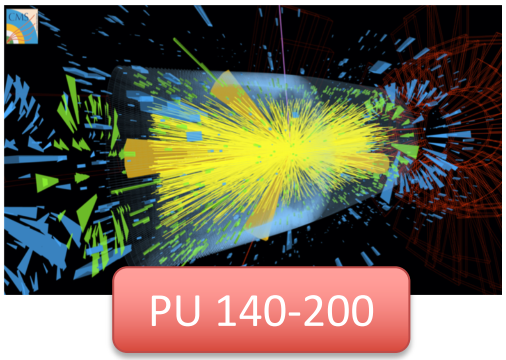
The Challenge





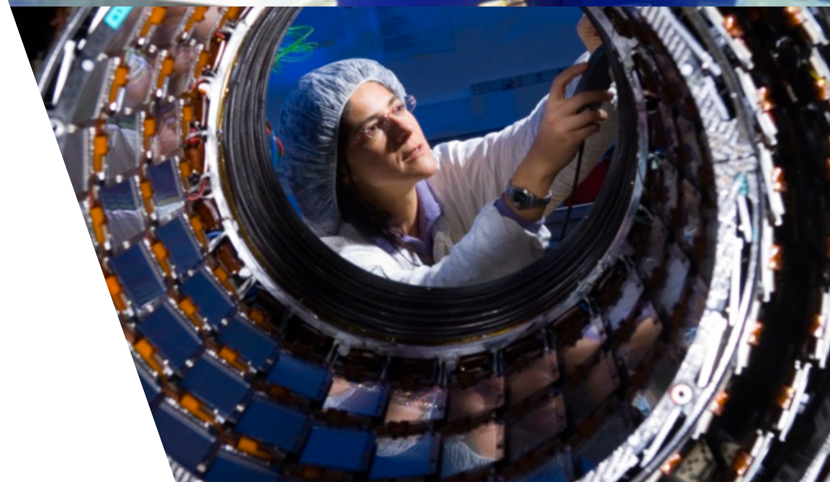


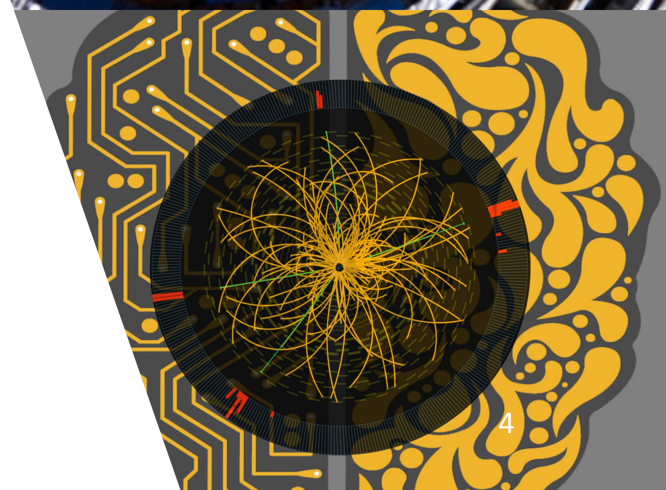




The Opportunity

- **Silicon technology**
- **SiPM on scintillator**
- **65nm ASICs**
- **Fast optical links**
- **Advanced triggers**
- **Software and computing**
- More!



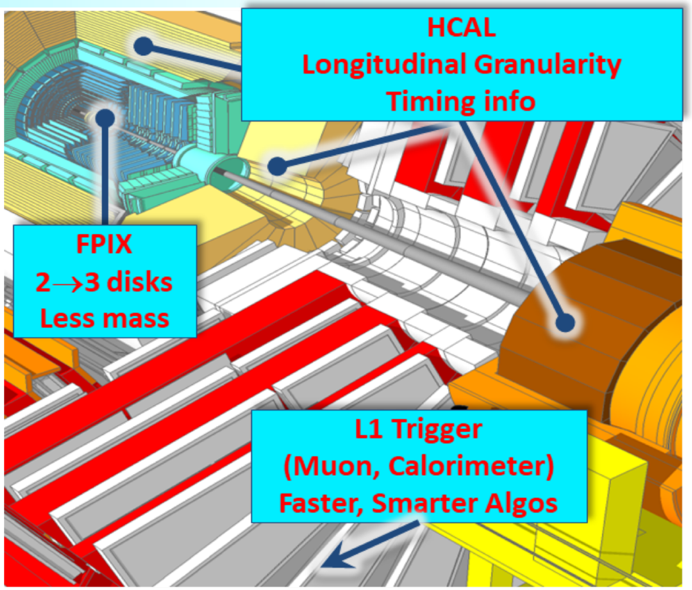


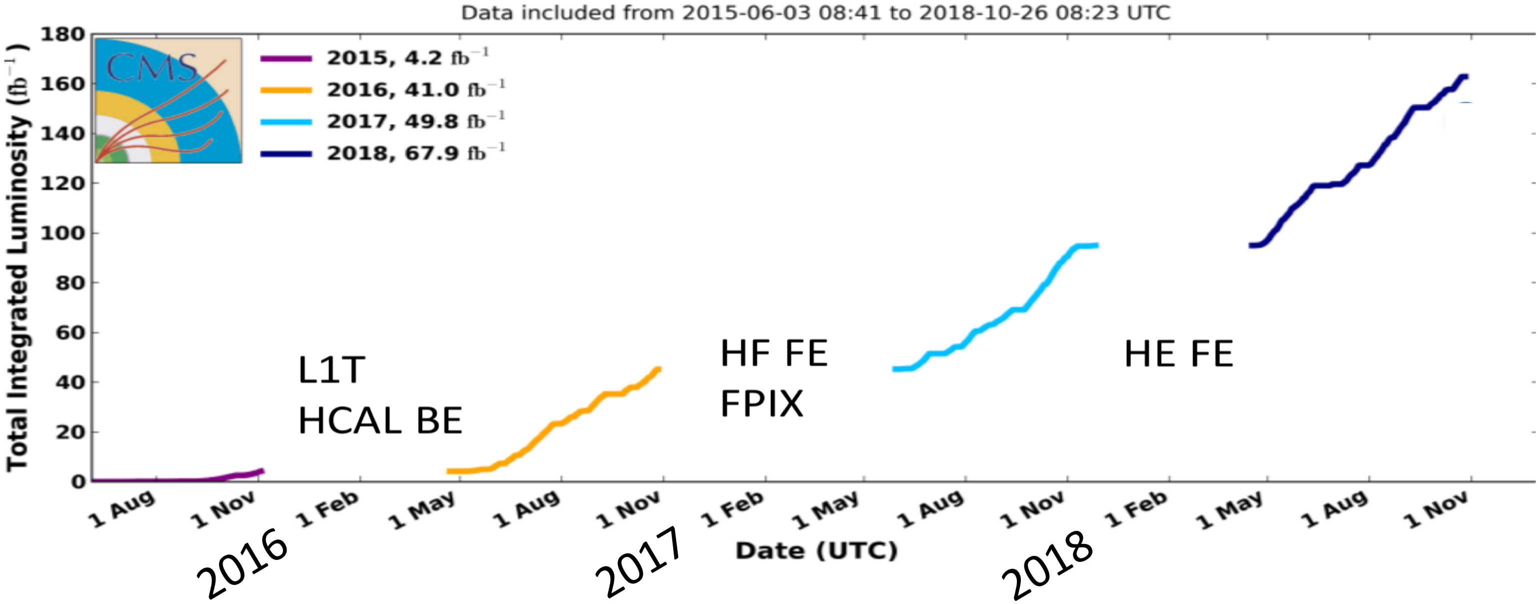
Building on Fermilab Strengths

- **Fermilab, host lab for U.S. CMS**
  - Central role in the upgrade
- **Providing high profile and specialized facilities and critical expertise**
  - Silicon Detector Facility and Scintillator/SiPMs expertise
  - Large integration facilities with alignment survey
  - Facility for fabrication of Carbon Fiber supports
  - ASIC engineering
  - Trigger/DAQ expertise
  - Software and computing
  - Fermilab Test Beam Facility
    - ITA (irradiation test area) under consideration

Phase 1 Upgrade: Overview

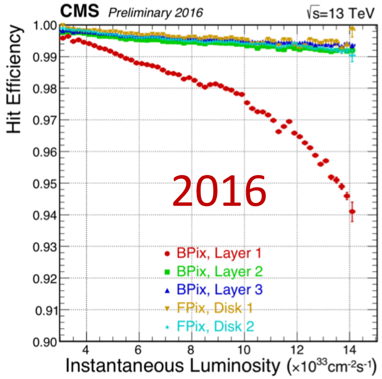
- "Complete the LHC Phase 1 Upgrades …", 1st project specific recommendation of P5
- Mission statement of U.S. CMS scientists at FNAL and 30 U.S. CMS institutions in the past six years
- CD-4 in May 1, 2019; ESAAB June 10, 2019!
- FermiNews https://news.fnal.gov/2019/05/cms-upgrades-take-a-big-step/

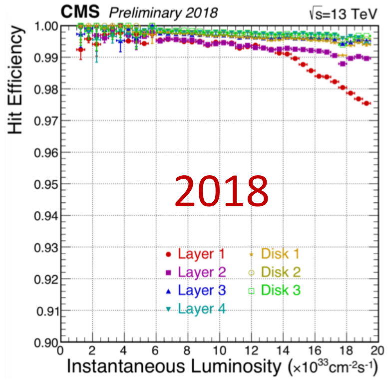


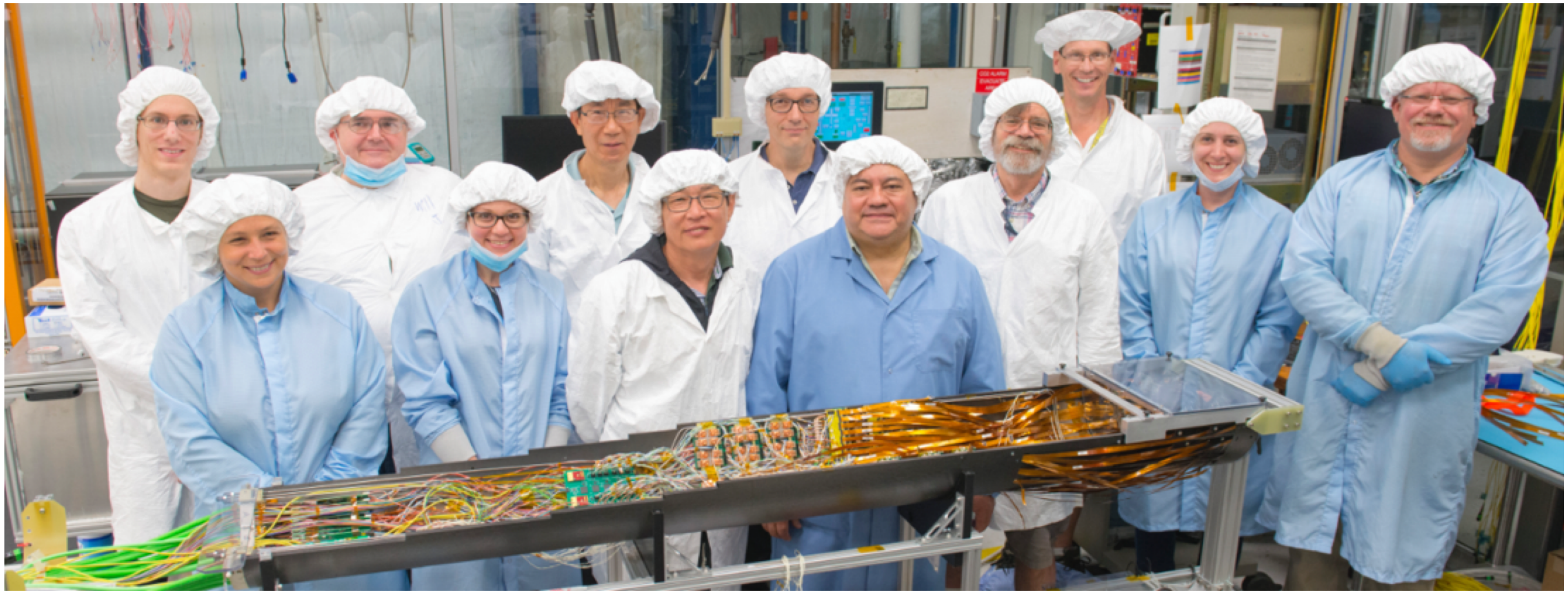


Forward Pixel Detector

- New vertex detector with one additional layer closer to the beam
  - More precise tracking
  - improved vertex separation
- 672 modules for a total of 45 million pixels read out at 100 kHz
- Fully digital ASIC with deeper buffer, reduced material
- Integration of modules into large structures at Sidet, FNAL

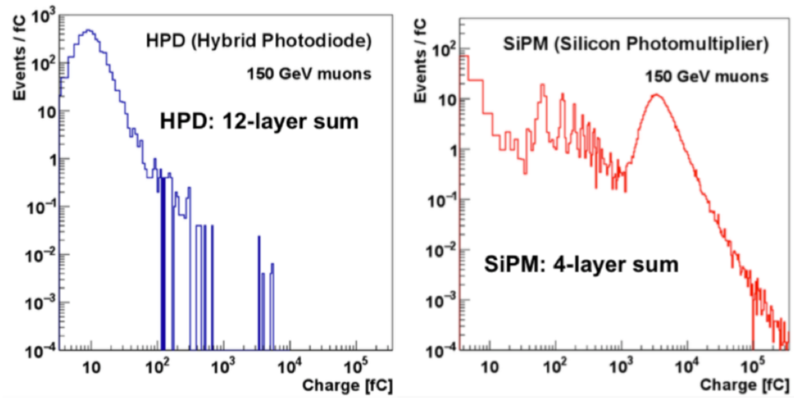


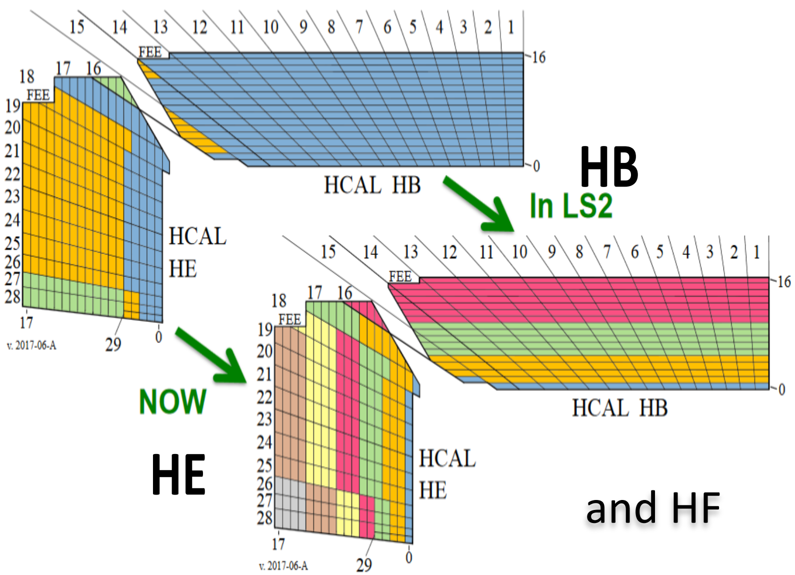




HCAL Upgrade

- Upgrade (HF) or replacement (HE/HB) of the photodetectors with SiPMs
  - Increasing granularity of the energy measurement and providing timing measurement
  - Leading to increased throughput to L1 trigger and data acquisition system
- FNAL designed charge integrating ADC, with integrated TDC (QIE10 and QIE11)
- Hadronic Endcap and Hadronic Forward Calorimeters
  - Installed, commissioned, operated in 2017 and 2018
- Hadron Barrel Calorimeter Installation & commissioning now
  - Requiring extended access to the inner guts of the detector!
  - Full upgrade ready for the first data of Run 3, expected mid 2021

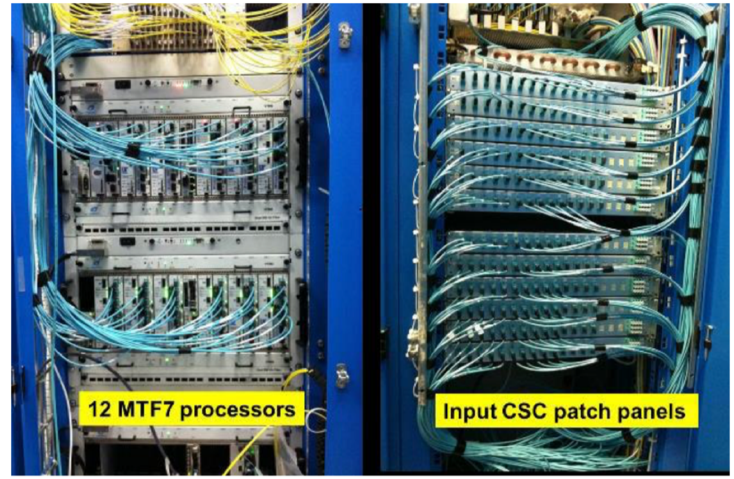




Jim Hirschauer received DOE ECA

L1 Trigger Upgrade

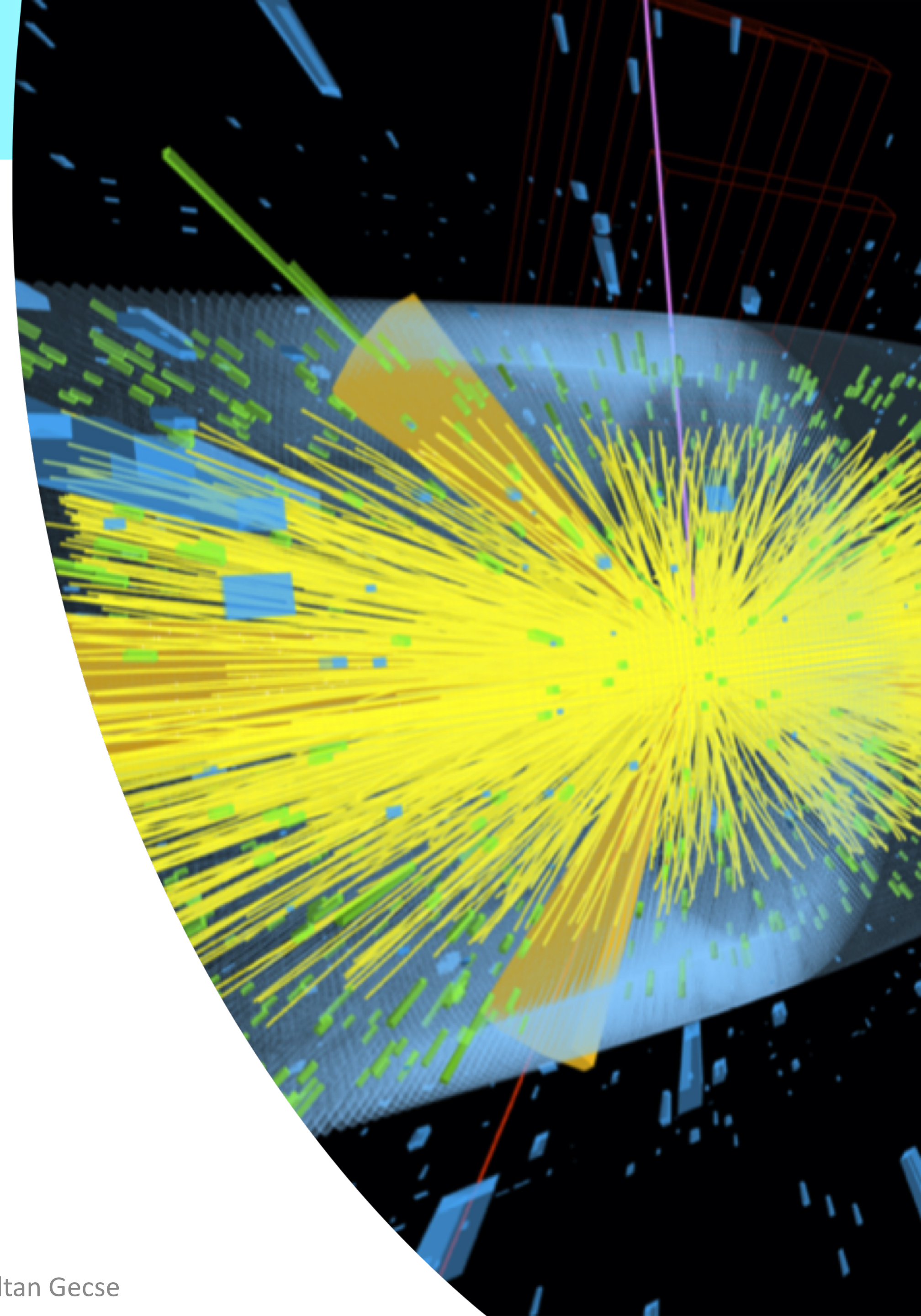
- State-of-the-art electronics (FPGAs) and high-bandwidth optical transmission, allowing for more granular input data and more complex filtering algorithms with pileup suppression
- Forefront of the uTCA revolution
  - New generation FPGAs with on-board processors, high bandwidth I/O, higher granularity in the trigger
- Innovative full implementation of High-Level-Synthesis (HLS) allowing physicists to code firmware
- Parasitic confirmation in 2015, default L1T in 2016



CTP7 board for L1 Calo

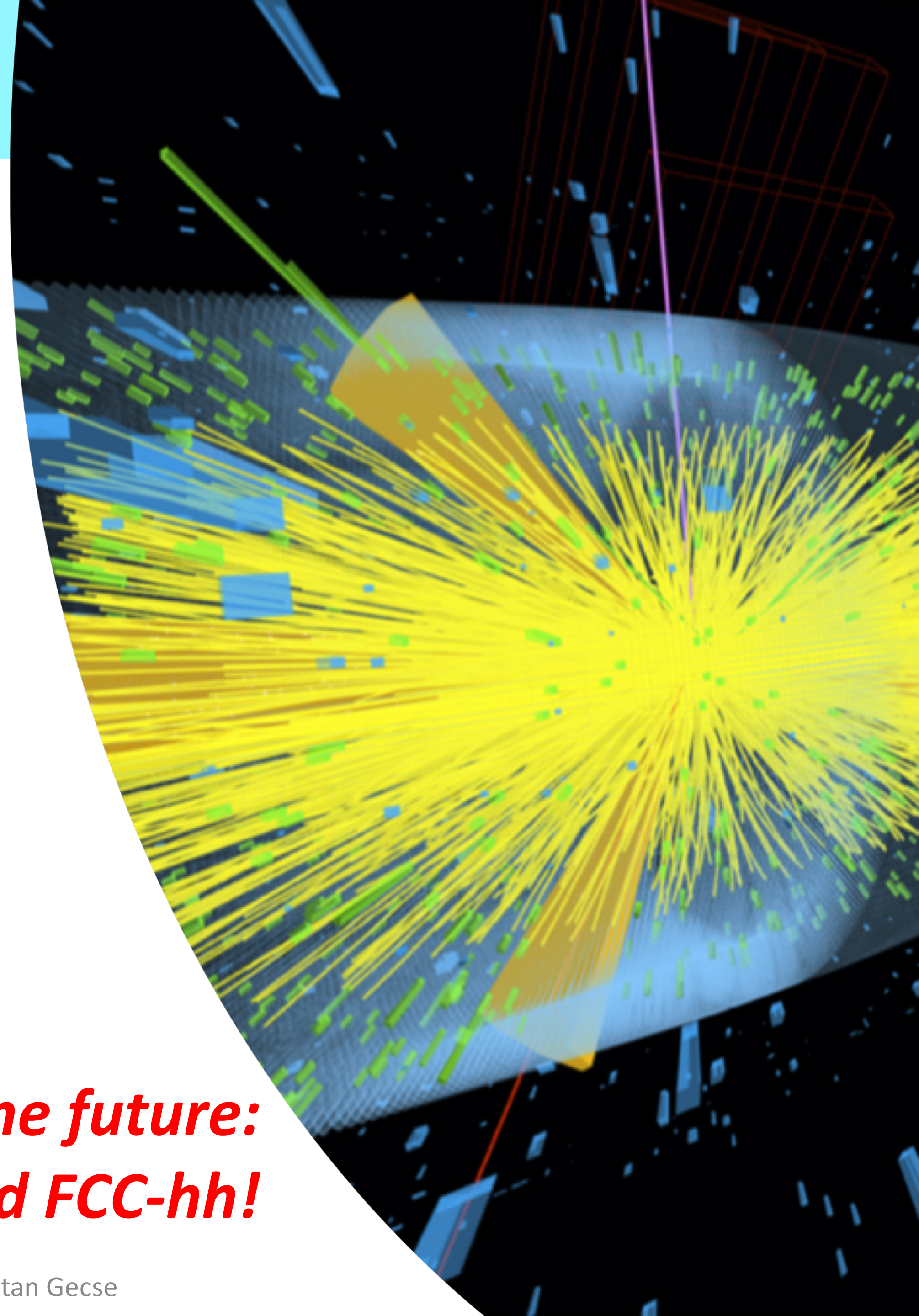
HL-LHC: The Challenge

- x7 higher instantaneous luminosity - w.r.t. nominal one
  - Occupancy in inner most layer up to 3.5 GHz/cm^2
  - 200 pile up events, about 10k tracks per event
- x10 higher radiation levels
  - Fluence up to 2.3x10^{16} 1 MeV neq/cm^2
  - Total ionizing dose up to 1.2 Grad



HL-LHC: The Opportunity

- Increase usage of silicon
  - To survive radiation
- Increased granularity and extended coverage
  - To cope with pileup
- Precision timing < 50ps
  - To separate collisions in time as well in space
- Faster processing in real time for trigger using high speed electronics
- More input to the trigger
  - including tracking at 40MHz



Preparing for the future:

PU of 800-1000 at HE-LHC and FCC-hh!

CMS Upgrades for HL-LHC

DOE and NSF

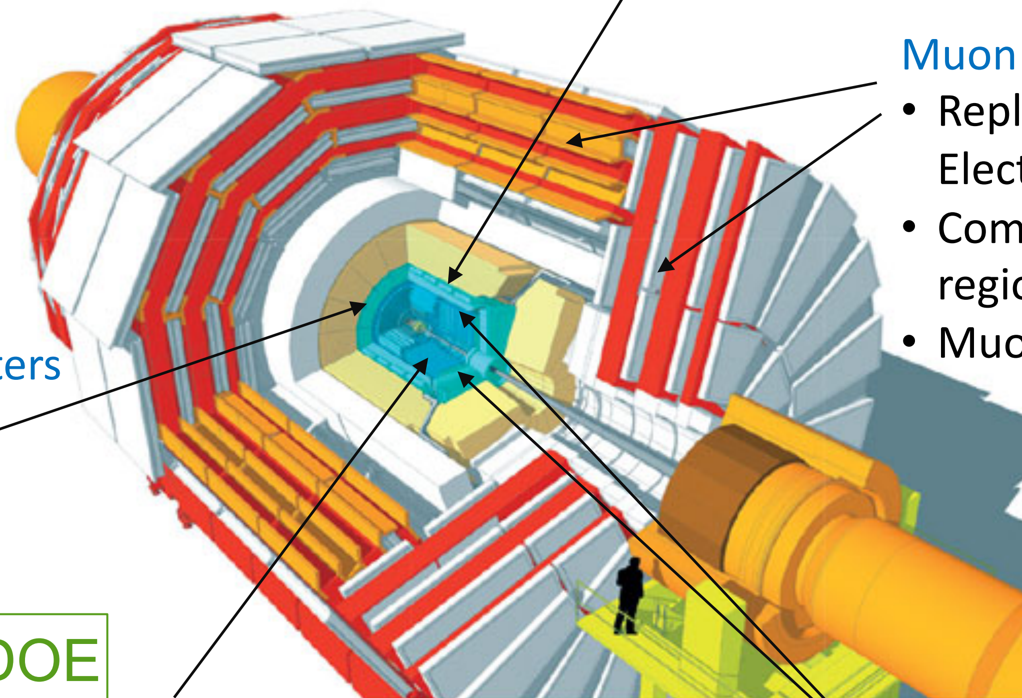
Trigger/HLT/DAQ
- Track information in L1-Trigger
- L1-Trigger: 12.5 μs latency – output 750 kHz
- HLT output 7.5 kHz

NSF

Barrel ECAL/HCAL
- Replace FE/BE electronics
- Lower ECAL operating temp. (8 °C)

NSF

Muon Systems
- Replace DT & CSC FE/BE Electronics
- Complete RPC coverage in region $1.5<\eta<2.4$
- Muon tagging $2.4<\eta<3$



DOE

New Endcap Calorimeters
- Rad. Tolerant
- High granularity
- 3D capable

DOE

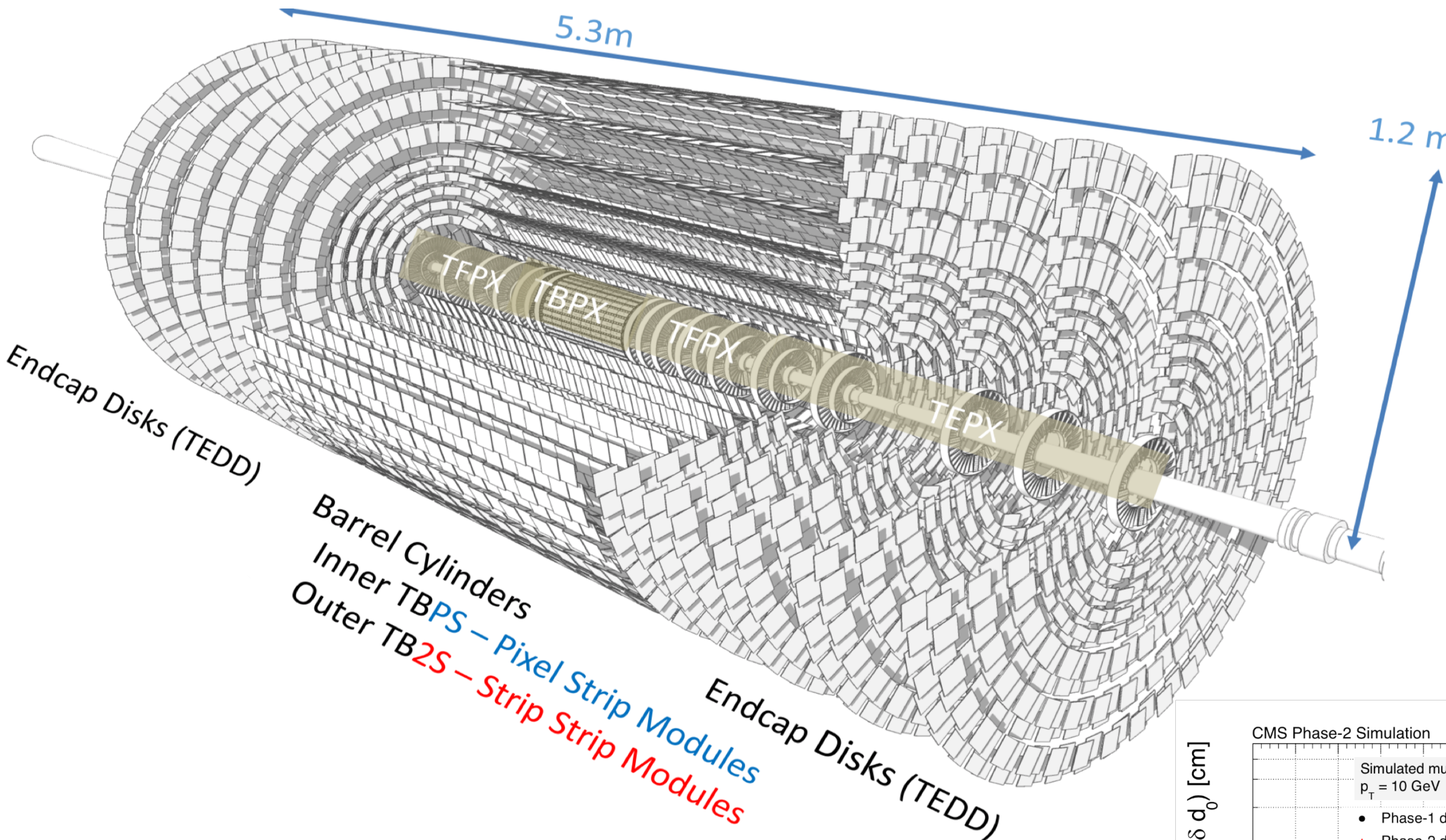
New Tracker
- Rad. tolerant – high granularity – significant less material
- 40 MHz selective readout (p_T>2 GeV) in Outer Tracker for L1 -Trigger
- Extended coverage to $\eta=4$

NSF

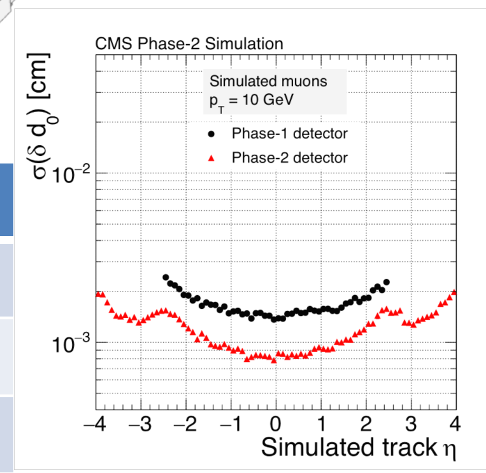
DOE

MIP Precision Timing Detector
- Barrel: Crystal +SiPM
- Endcap: Low Gain Avalanche Diodes

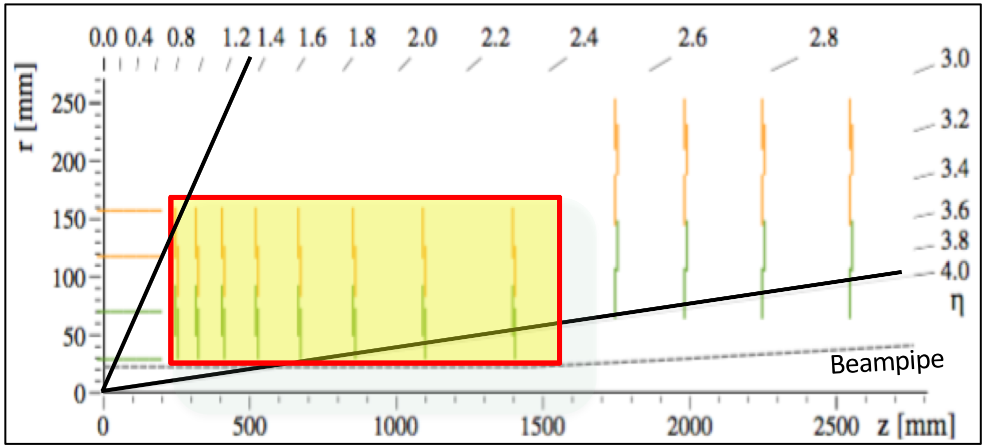
All Silicon Tracker



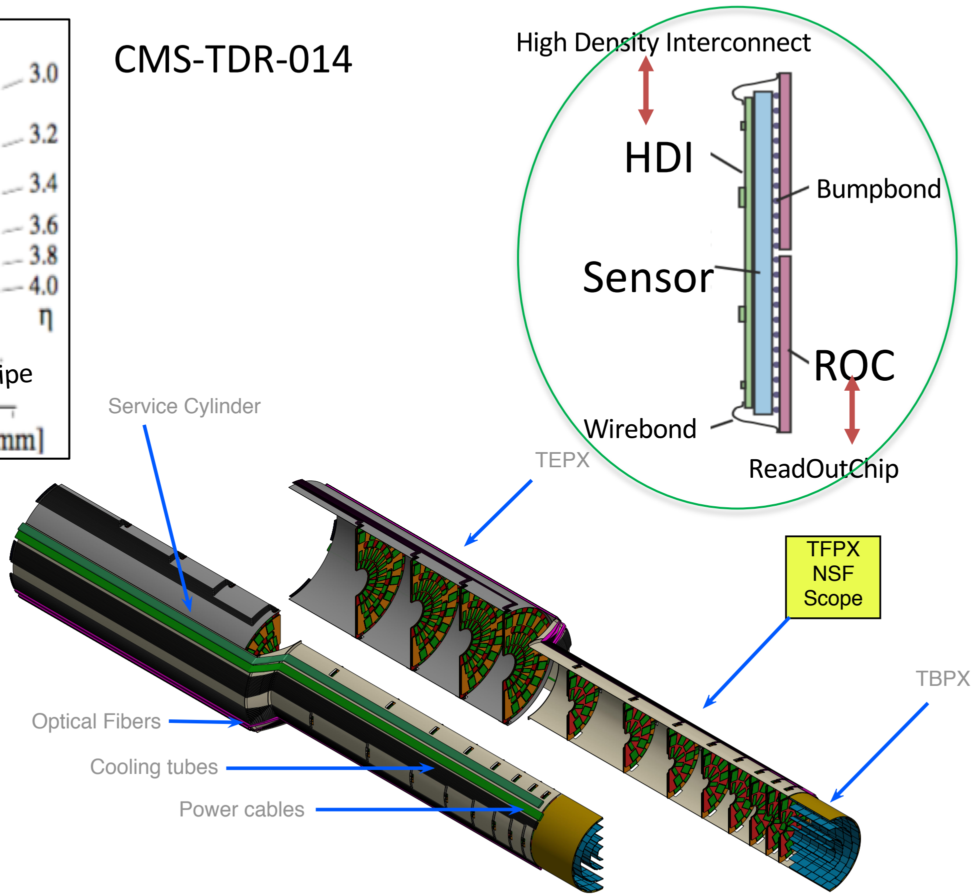
	Current Detector	Phase2 Detector
Inner Tracker	66 M, 1 m^2	2 B, 2m^2
Outer Tracker	9.3 M, 210 m^2	4.2 M strips, 170 M pixels, 192 m^2
Eta coverage	2.5	3.8



Inner Tracker: TFPX



CMS-TDR-014

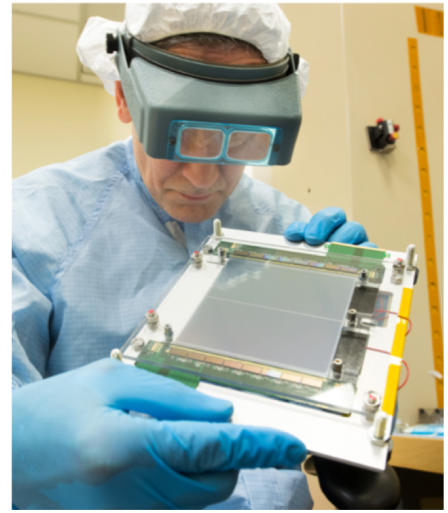


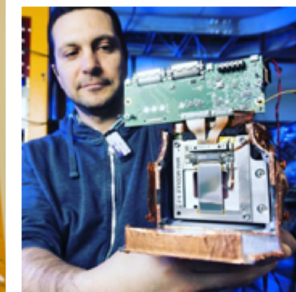
- Thin sensors (100-150 µm) for radiation hardness
  - 2.3×10^{16} 1 MeV neq/cm^2
  - 3D being explored
- Small pitch pixels (25x100 or 50x50 µm2) to cope with track density
- Frontier Readout Chip
  - RD53: 65 nm, low threshold 1000e
  - For 1.2Grad, 3.2GHz/cm2
- Serial powering, novel in a HEP experiment!
- Light structure

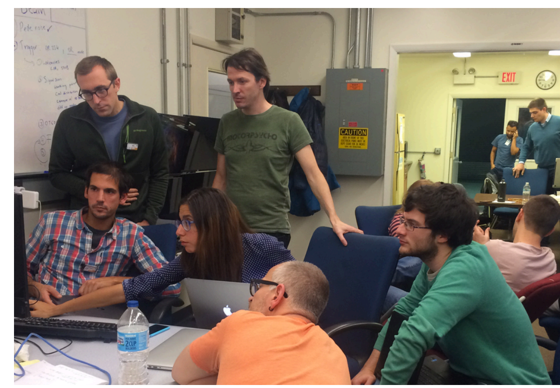
- Design: Data-Trigger-Control board and port-cards, service cylinders, inner tracker support tube
- Deliverables: 8+8 small disks with 1728 modules; associated mechanical structures (32 “Dees”), 4 complete service cylinders, 1 inner tracker support tube

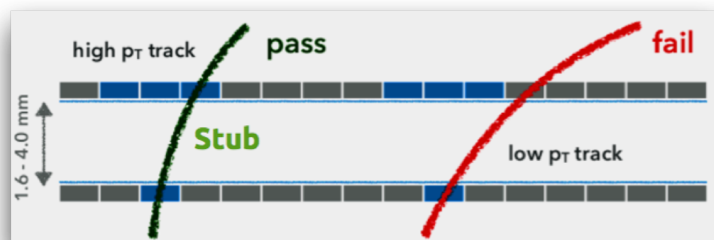
Outer Tracker

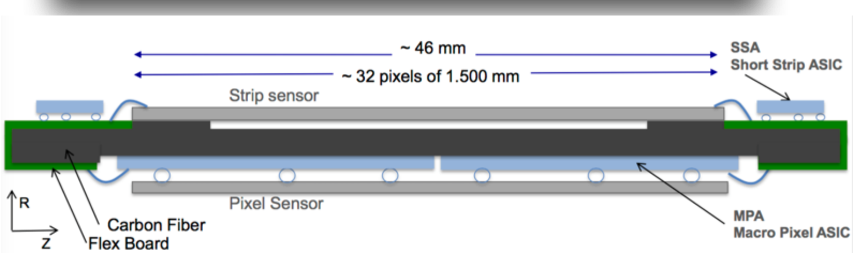
- Advanced technology enabling the transmission of tracking information to the Level-1 trigger at 40MHz for the first time at hadron collider
- Local data reduction based on two-layer silicon modules
  - Standalone units equipped with Front End ASICs that perform bottom and top sensor correlation providing track pT measurement
    - 2S modules with 2 strip sensors
    - PS modules with 1 pixelated sensor and 1 strip sensor
  - 200 tracks with p_T > 2 GeV leading to 15k stubs











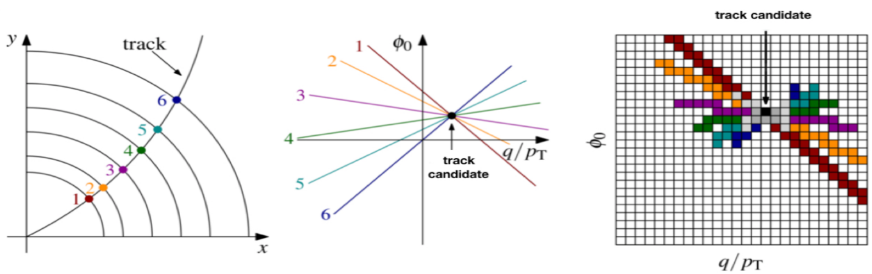
CMS-TDR-014

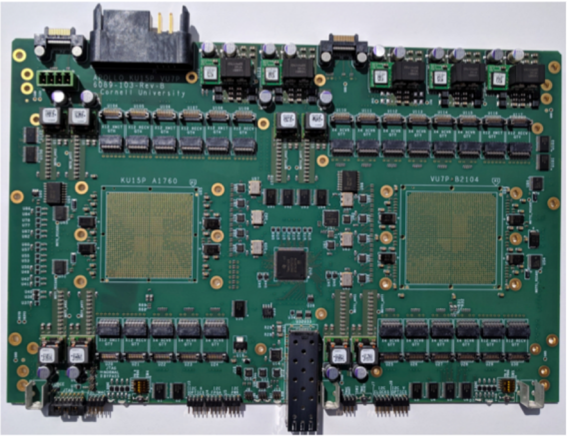
- Design: Flat Barrel, modules, DAQ/DTC
- Deliverables: 30% of the modules (4500), entire flat barrel, 100% of MaPSAs (6400), contribution to DAQ and DTC

Track Trigger

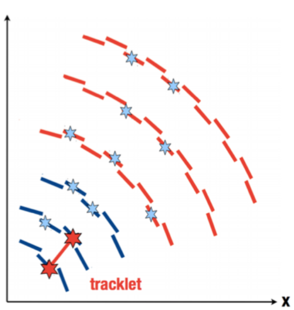
- Breakthrough technology to carry out quasi-full track reconstruction for p_T > 2 GeV tracks at 40MHz within 5μs
  - Capability to separate primary vertices
- Tracker segmented into nonants in ϕ providing input to Time Multiplexing Track Finder board exploiting state-of-the-art FPGAs
- Hybrid approach being considered
  - “Hough Transform + Kalman filter” and ”Tracklet”

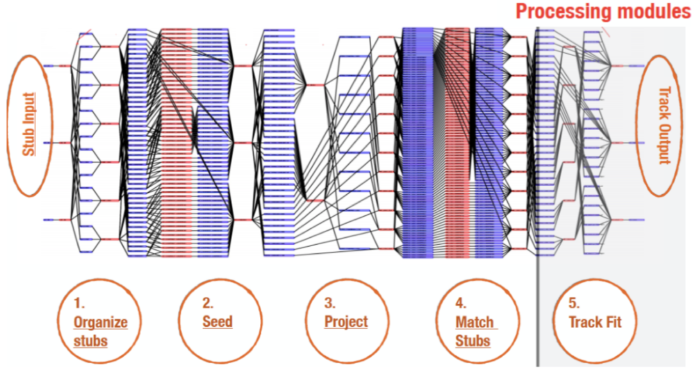
Hough Transform





Tracklet



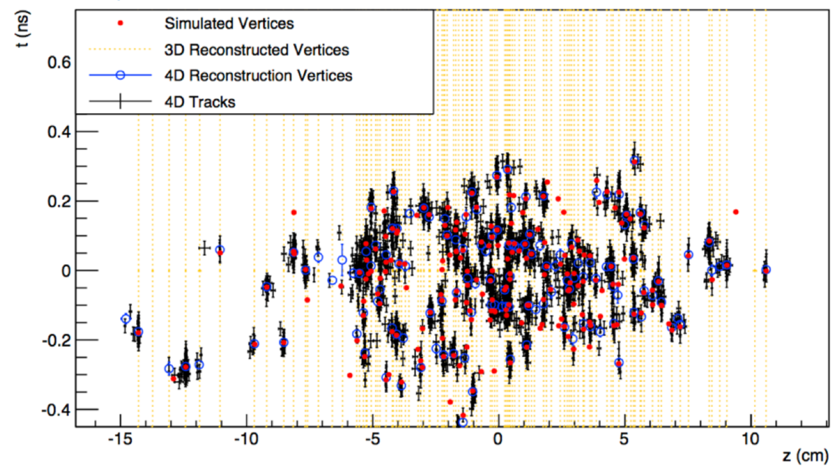


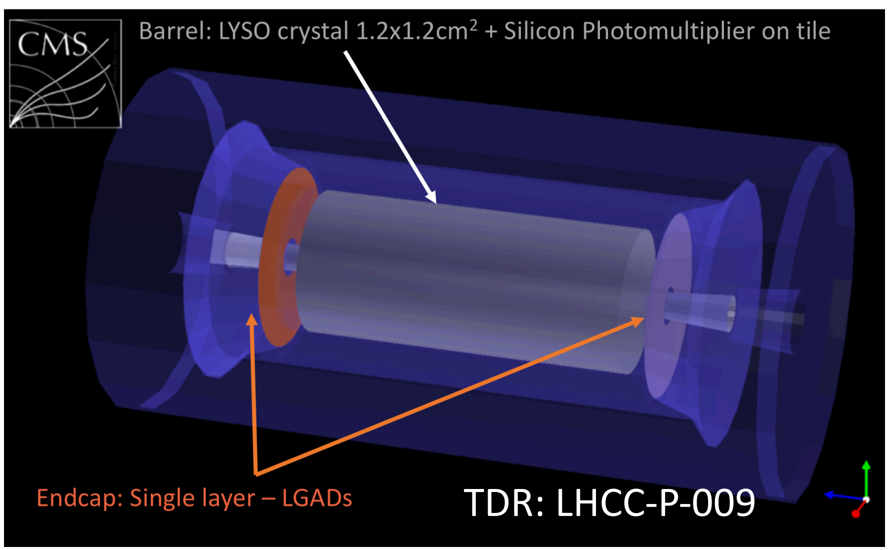
- Design: contribution to the design of the universal ATCA board and the FW development
- Deliverables: deliver 162 custom trigger boards

CMS-TDR-014

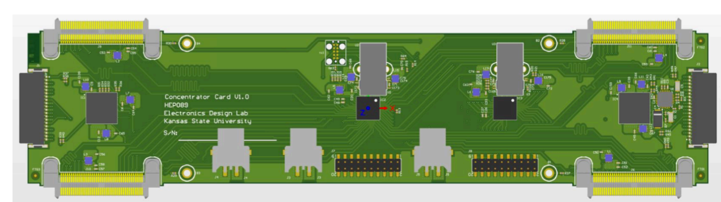
Barrel MIP Timing Detector: BTL

- Innovative detector providing timing information with 30 ps nominal timing resolution
  - Critical to PU mitigation, by 'slicing' the collisions into 30 ps intervals and bringing the PU down to the Run2-Run3 levels
    - Effective gain of O(20%) of luminosity for selected Higgs measurements
  - Enhancing capability of CMS to probe for long lived particles
- Barrel MTD:
  - Lyso Crystals 11x11 mm^2 + SiPM 4x4 mm^2, 250k channels, $40m^2$
  - Readout Chip with 20 ps timing resolution
- Challenging clock distribution(10 ps jitter)



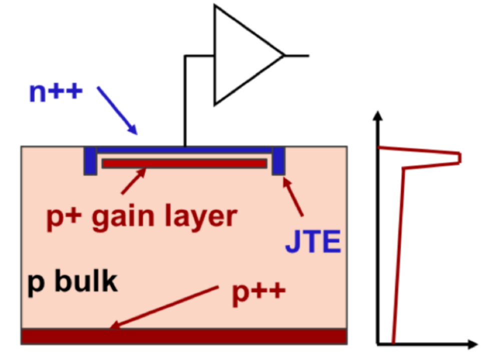


- Design: concentrator card, SiPMs, modules
- Deliverables: purchase 40% of Lyso crystals, 34% of SiPM; build 476 (100%) concentrator cards and 60% trays of modules & readout units



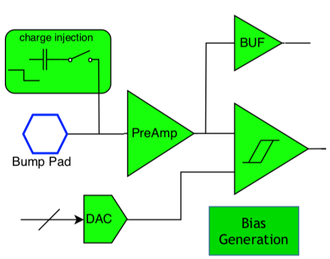
Endcap MIP Timing Detector: ETL

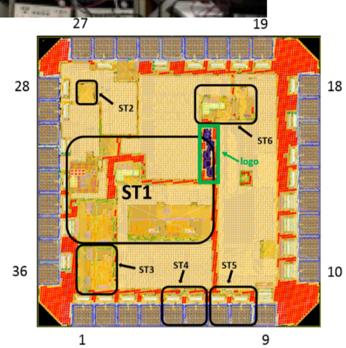
- Innovative detector providing timing information with 30 ps nominal timing resolution
- End Cap MTD:
  - LGAD: 1.3 x 1.3 mm^2, 9M channels, 15.8m^2
  - New silicon technology at hadron colliders!
- Cutting edge front end read out
- Single channel ASIC prototype meets performance requirements

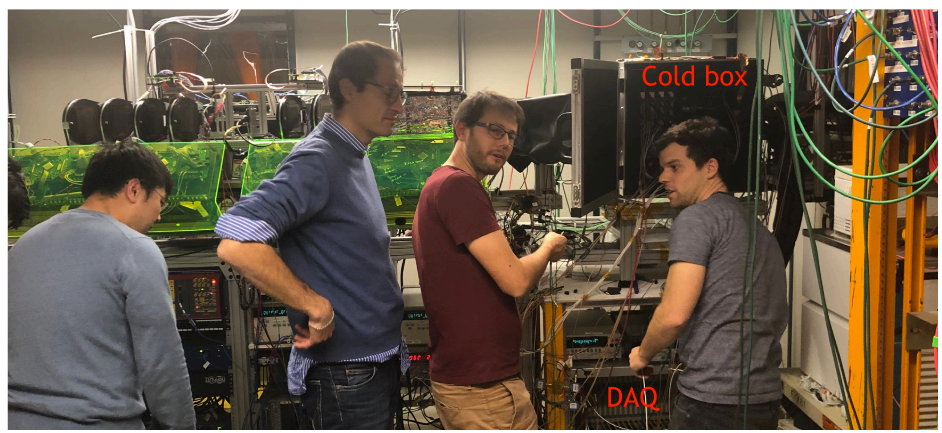


Ultra Fast Silicon Detector   E field

- <u>Design:</u> readout ASIC, LGAD sensors, mechanics & engineering
- <u>Deliverables</u>: purchase 50% of FE ASICs, assemble 50% of modules

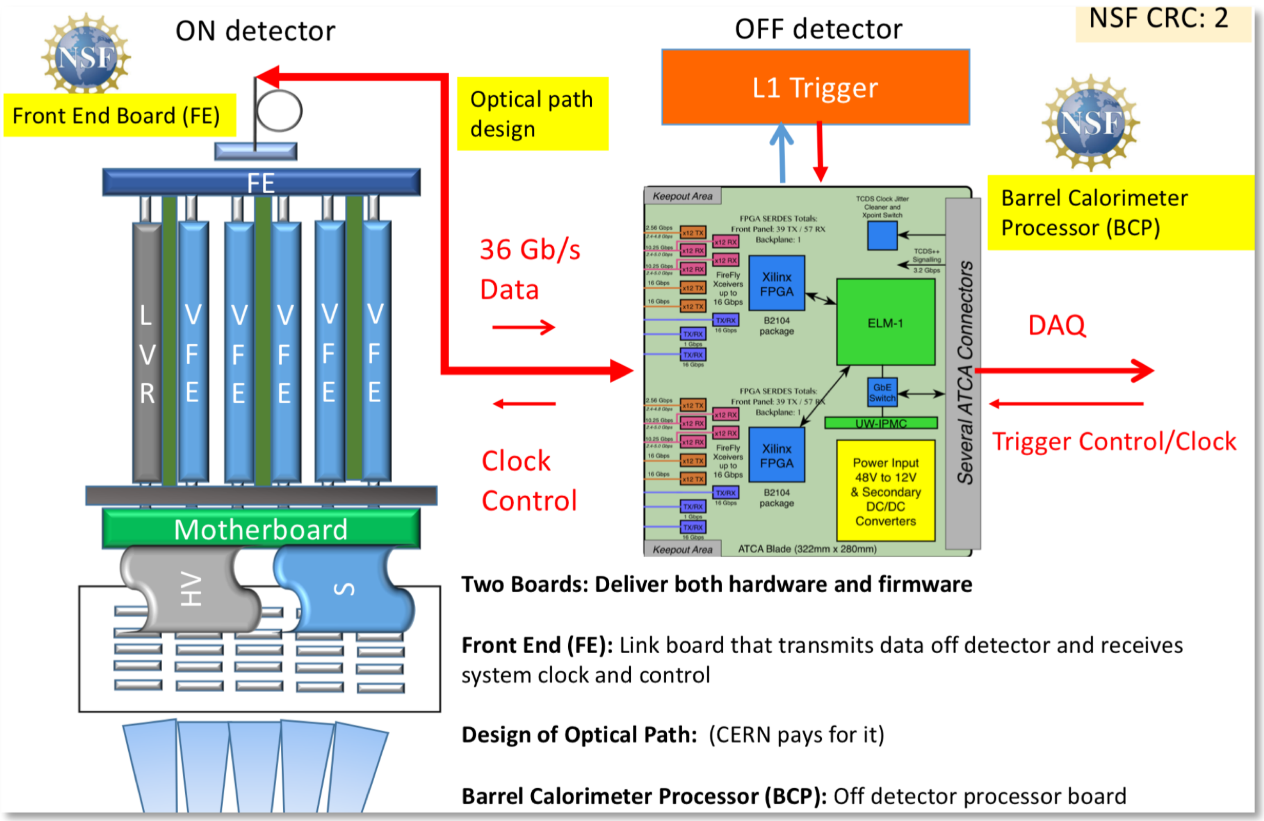






Barrel Calorimeter

- Electronics replaced for precision timing and better trigger granularity
  - Faster response preamplifier to give 30 ps resolution
  - High speed processor board to deal with greater spatial and time granularity
  - Higher bandwith transmission off detector to provide high granularity to the trigger



Two Boards: Deliver both hardware and firmware

Front End (FE): Link board that transmits data off detector and receives system clock and control

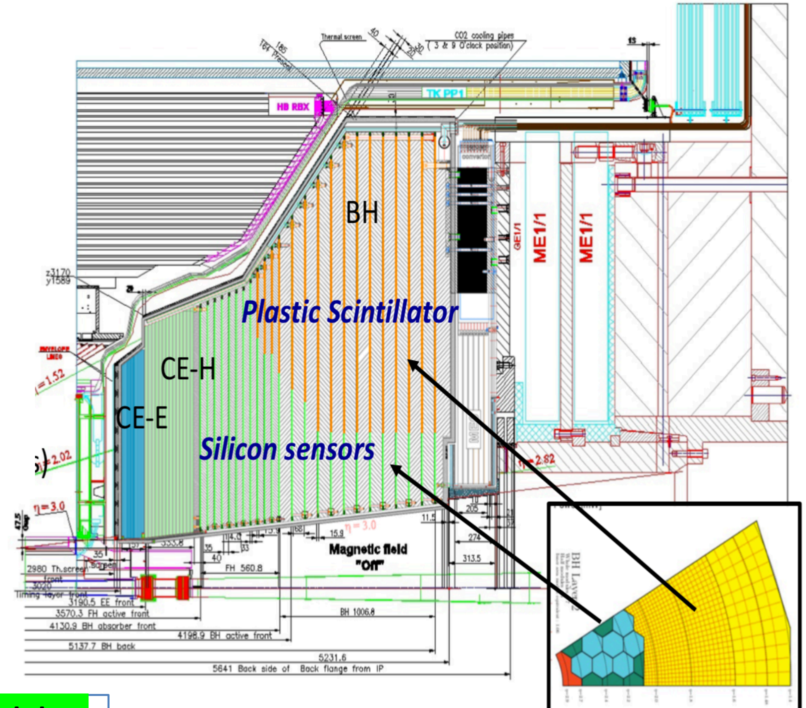
Design of Optical Path: (CERN pays for it)

Barrel Calorimeter Processor (BCP): Off detector processor board

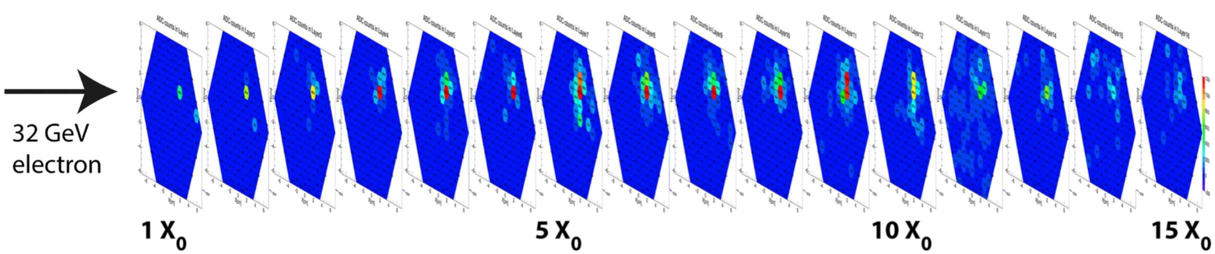
- Design:
  - Frontend board
  - Optical path
  - Processor board
- Deliverables:
  - 2448 Front End boards for ECAL & firmware
  - 126+ Barrel Calorimeter Processor boards for ECAL+HCAL & firmware

High Granularity Calorimeter

- Leap forward in imaging calorimetry!
  - Exporting silicon-based tracking to calorimetry
  - 28 electromagnetic layers, silicon modules (CuW/Pb absorber, 25 X_0, 1.7 lambda)
  - 22 hadronic layers: 8 Si + 14 Si/SiPM layers (stainless steel absorber, 8 lambda)
- High granularity (200k → 6M channels) in 3D and good timing resolution, 50 ps
- Good cluster energy resolution, detailed topological information, excellent 2-particle cluster resolving power
  - Suitable for particle-flow like reconstruction in high density environment

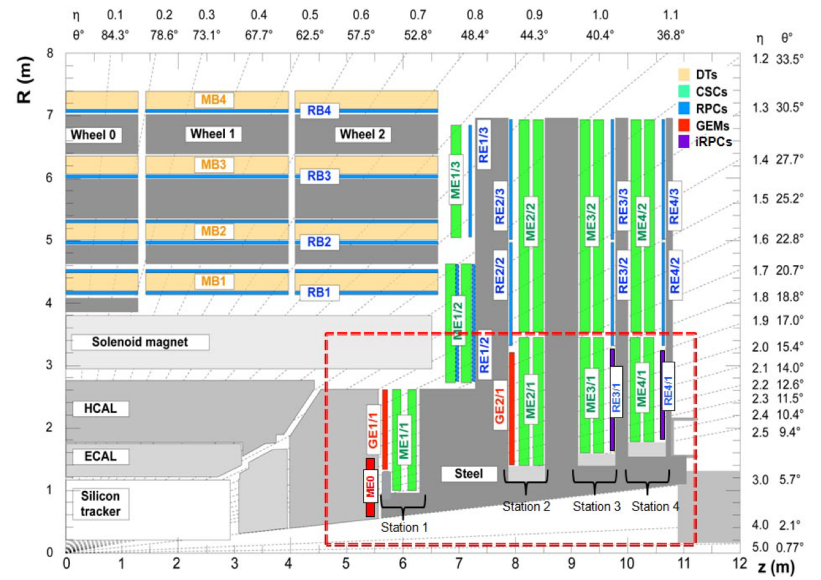


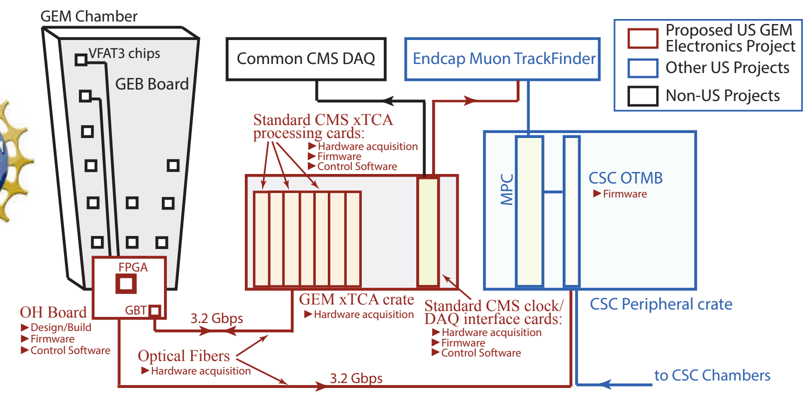
- Design: Silicon sensor, scintillator, module assembly, concentrator ASIC and motherboards, cassettes
- Deliverables: cassettes for the hadronic section, including sensors and modules



Muon Chambers

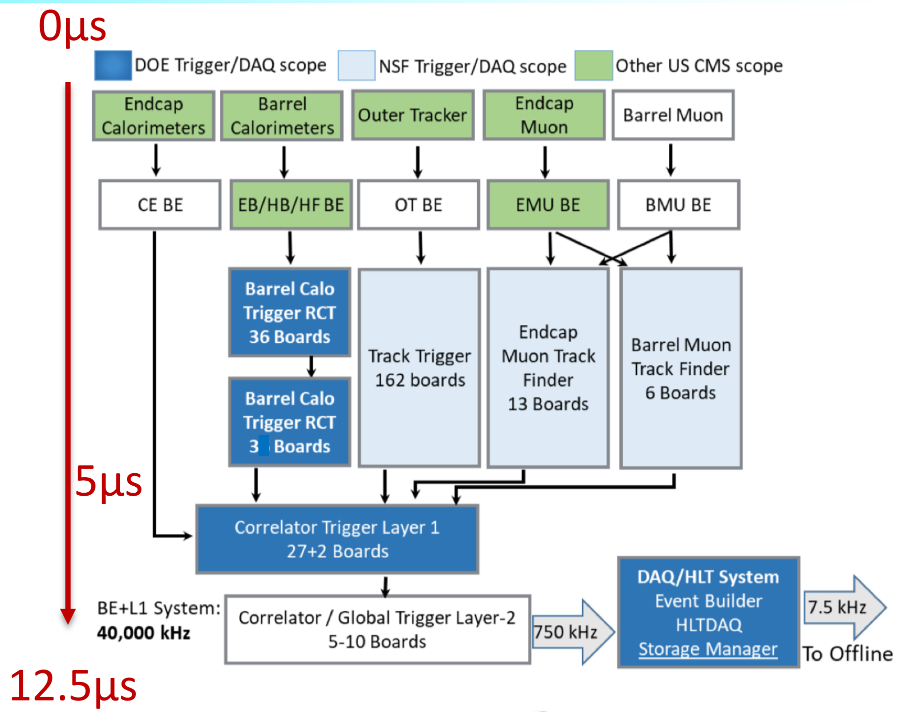
- Replace electronics to improve trigger performance
  - better p_T resolution enabling to lower the trigger threshold
- Extension of coverage to η = 3 with GEMs
- Upgrade of Cathode Strip Chamber (CSC) ME1-4/1 electronics to cope with data volume/BW:
- Data acquisition system for new GEM detectors:
  - GE1/1 and 2/1 work with CSC ME1/1 and ME2/1 to maintain muon trigger
  - ME0 works with ME1/1 to maintain trigger and extends offline coverage η=2.4−2.9
  - Transfer data to Level-1 muon track finder and central CMS DAQ system



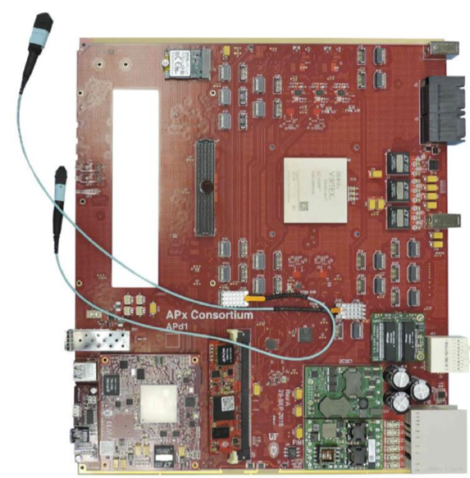


Trigger Upgrade

- Revolutionary L1 trigger
  - exploiting tracking, high granularity calorimetry, muon information
  - matching tracks with calorimeter clusters, fitting muon and tracks together
  - producing complex objects with corrections for PU
- Heterogenous architectures at HLT
  - coprocessors to run a specific program, *e.g.* GPUs for tracking (mkFIT project supported by SciDAC: $17.5M grant from U.S. Department of Energy's Scientific Discovery through Advanced Computing)

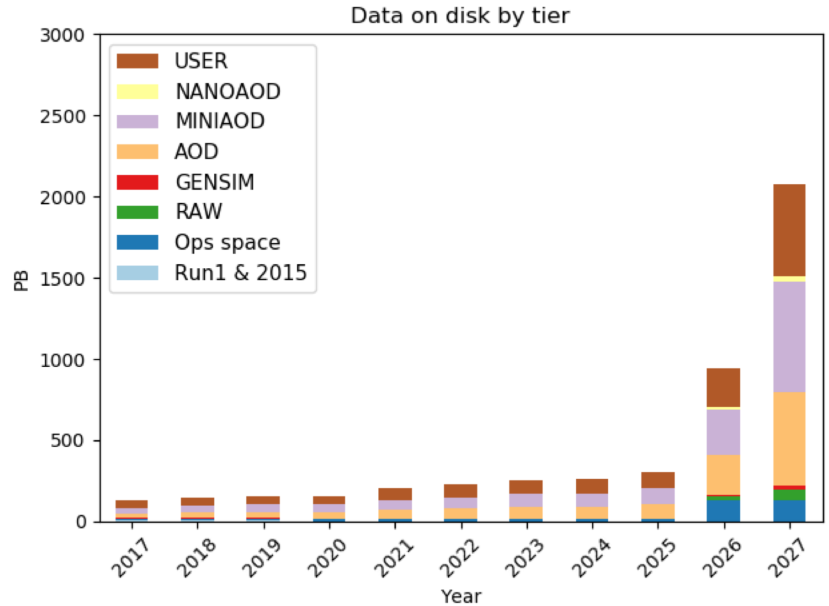


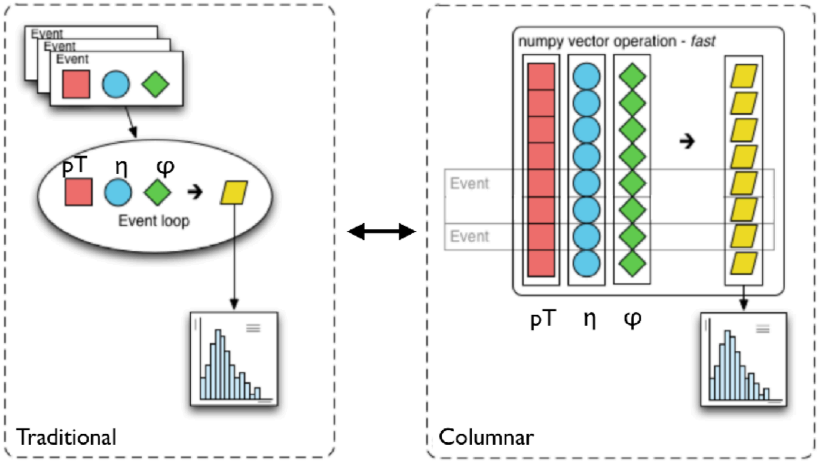
iris hep
Institute for Research & Innovation in Software for High Energy Physics



Software at HL-LHC

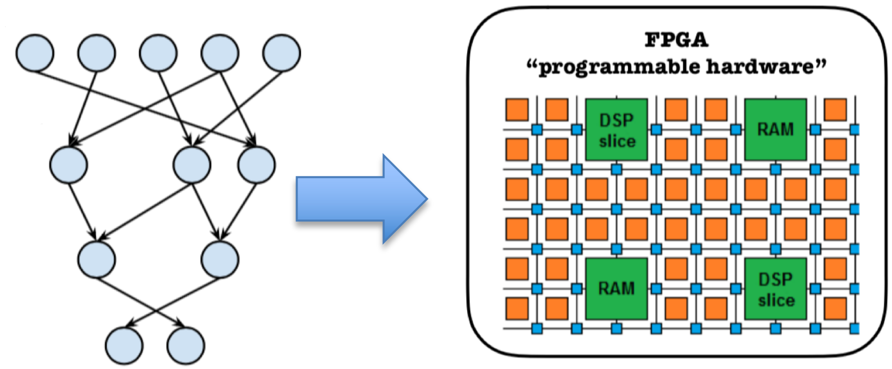
- Already > 100 petabytes of raw data
- x60 more at HL-LHC!
  - innovative solutions to the big-data challenge in HEP for decades to come are essential (https://news.fnal.gov/2019/04/cms-explores-new-technologies-for-big-data-analysis)
- Pushing the frontier in many areas:
  - Processing will utilize accelerators (GPUs, FPGAs, …) because of hardware trends and industry demand
  - Facility concepts will use commercial clouds and DOE/NSF high-performance-computing centers through FNAL HEPCloud portal
  - Storage and delivery of data through new storage technologies and caching
  - Analysis facility concepts (FNAL Striped, Apache Spark, …)
  - Declarative models for user code
  - Columnar approach to data analysis loading arrays of variables (columns) spanning several events (rows) and applies array programming expressions to these columns

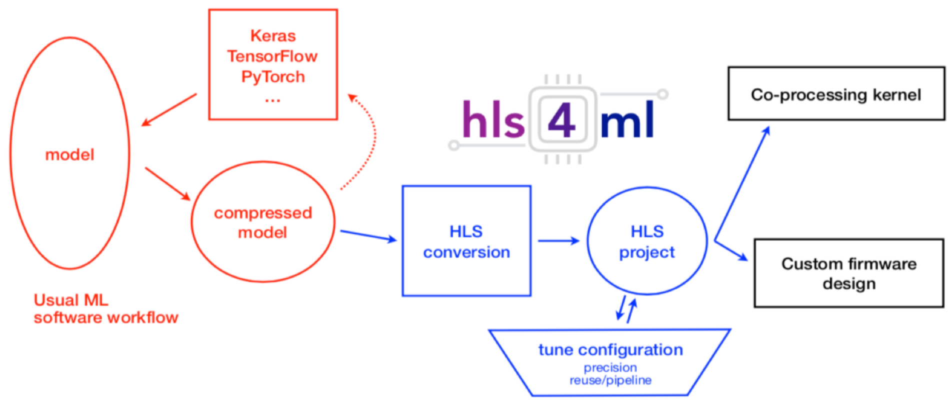




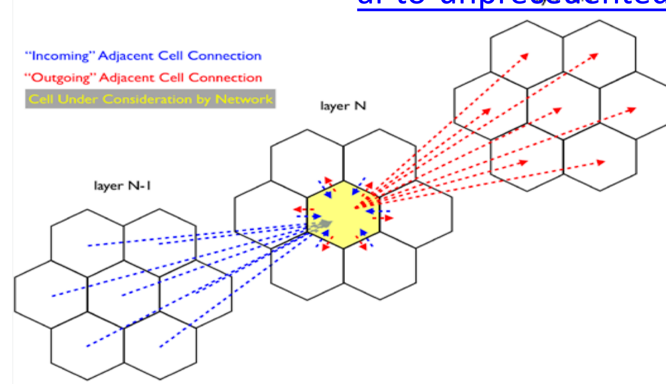
Machine Learning for Trigger and Computing

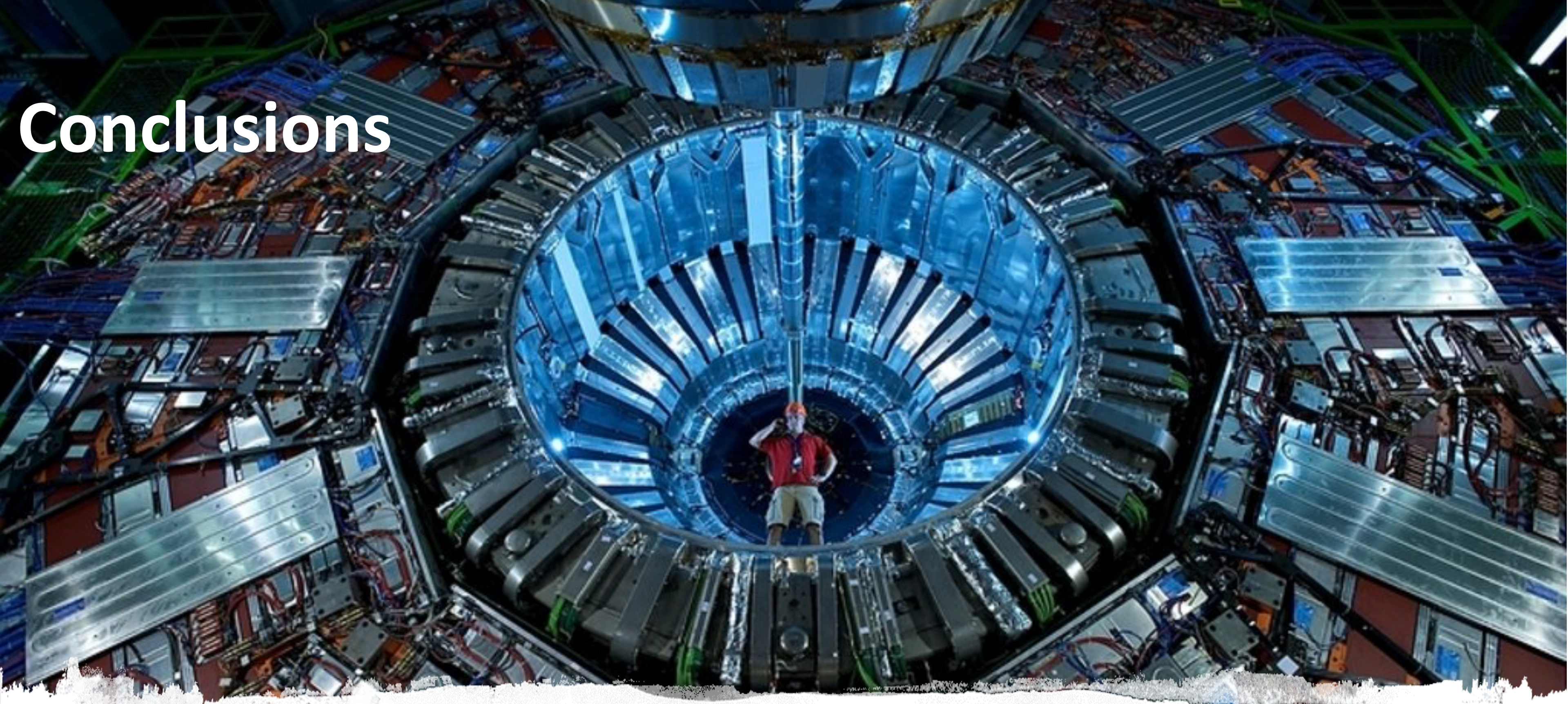
- Neural Networks naturally implemented in FPGAs
  - Results in faster inference
- New tool “hls4ml” to translate ML algorithms into FPGA firmware
  - JINST 13 (2018) P07027
- Deep-neural-network inferred in <100ns
  - Suitable for L1 trigger
- ML to help with offline computing problem
- Recasting reconstruction software in terms of ML
  - HEP.TrkX work with graph neural networks
  - Graph Neural Networks for Accelerating Calorimetry and Event Reconstruction (Awarded LDRD)





https://news.fnal.gov/2019/01/fermilab-scientists-help-push-ai-to-unprecedented-speeds/





Conclusions

- The LHC and HL-LHC will deliver an unprecedented amount of collisions
- To fully exploit the discovery potential of these datasets, cutting edge detectors are being designed and built with significant US contributions
- Excellent opportunities for R&D in:
  - Silicon sensors and SiPMs
  - ASICS, high speed optical readout, triggers
  - Heterogeneous computing and machine learning algorithms

A special time for collider physics experiments!