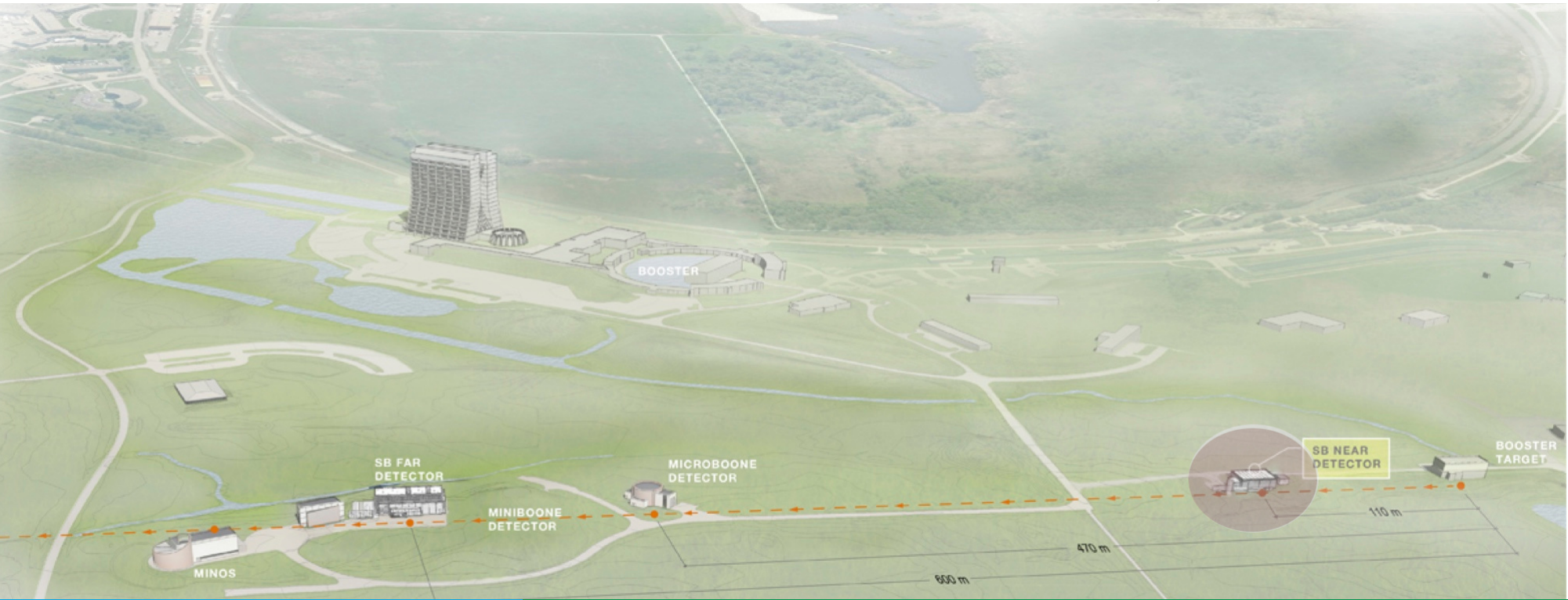
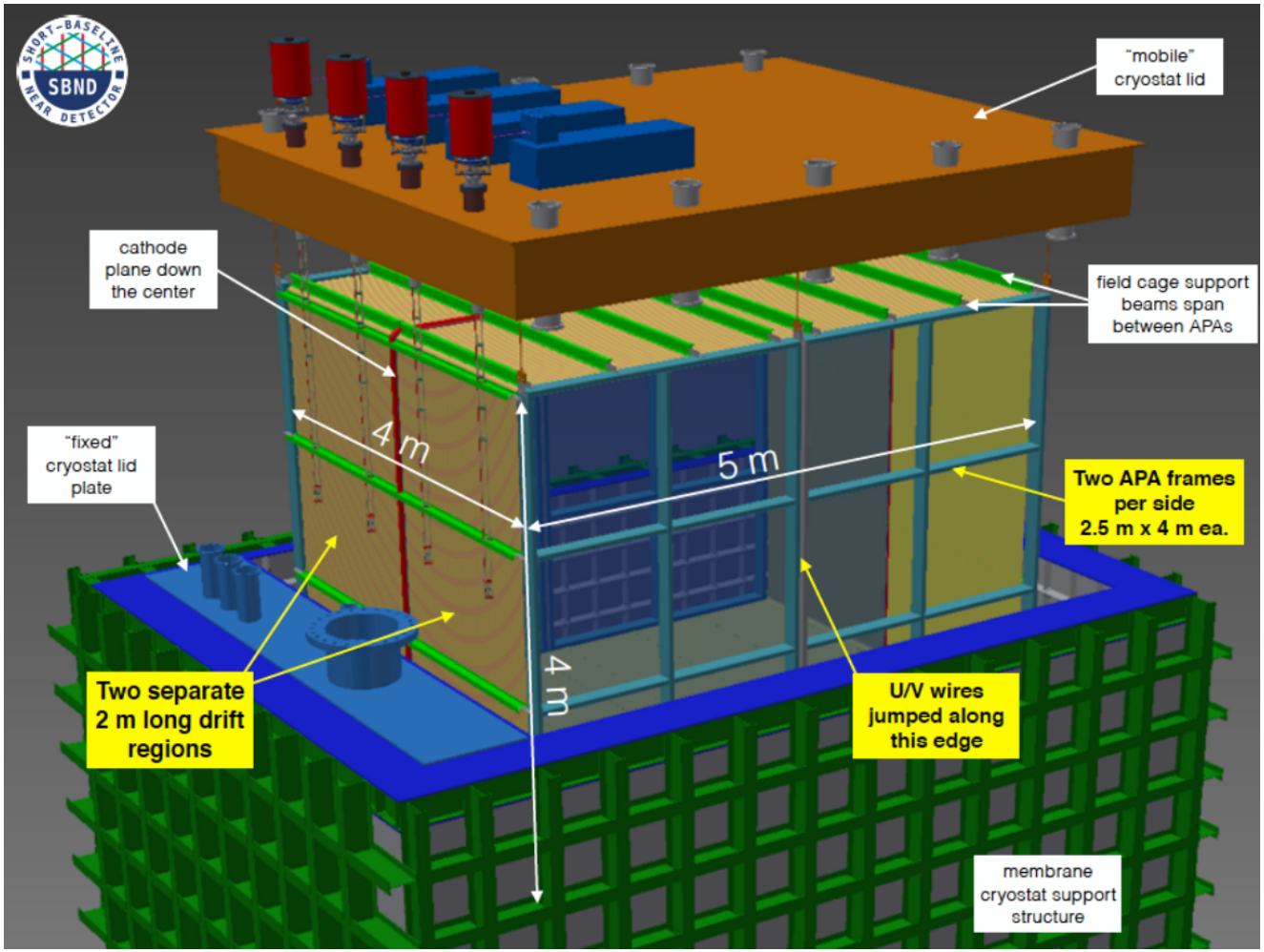
New Perspectives
Ryan LaZur

June 10, 2019

Overview of SBND Cold Electronics

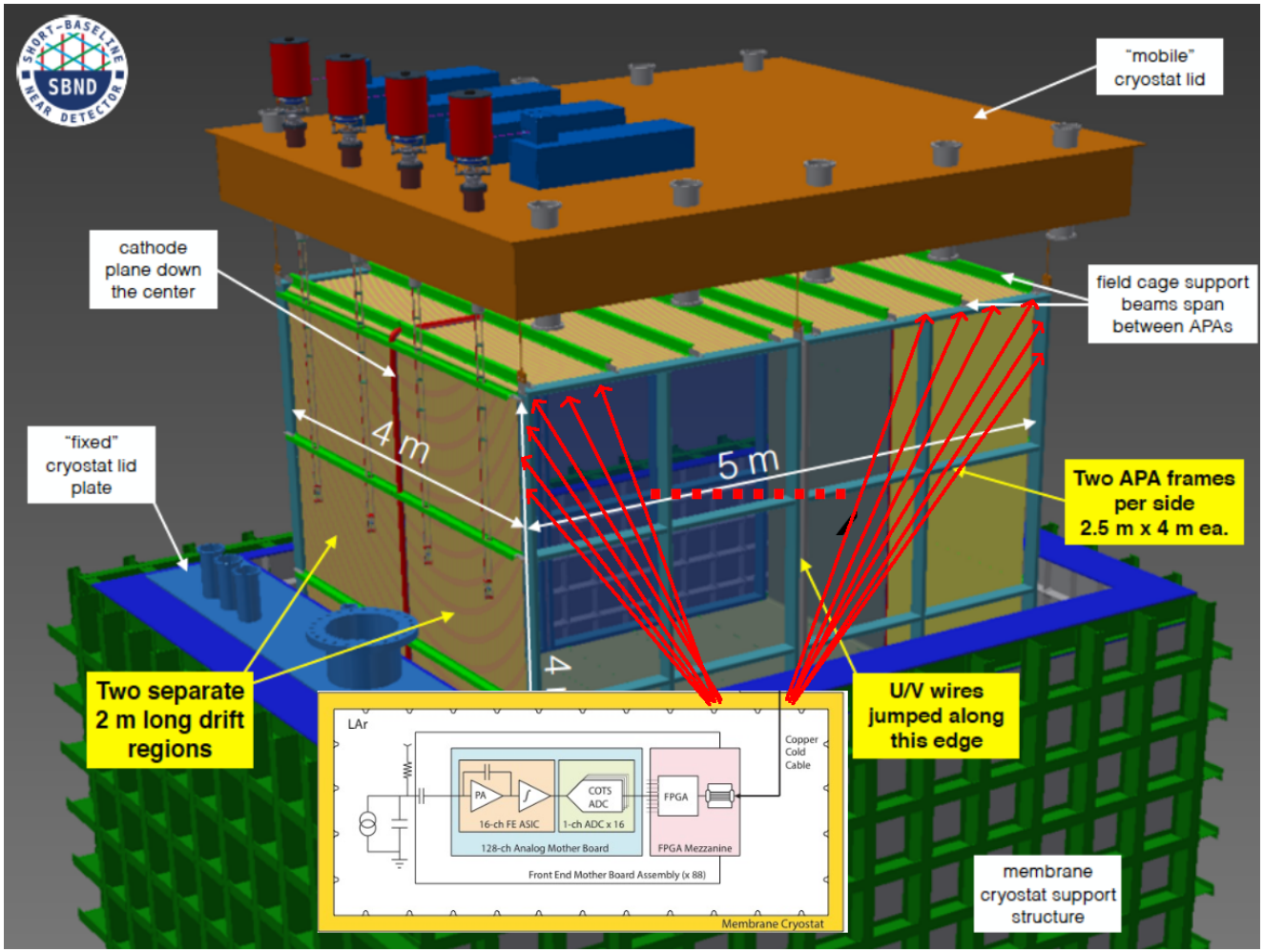


SBND TPC Electronics



You listened to an overview of SBND (in 10 minutes)...

SBND TPC Electronics

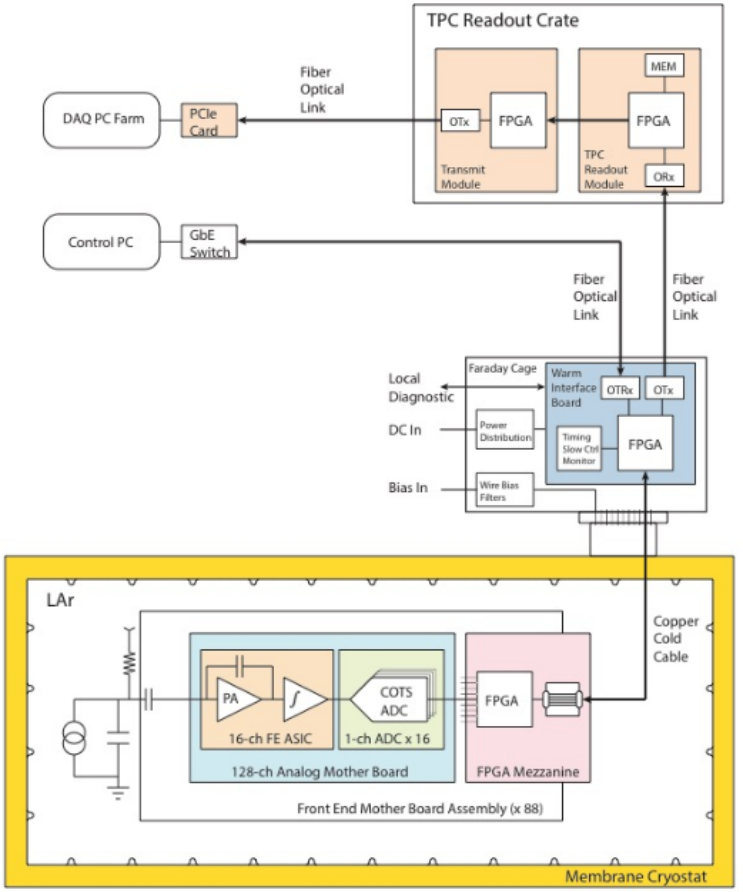


...Now we will discuss the readout electronics in more detail!

SBND Readout Electronics

Brief Overview

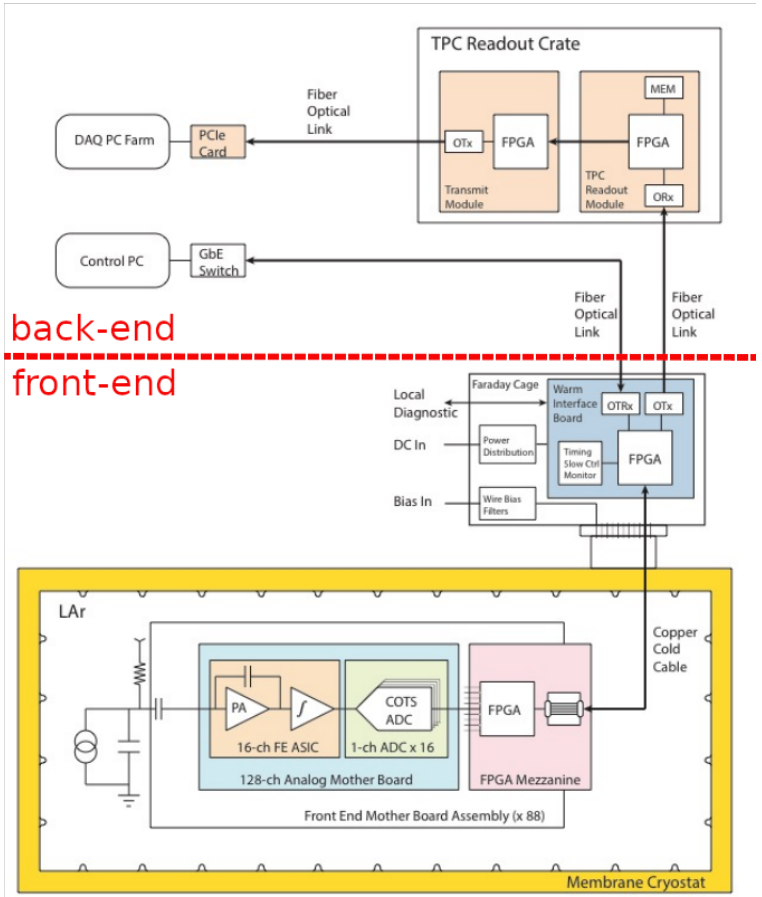
- The goal of the TPC readout electronics is to amplify, shape, digitize, and losslessly compress TPC ionization signals while maintaining high signal-to-noise ratio
- The SBND electronics build upon technology employed at MicroBooNE and has similar components to ProtoDUNE
  - See Maura's talk at noon tomorrow



SBND Electronics

Front-end and Back-end

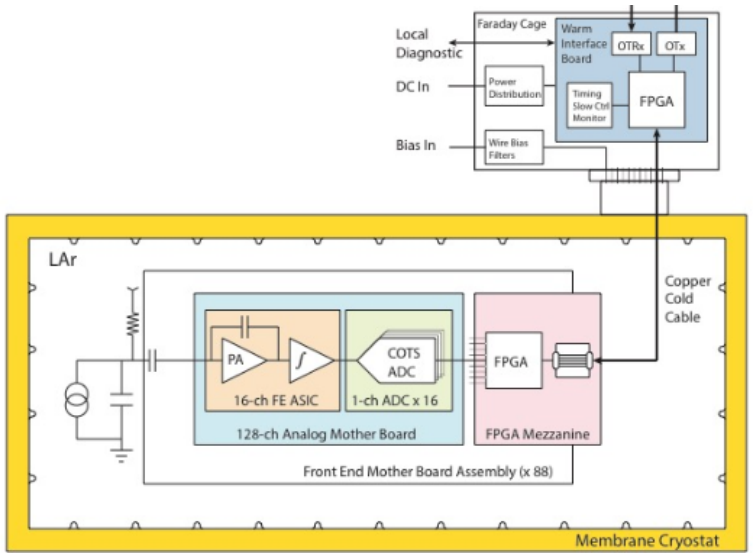
- Components inside the cryostat provide gain and shaping then digitize and multiplex the signal
- Warm interface components configures components inside cryostat and convert digital signal to optical and can be programmed by external PC
- The back-end (BE) electronics compress and store the data for later analysis



SBND Front-End Electronics

Cold electronics

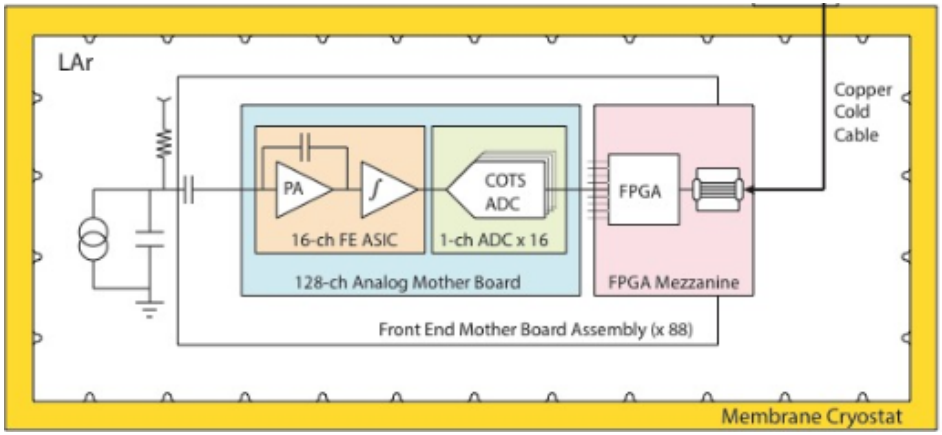
- FE motherboards (FEMBs)
  - FE application specific integrated circuits (ASICs)
  - Analogue-to-digital converter (ADC) ASICs
  - Field-programmable gate arrays (FPGAs)
  - Other components qualified in cryogenic operation
- Warm interface boards (WIBs)
- Cold cables



FEMB

Front-End Motherboard

- Each FEMB handles 128 channels of TPC readout
  - 8 FE ASICs $\times$ 16 channels/ASIC $=$ 128 channels
  - 128 single-channel commercial-off-the-shelf (COTS) ADCs
- Single FPGA per FEMB multiplexes the 128 channels and stores input from DAQ/external PC
- 11,264 channels per SBND / 128 $=$ 88 FEMBs

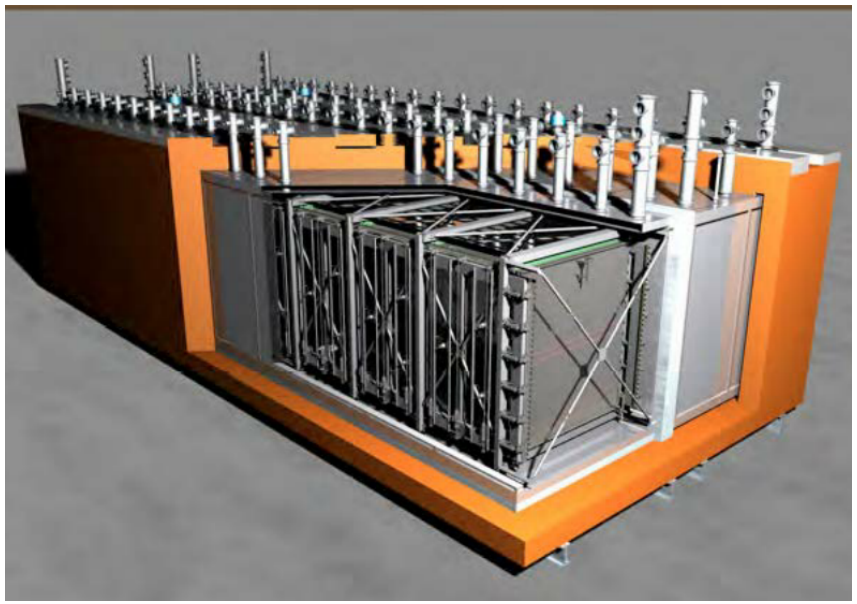


SBND Cold Electronics

Motivation

Why put the FEMB in the cryostat?

- Increased detector design flexibility
  - Less cabling
    - ★ Less TPC penetrations
    - ★ Less outgassing
- Improved signal-to-noise ratio
  - Reduced thermal and capacitive noise



ICARUS multiplex outside cryostat necessitating many feedthroughs

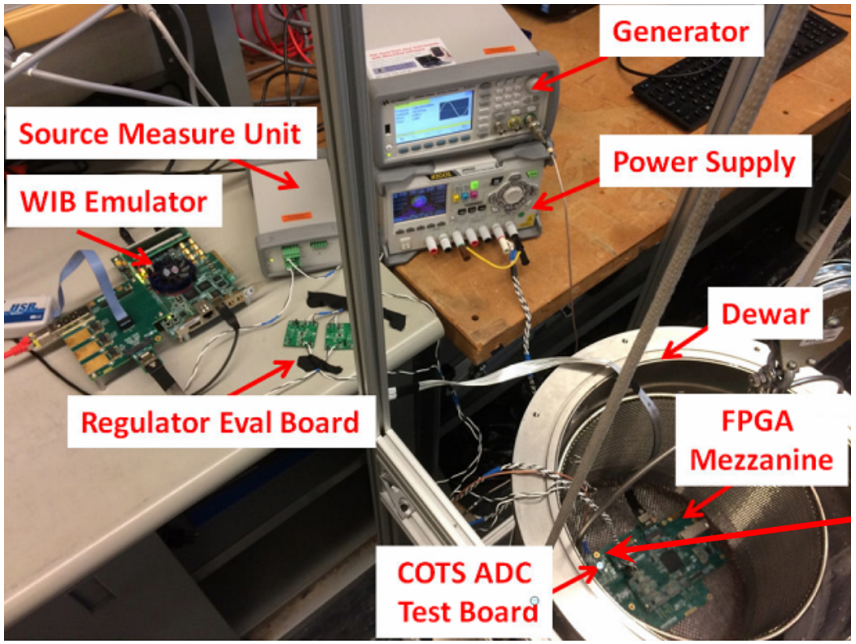
Electronics Noise:

$$ENC^2 \approx \frac{1}{2} A_1 \frac{e_n^2 C_{in}^2}{t_p} + A_2 \pi C_{in}^2 A_f + A_3 \left(q_e I_0 + \frac{2 k_B T}{R_b} \right) t_p$$

ADC ASIC Testing

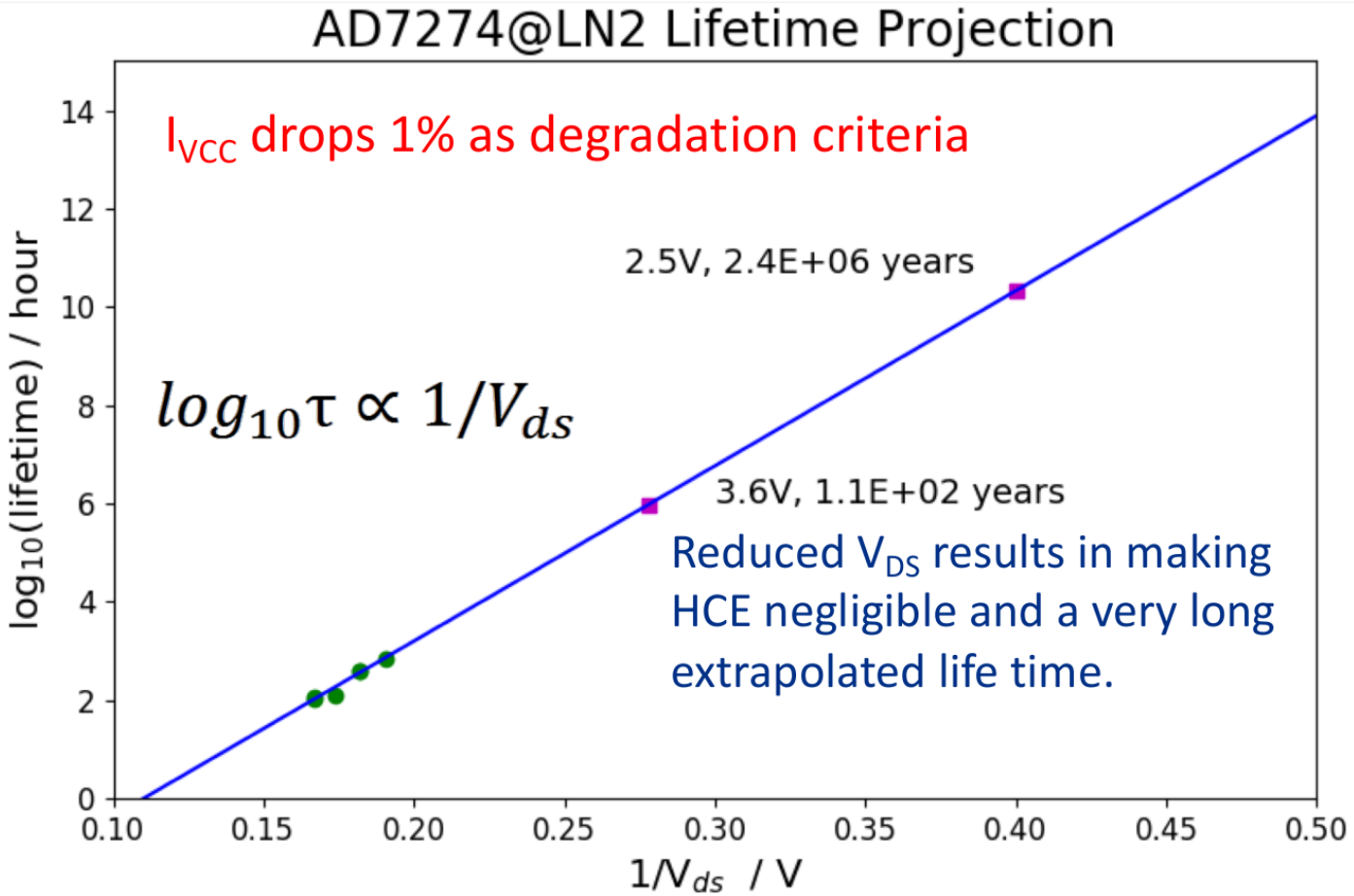
Test Setup

- The SBND ADC ASICs, unlike those in MicroBooNE, are in the LAr
  - SBND will employ commercial (COTS) ADCs
- Tests at BNL and Manchester qualify the ADC ASICs for use in SBND



ADC ASIC Testing

Lifetime Results

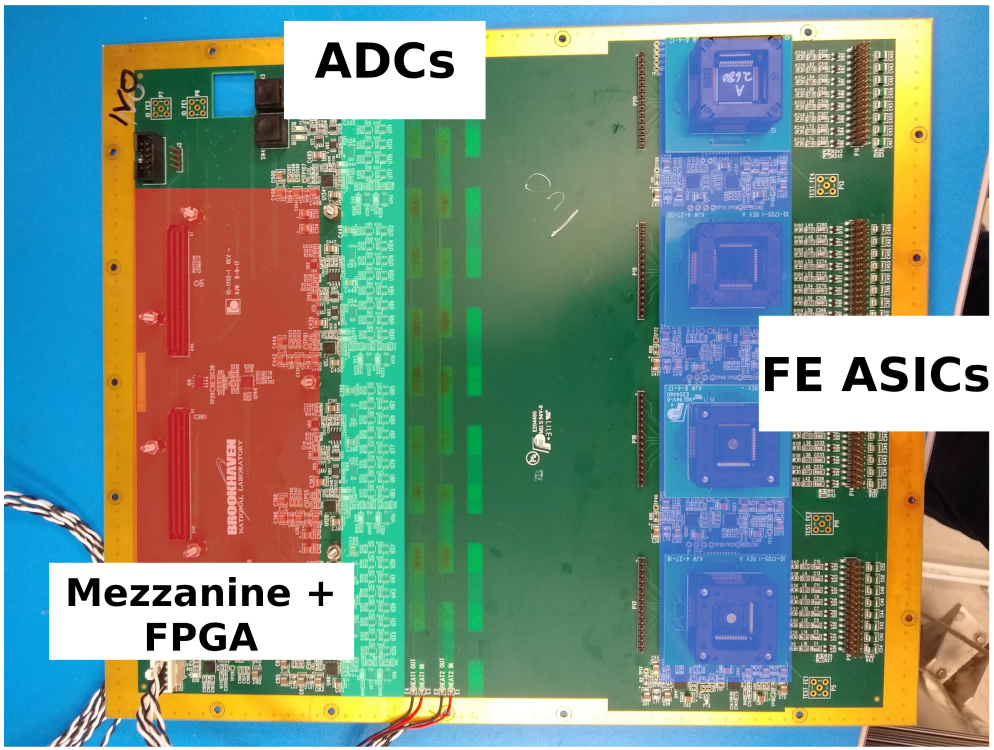


Lifetime projection is $\sim 2.4 \times 10^6$ years at 2.5V operation

FE ASIC Testing

Testing Setup at BNL

- Custom extended motherboard submerges FE ASICs in LN2
- Custom MSU Cryogenic Testing System (CTS) allows for quick, semi-automated testing



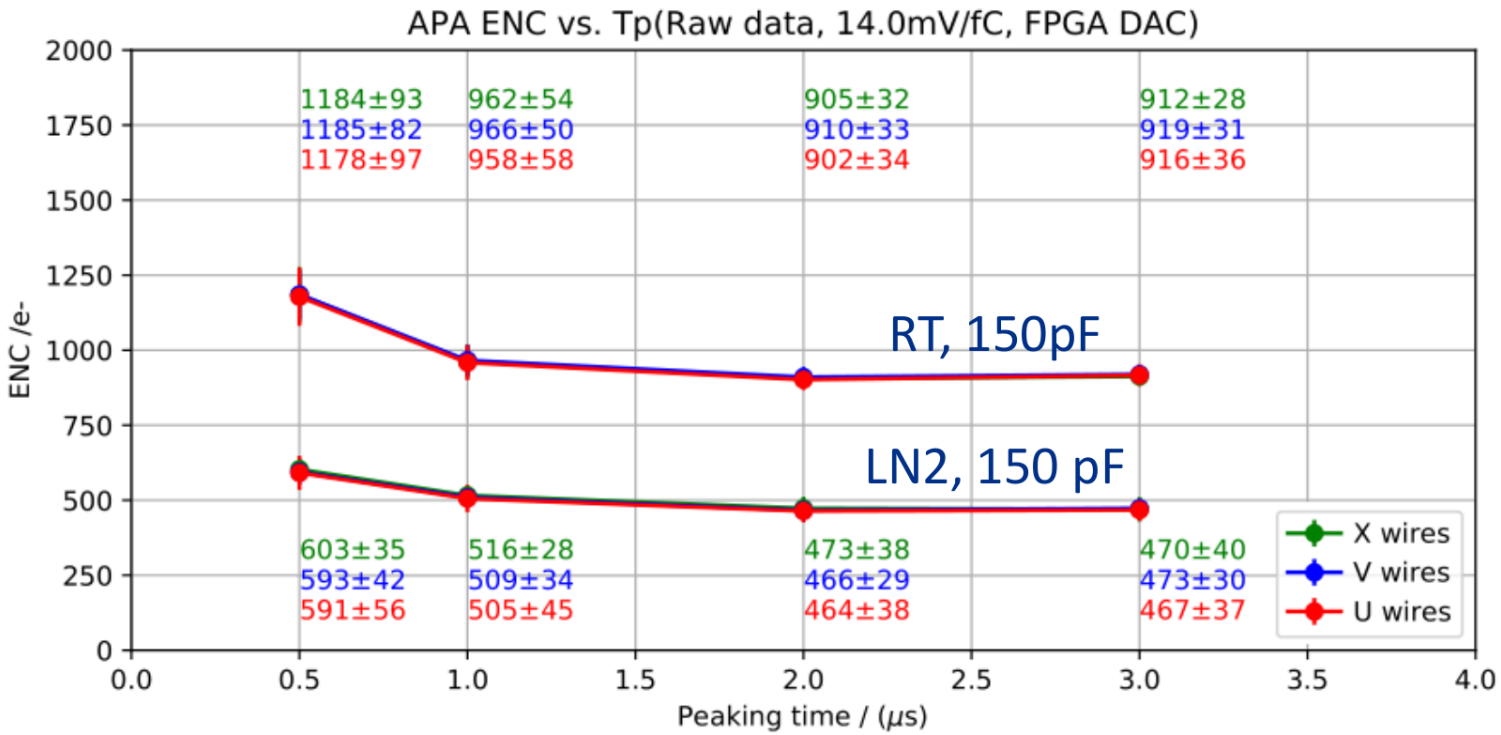
FE ASIC Testing

Testing Summary

- Each FE ASIC was tested for proper pedestal, pulse response, and power cycle resilience
- 1,200 LArASICv7 passed testing at BNL over the course of < 2 months to be used at ProtoDUNE and SBND
  - Testing time was optimized to take ≈ 1 hour with significantly reduced chip breakage
  - LArASICv7s are custom BNL FE ASICs used at SBND and ProtoDUNE
- A similar testing procedure should be implemented for DUNE

FEMB Performance Test

Room vs Cryogenic Temperatures



- Equivalent noise charge (ENC) is a noise metric
- Factor of two reduction in noise in cold (LN2) vs room temperature

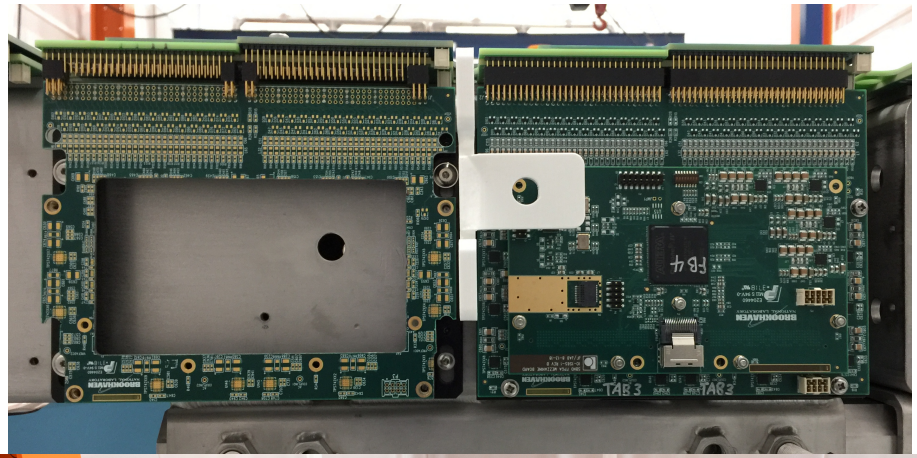
Cold Electronics Activities

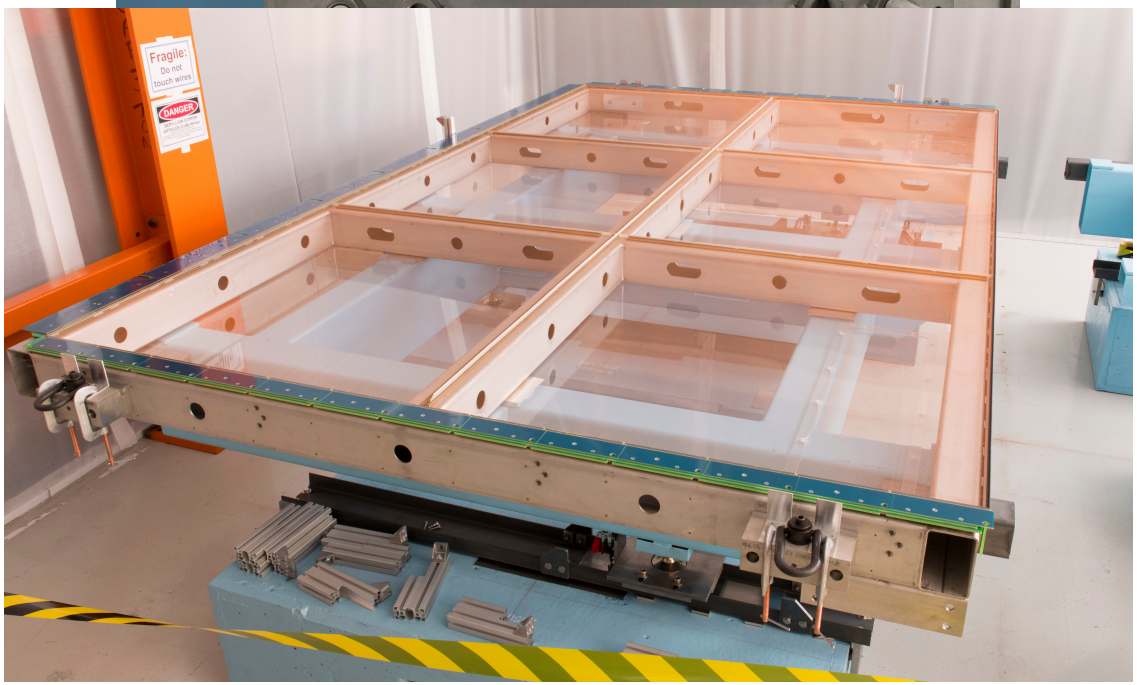
Production and Integration

- CE production
  - All FEMBs must pass 6 hour QA/QC tests
  - Half of all components have arrived at FNAL
- CE integration
  - Final integration test with FE and BE scheduled for June 18^{th} at Nevis Labs

Installing Cold Electronics to TPC

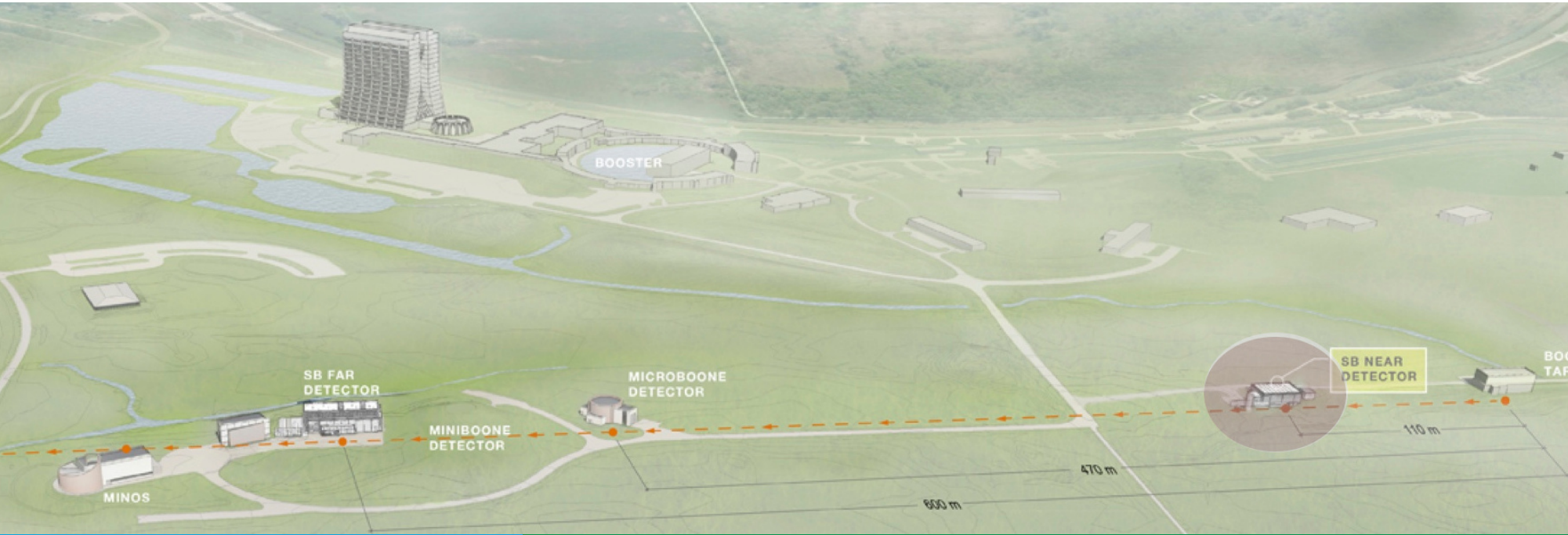
In the Detector Assembly Building





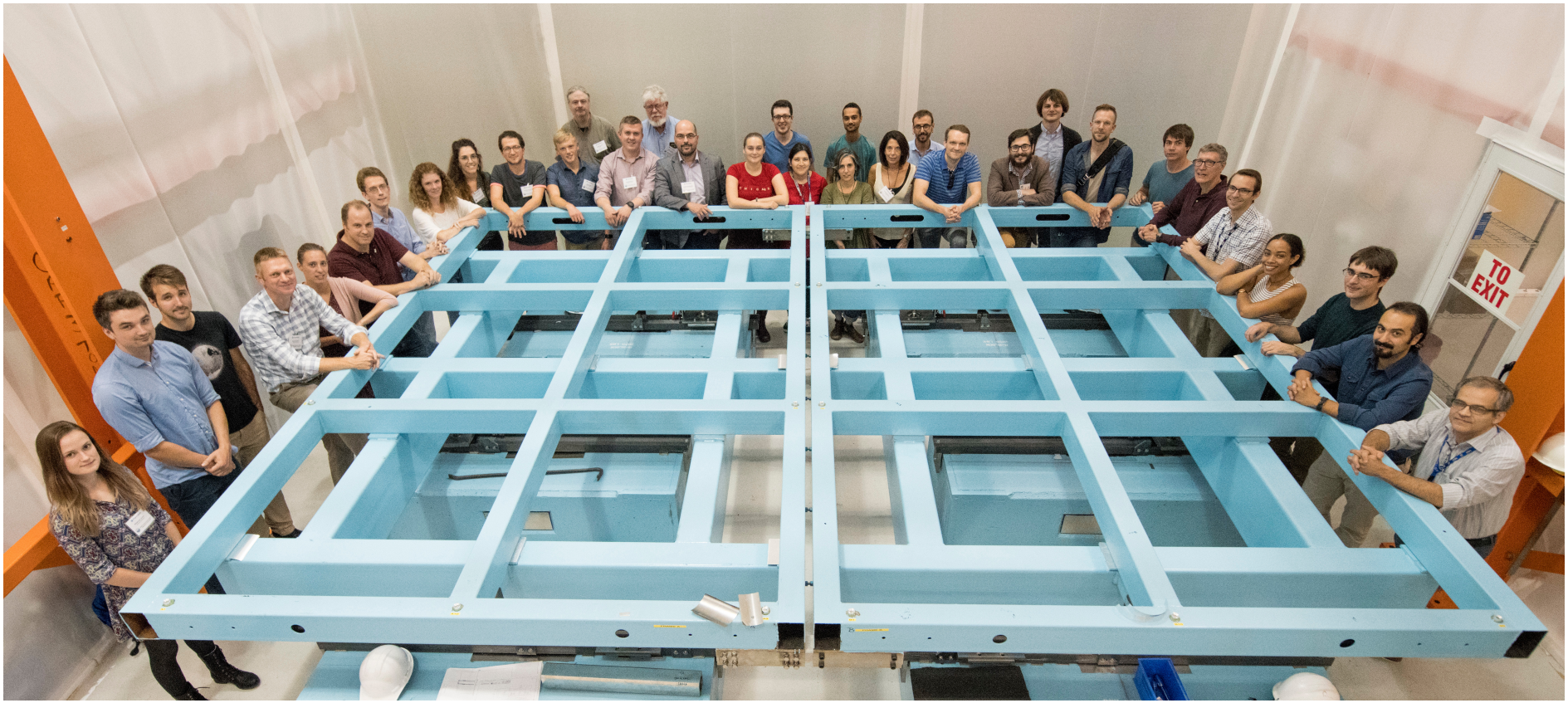
In Conclusion

- The SBND FE electronics are employing FE ASICs, COTS ADC ASICs, and FPGAs **in LAr** to improve the signal-to-noise ratio and simplify detector design
- R&D at SBND will greately benefit future LArTPC experiments, such as DUNE, as they might share similar components and production techniques



Thanks for Listening!

Questions?



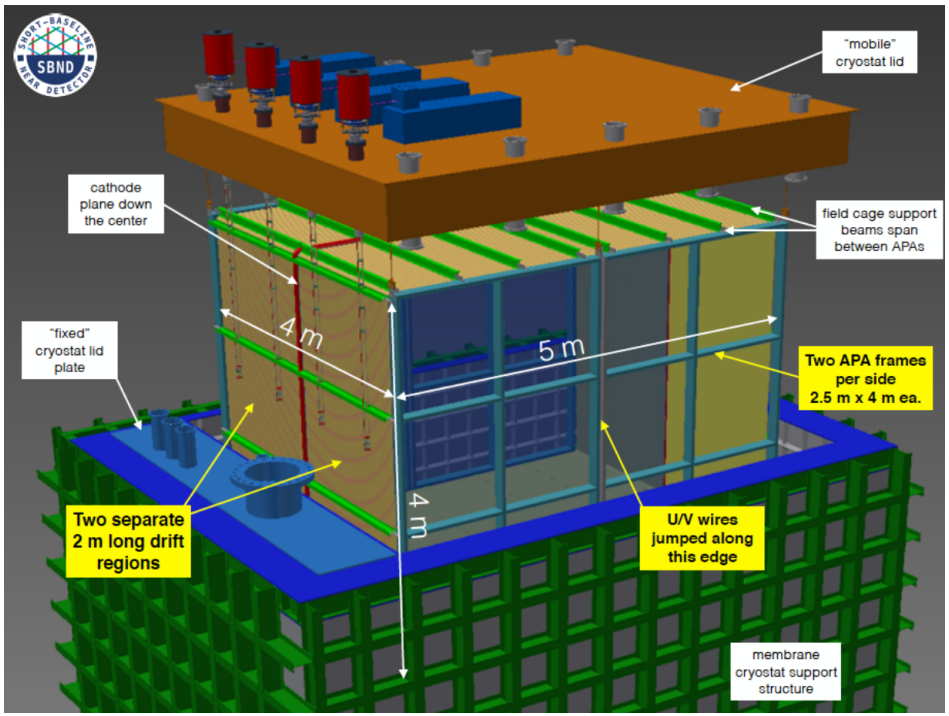
Backup

Slides

The Short-Baseline Near Detector

SBND

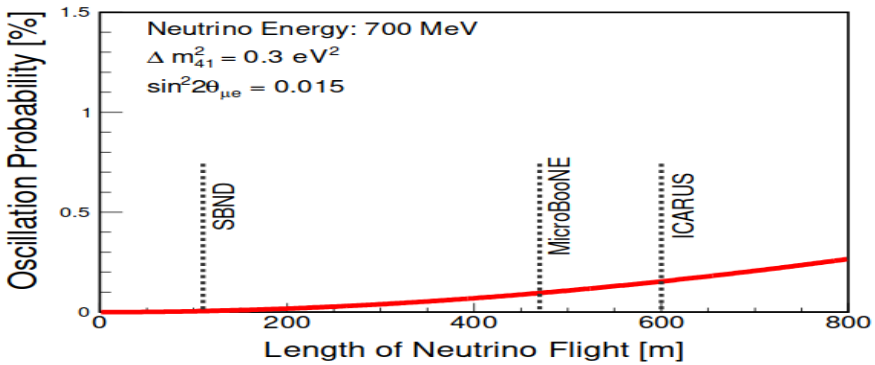
- A 112 ton liquid argon time projection chamber (LArTPC)
  - (4 x 4 x 5) m active volume
  - Two drift volumes
  - 3 wire planes: 0, $\pm 60°$
    - ★ 3 mm wire pitch
    - ★ 11,264 total wires
- 110 m downstream from the Booster Neutrino Beam (BNB) target at Fermilab
  - 8 GeV protons on a beryllium target
- Detector is under construction

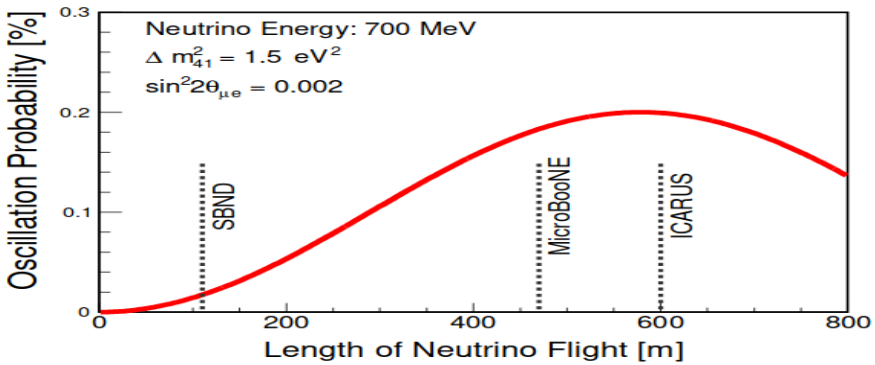


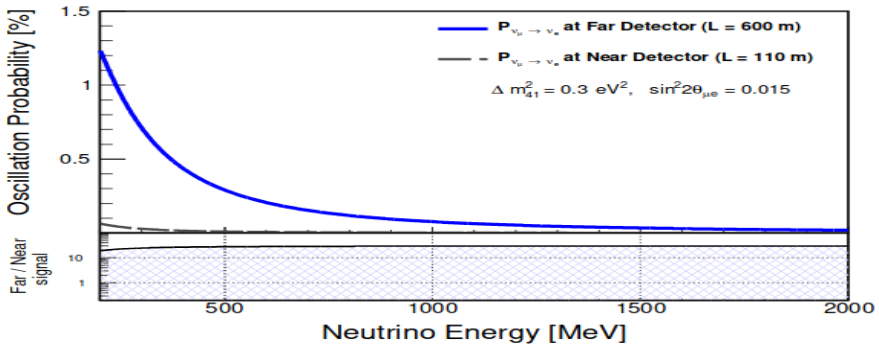
Physics

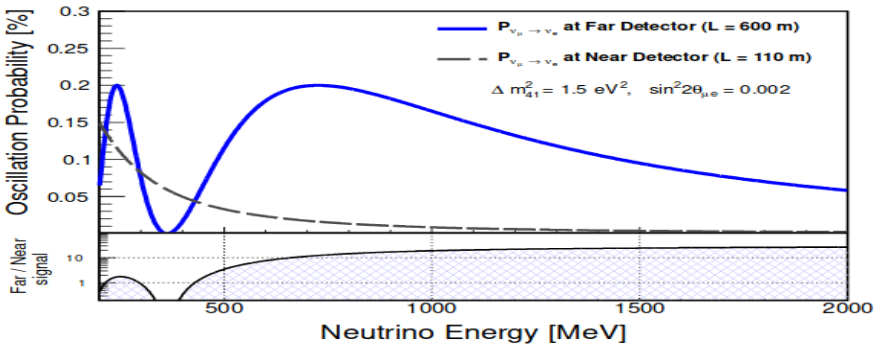
Physics goals of SBN

- Oscillation searches
  - World-leading $\sim$1 ev sterile neutrino sensitivity
  - ν_e appearance and ν_μ disappearance channels
- High statistics cross section studies
- Testing beyond the Standard Model theories









Machado, Pedro AN, Ornella Palamara, and David W. Schmitz. "The Short-Baseline Neutrino Program at Fermilab." arXiv preprint arXiv:1903.04608 (2019).

Warm Interface Electronics

WIECs and WIBs

- Warm interface electronics crate (WIEC) installed on each flange and contains the following
  - Six WIBs (each can control up to 4 x 128 channels)
  - One Power and timing backplane (PTB)
  - One Power and timing card (PTC)
- WIECs are the interface between FE and BE electronics
  - Convert signal to optical
  - Timing, control, and monitoring functionality