

CALICE-style ND ECAL

Detector Concept Status & R&D Questions

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Outline

- Global detector layout
- Main performance goals
- Technology choices & options
- Cost Drivers
- R&D plans

The Global Layout

Driven by the Dimensions of the HPgTPC

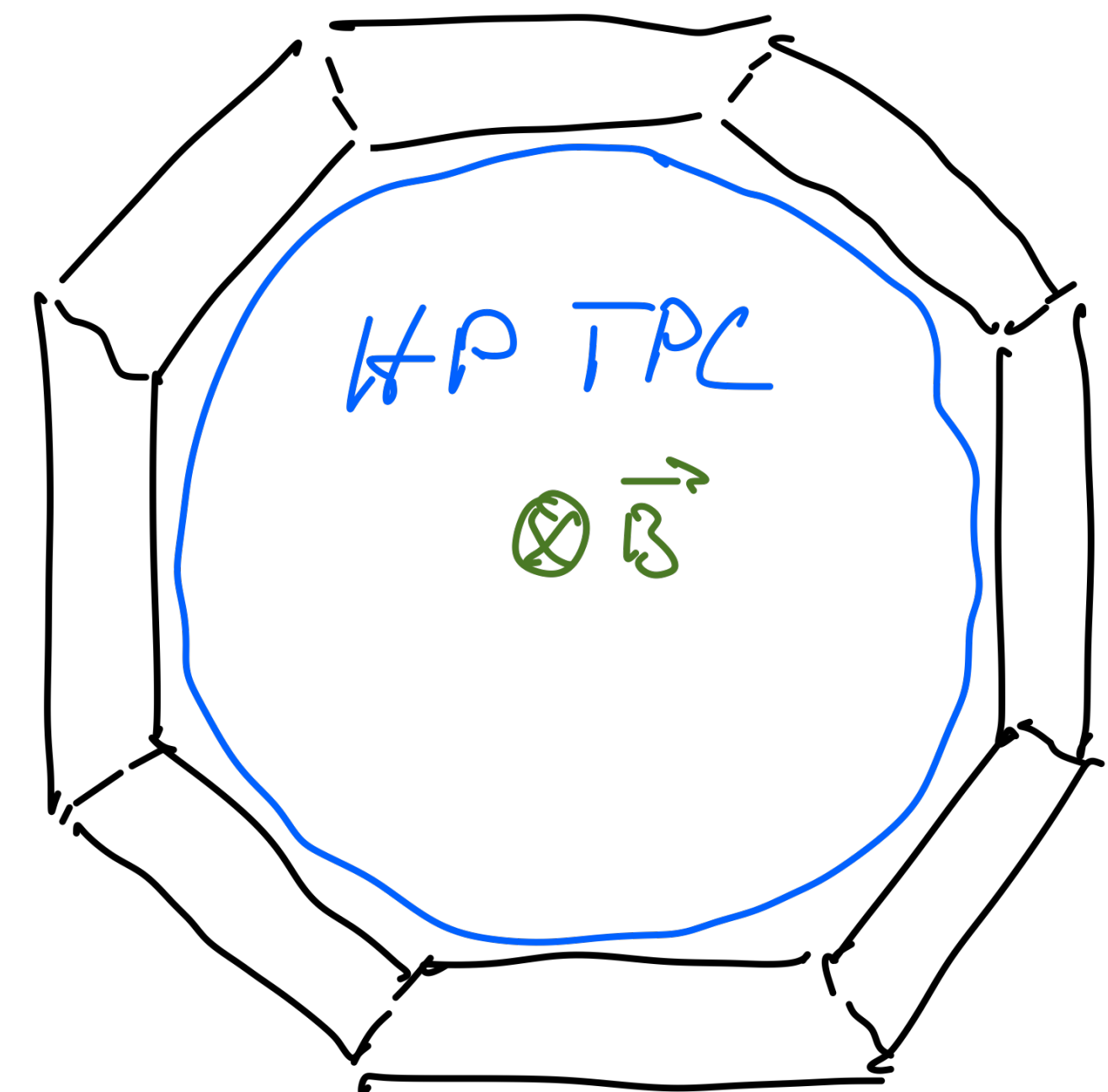
- *Dimensions* of the HPTPC fiducial volume
 - Radius: 2.7 m
 - Length: 5.5 m
- Need a calorimeter geometry that fits the intrinsically planar geometry of the highly granular sampling structures, and matches the cylindrical HPTPC structure & pressure vessel:
An octagonal structure

Dimensions:

- Octagon side length: 2.25 m
- Barrel inner surface: $\sim 100 \text{ m}^2$
- Cap inner surface: $\sim 50 \text{ m}^2$

Magnetic field:

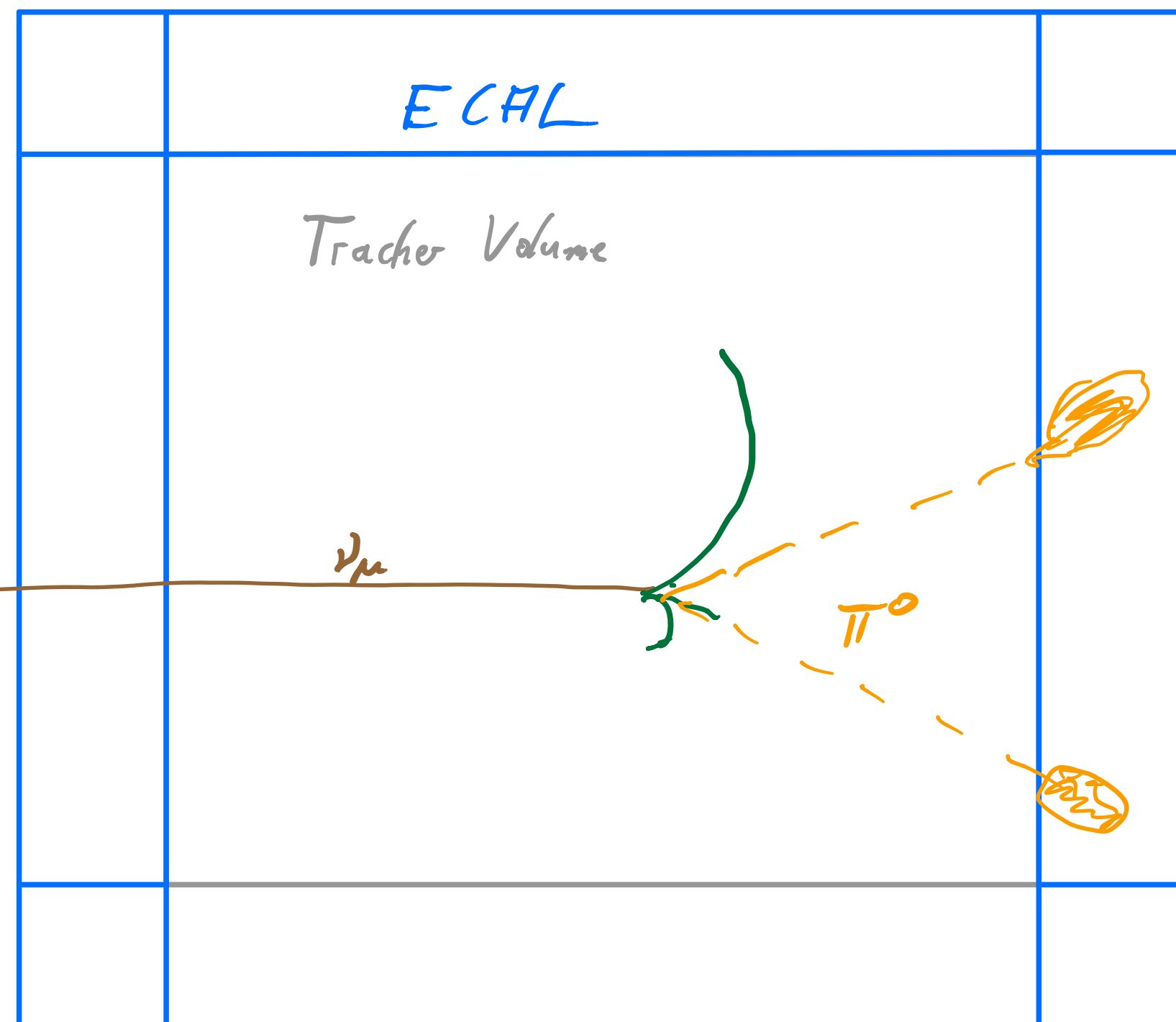
- parallel to drift direction (= cylinder axis)
- perpendicular to beam direction



Main Performance Goals

Must-haves, ideas & aspirations

- Electromagnetic resolution: 6 %- 8% / \sqrt{E} [GeV]
 - Drives sampling structure: Thin absorbers!
- π^0 reconstruction: Requires shower separation, position and angular resolution
 - Motivates highly granular readout

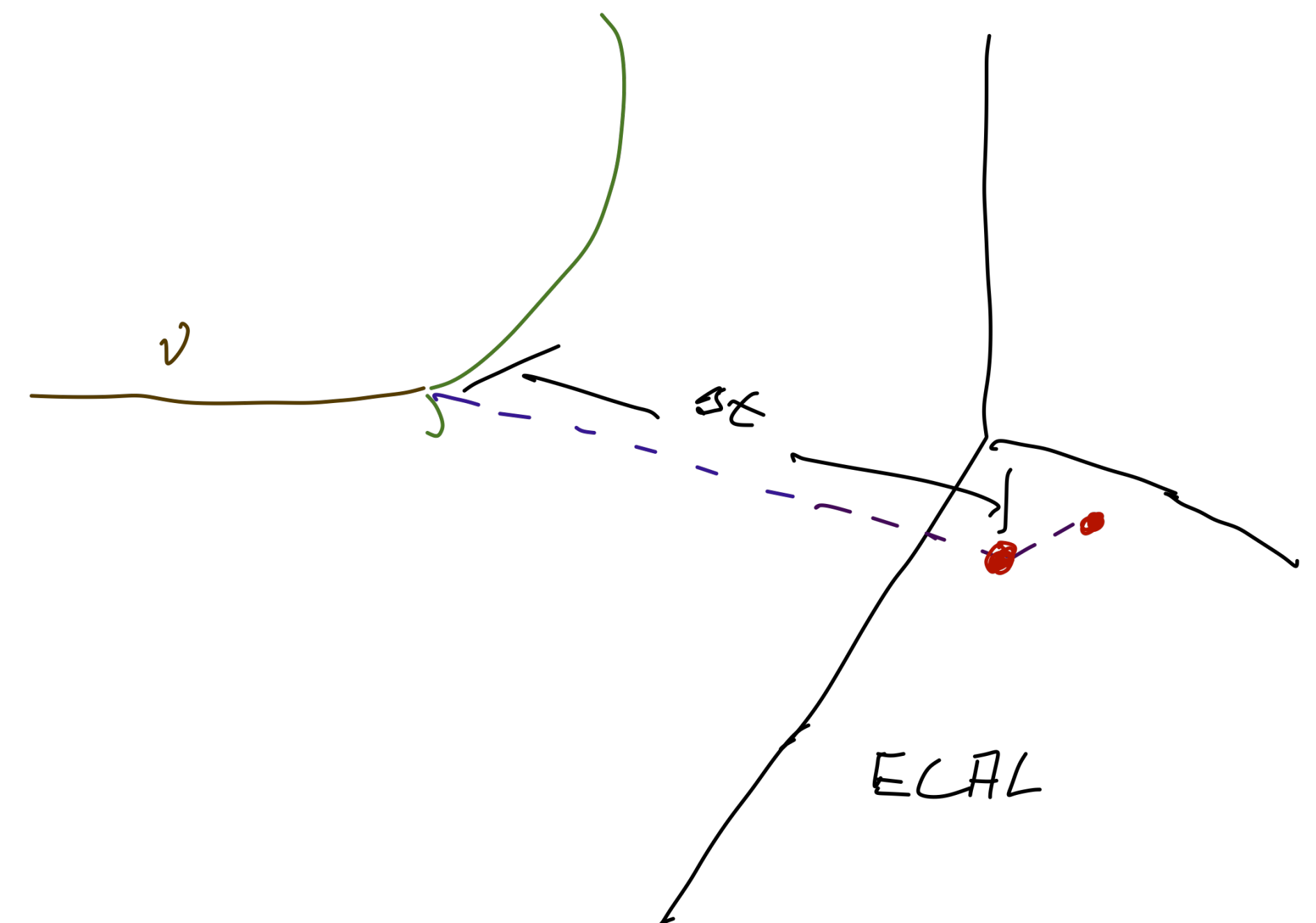
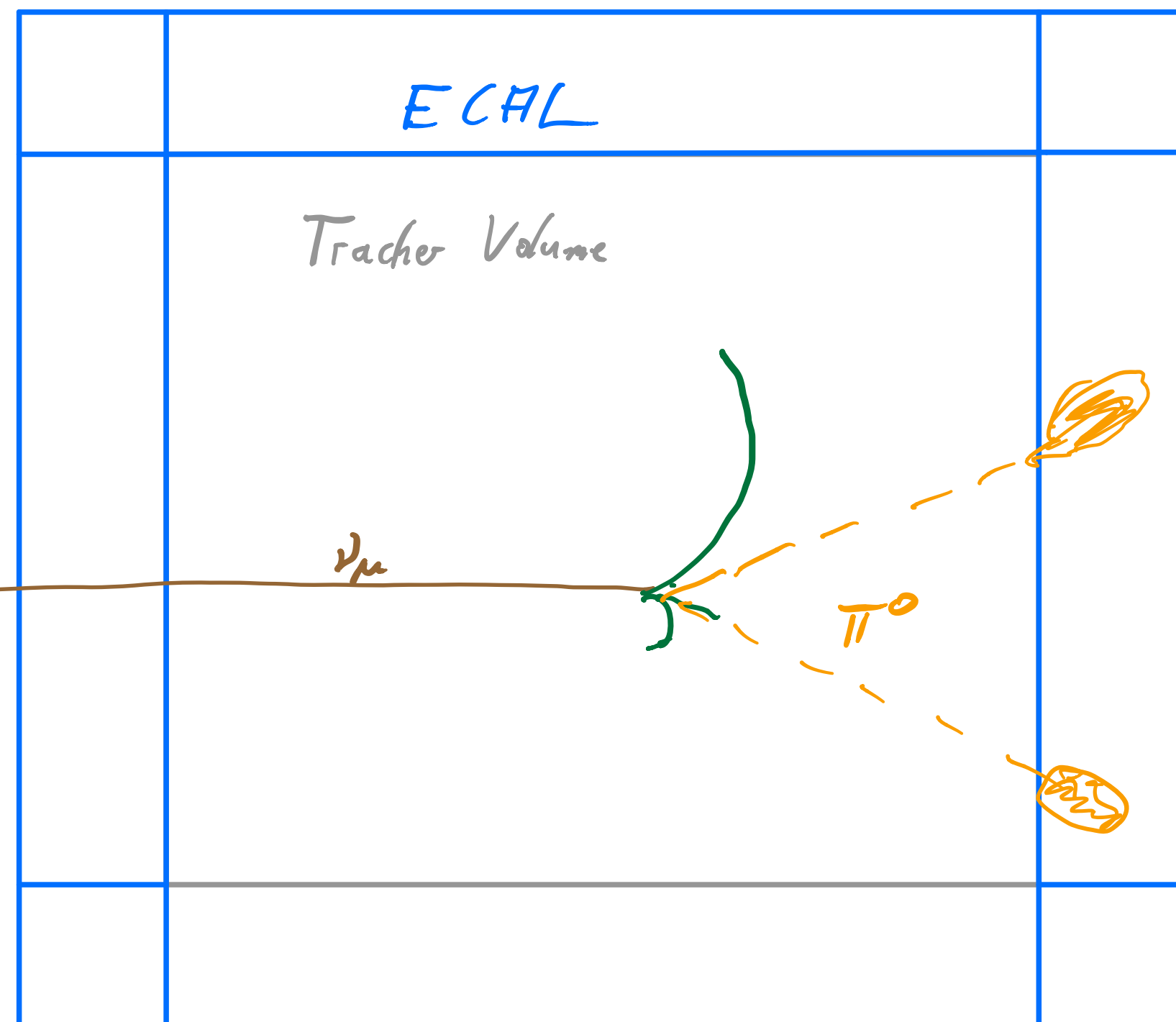


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- Neutron reconstruction - a potential game-changer [still needs to be established in realistic environments!]
 - Requires timing on the few 100 ps level to enable energy measurement via time-of-flight



Refining the Design

Accounting for environment and constraints

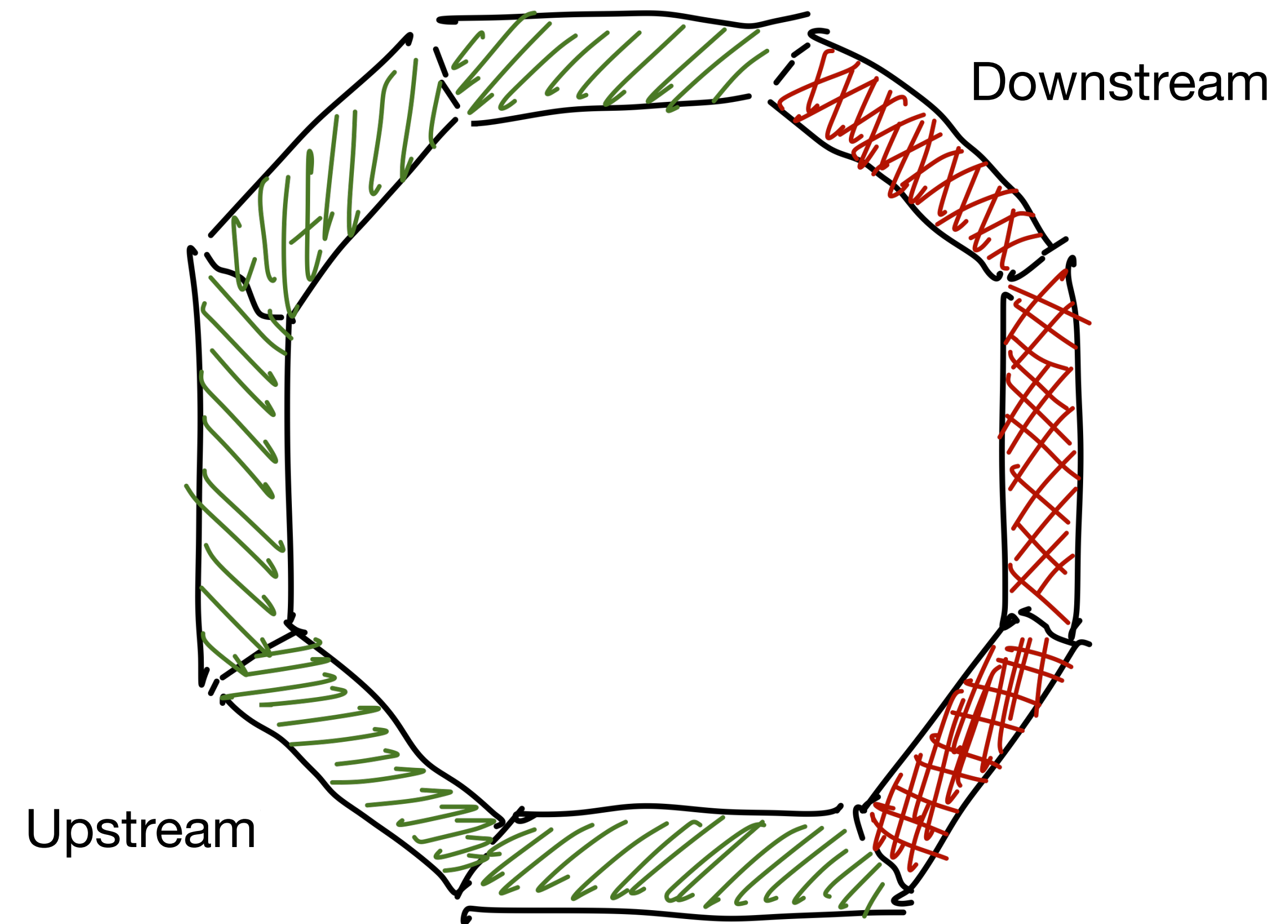
- Things tend to go forward - do not need the same granularity, and same depth / resolution everywhere
- Obviously something that requires understanding and optimisation - in progress

Defining two regions:

- DownStream (DS): Forward Region
- UpStream (US): Side & backward region (including caps)

Possibly variable longitudinal segmentation:

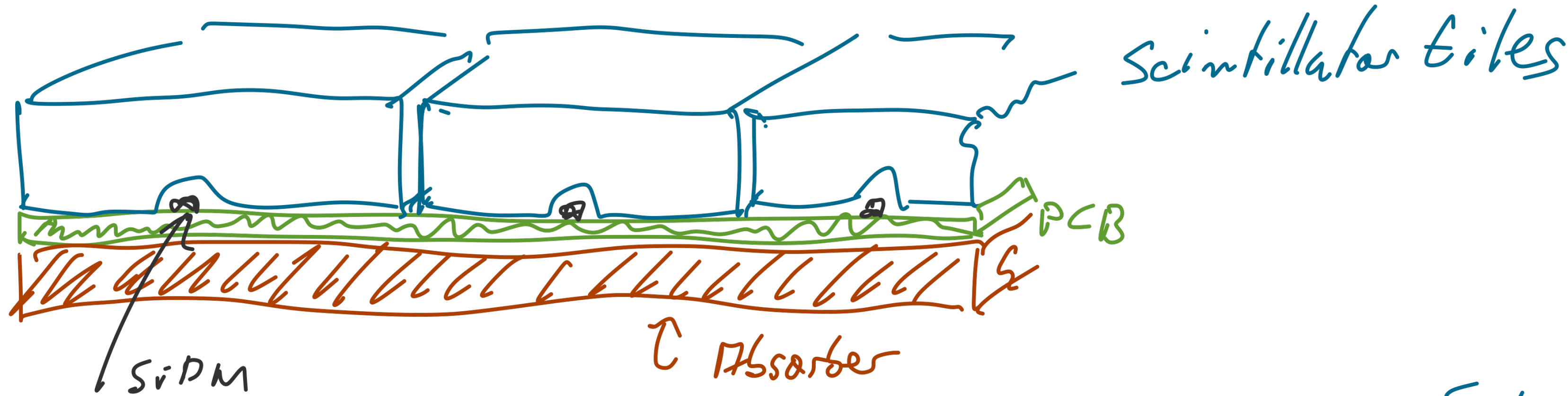
- thin layers in front to enable good energy resolution for low-energy photons
- thicker layers in the rear to ensure sufficient containment with a compact detector



Technology Choices & Options: Baseline

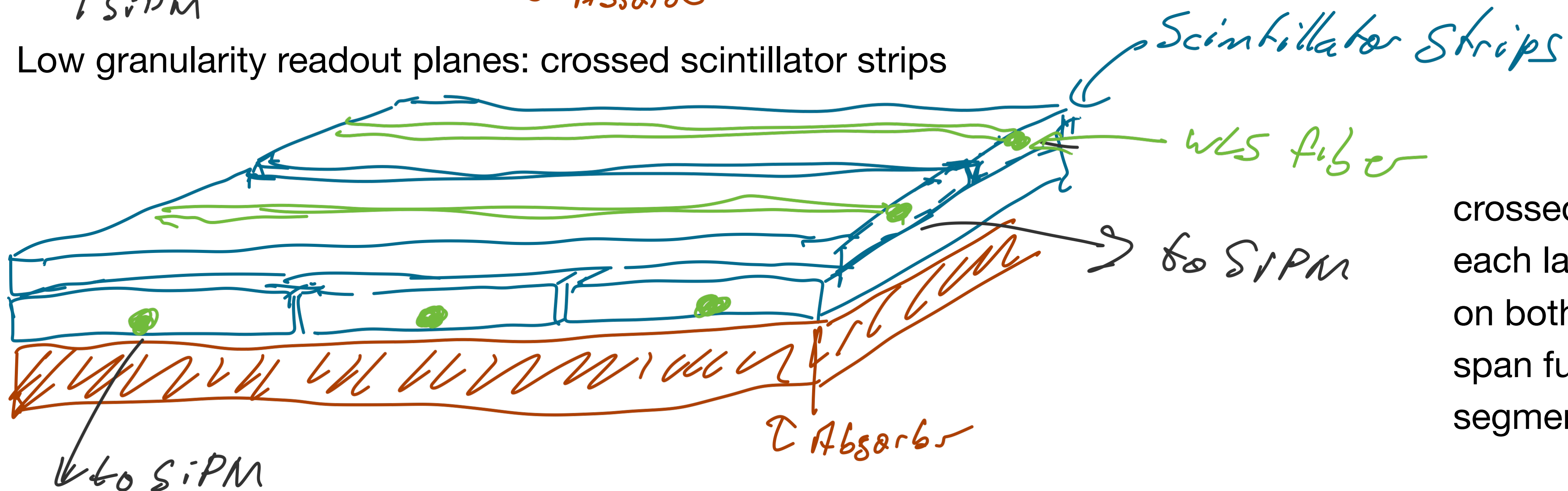
(Partially) based on CALICE AHCAL

- High granularity readout planes: scintillator tiles



one SiPM per tile

- Low granularity readout planes: crossed scintillator strips




crossed strips in each layer, read out on both sides (strips span full length of segment)

The Current Detector Model

What is in the Document - not what will get built

“Upstream” segment

 low granularity layers: alternating orthogonal bars

 high granularity layers: tiles

“Downstream” segment

- Downstream layout [3 downstream octagon segments]:
 - 80 layers, first 8 high granularity
- Upstream layout [5 side and upstream segments, endcaps]:
 - 60 layers, first 6 high granularity

Active elements:

- *high granularity*: 25 x 25 mm² tiles, 5 mm thick
- *low granularity*: 40 mm wide, 5 mm thick bars over full module length, crossed in alternating layers

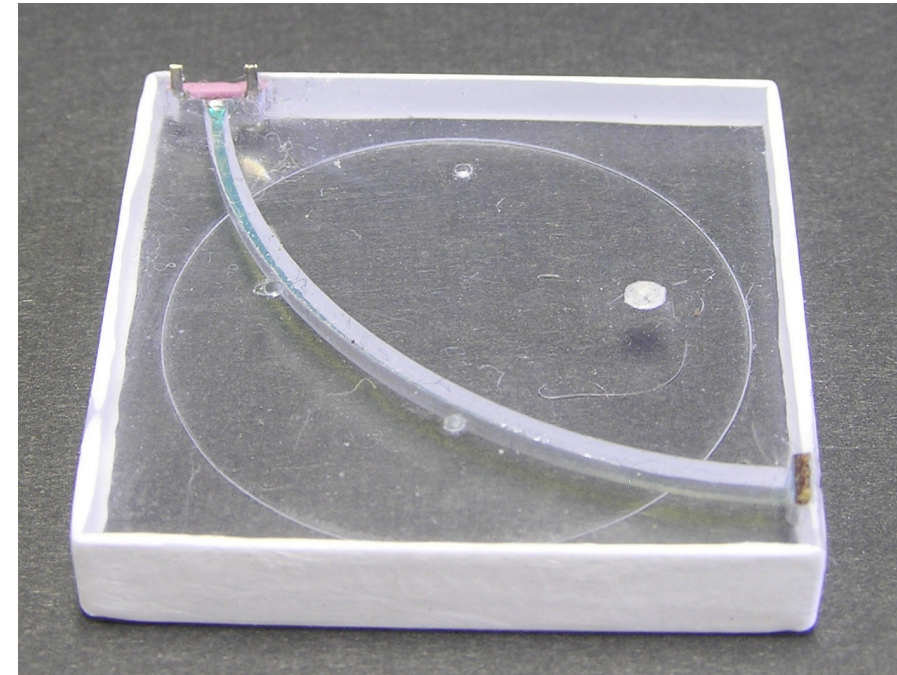
SiPM-on-Tile Technology

A closer look



- From the first large-scale application of SiPMs to the “**SiPM-on-tile**” technology

2008 - 2016



Physics Prototype

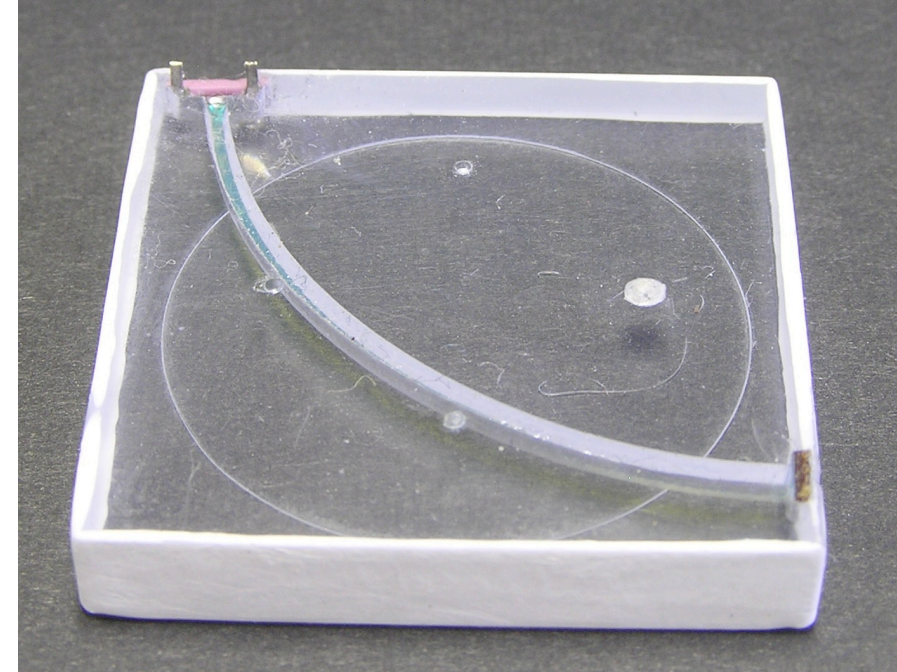
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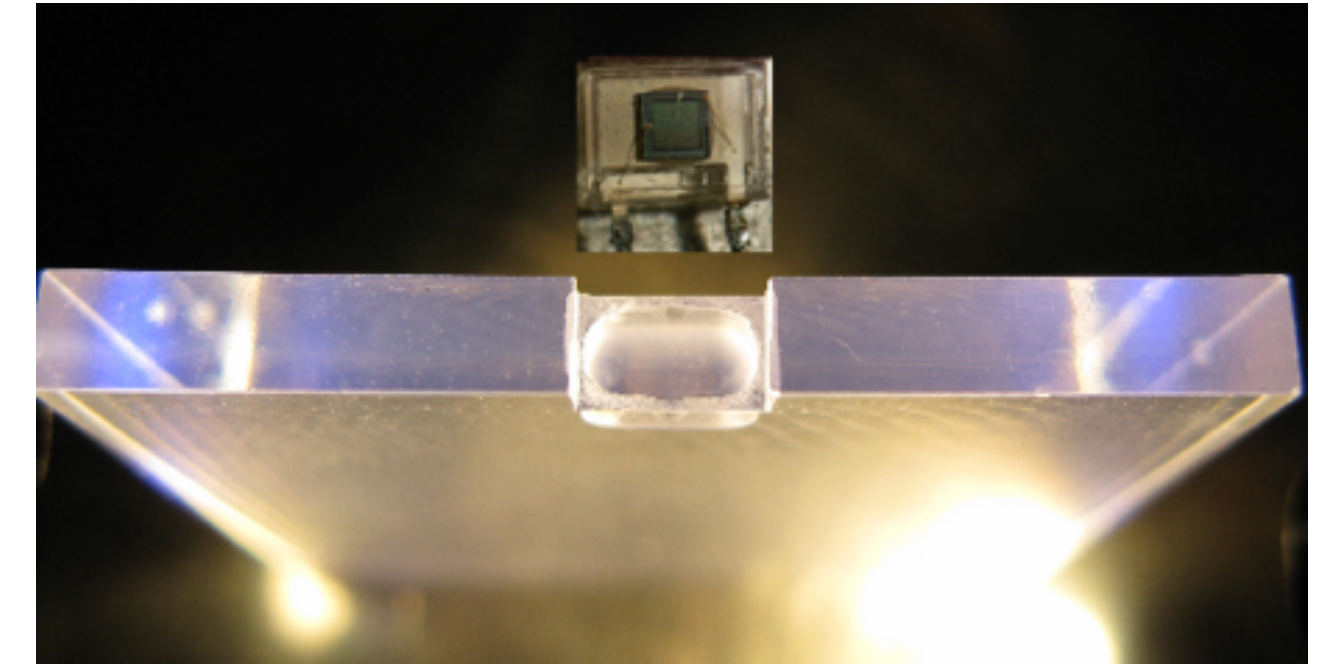


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Direct coupling of tiles
and photon sensors

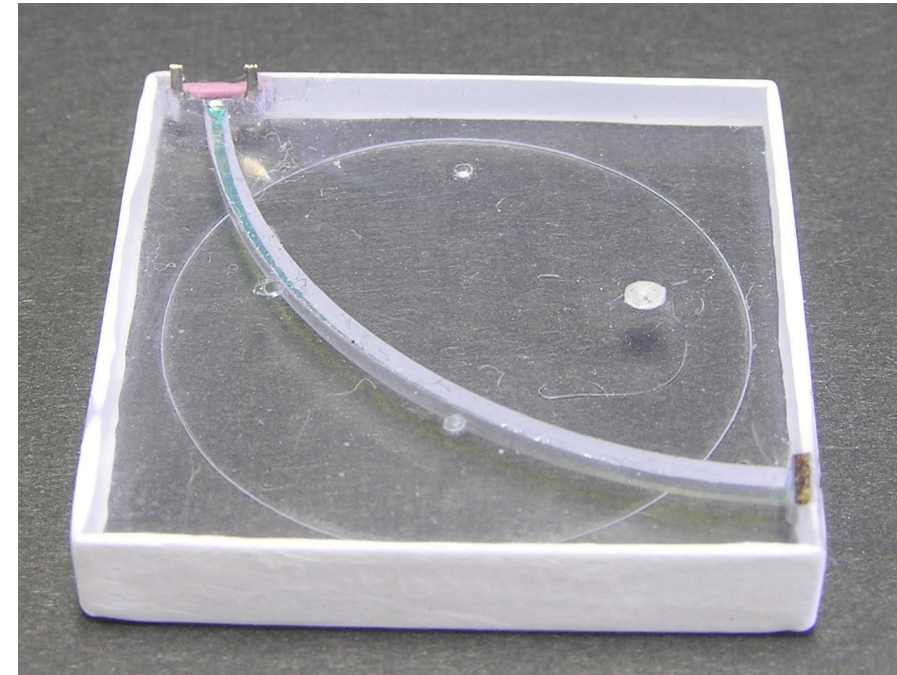
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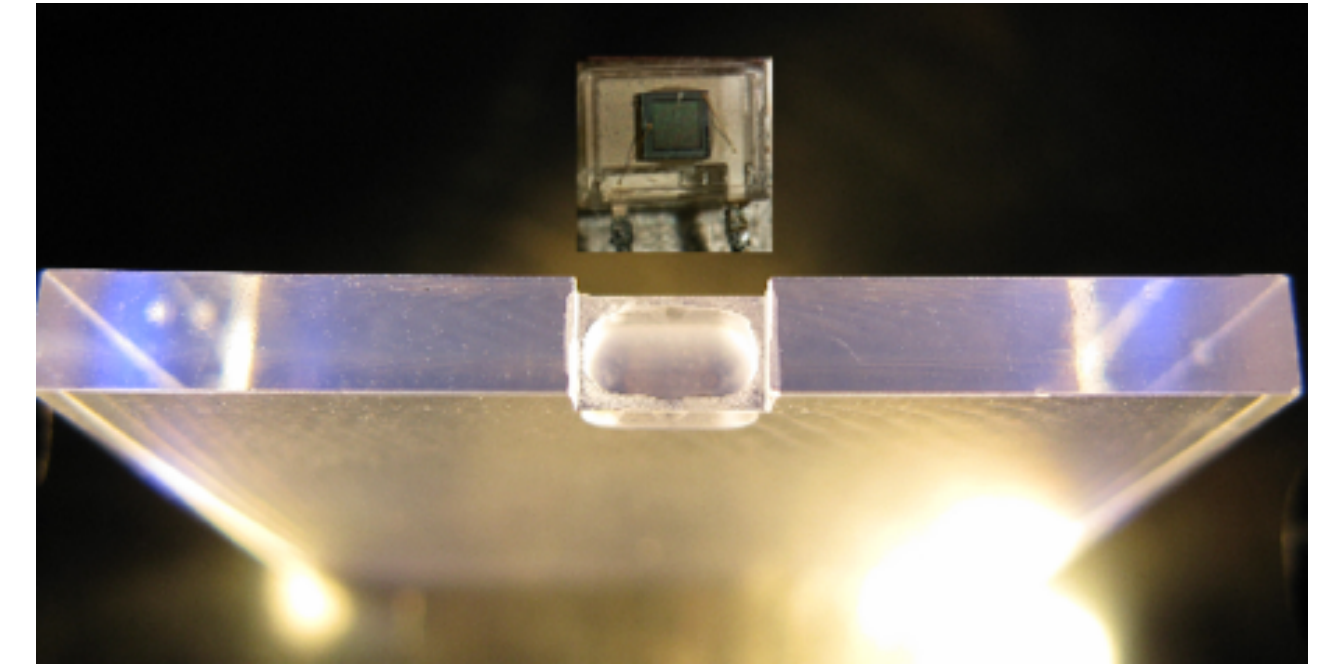


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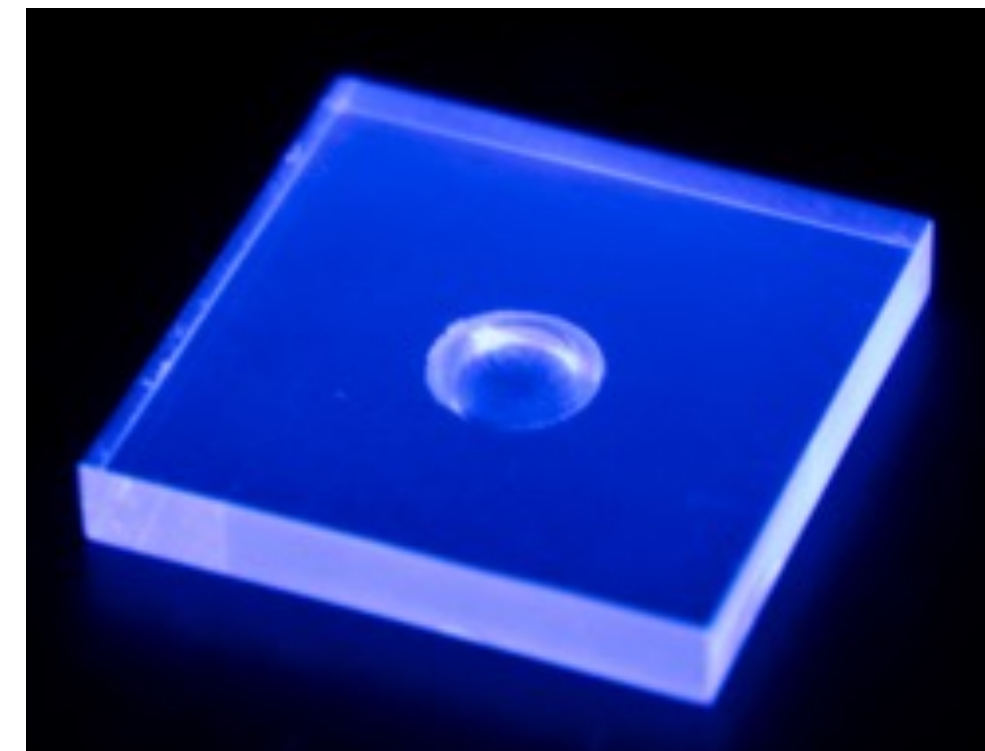
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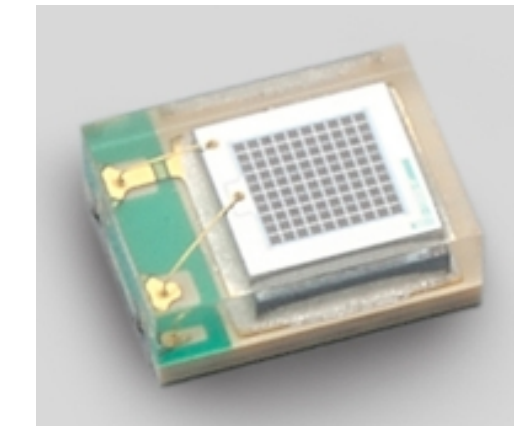
Physics Prototype



Direct coupling of tiles and photon sensors



SMD SiPMs, modification of direct coupling



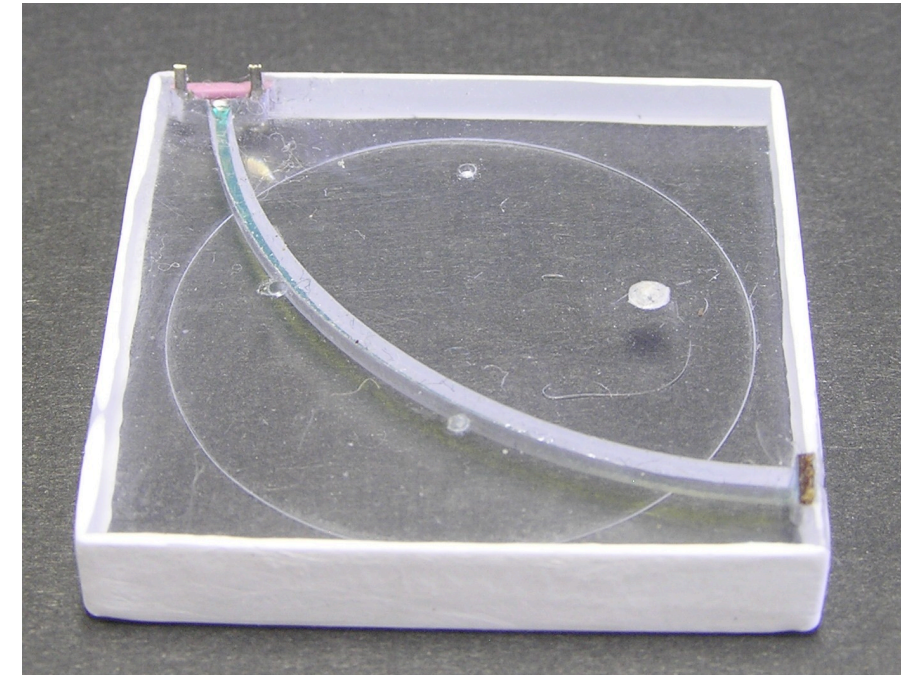
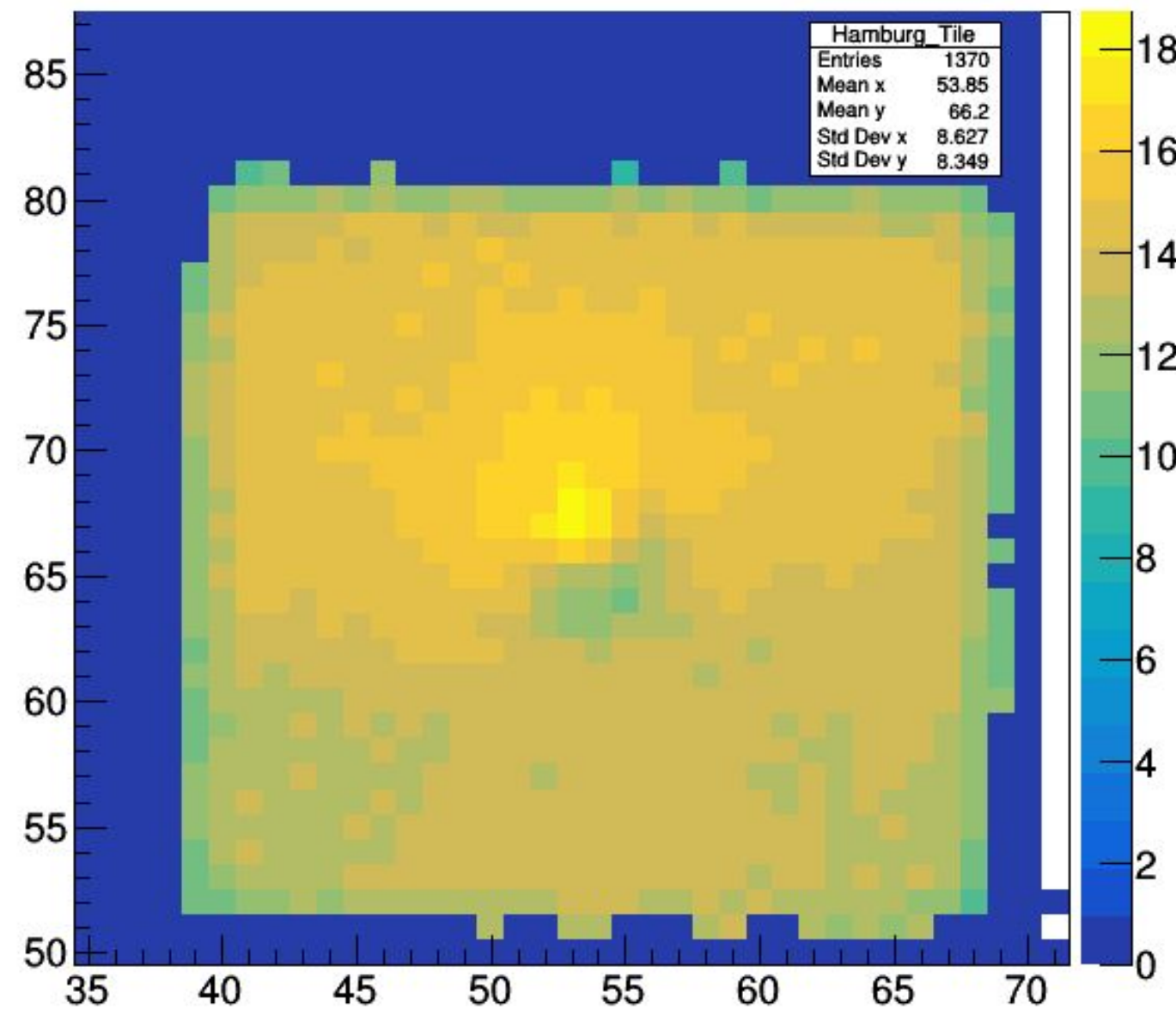
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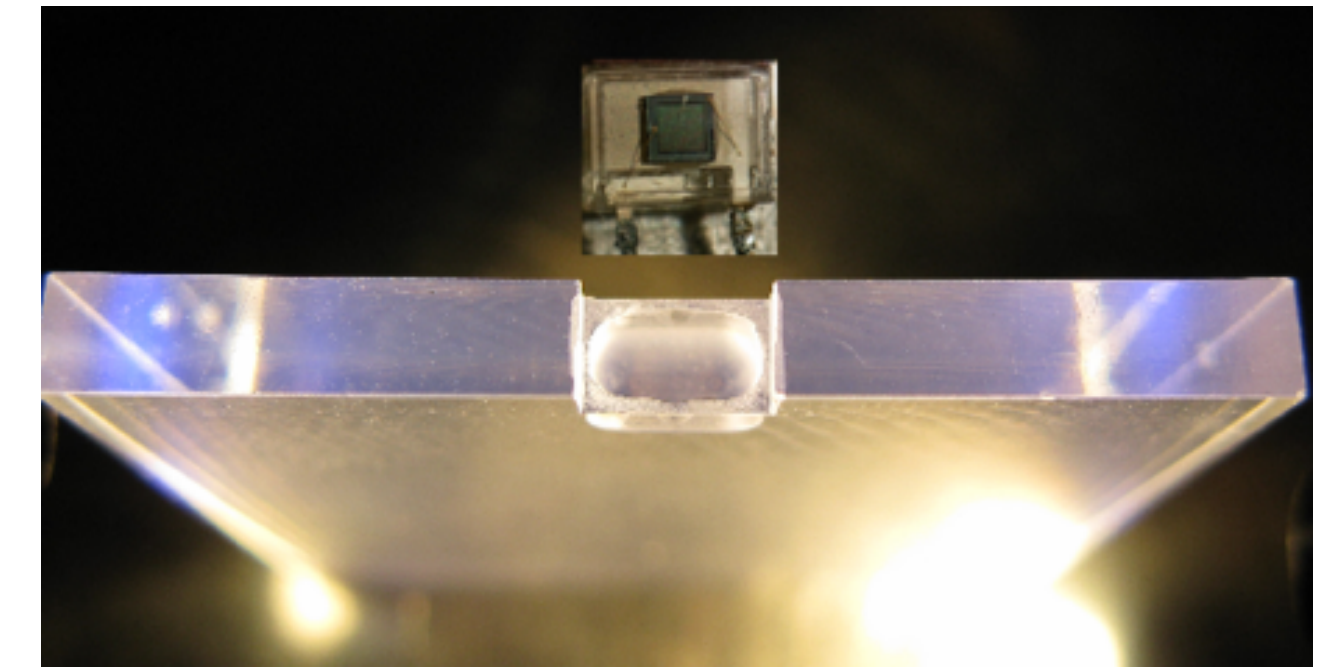


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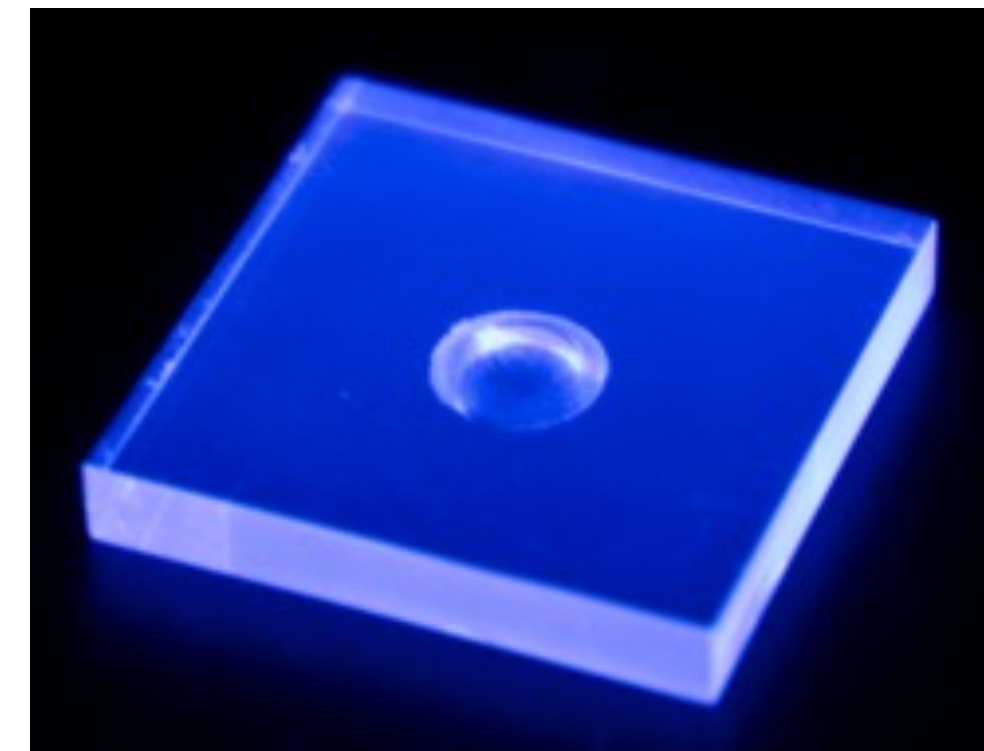
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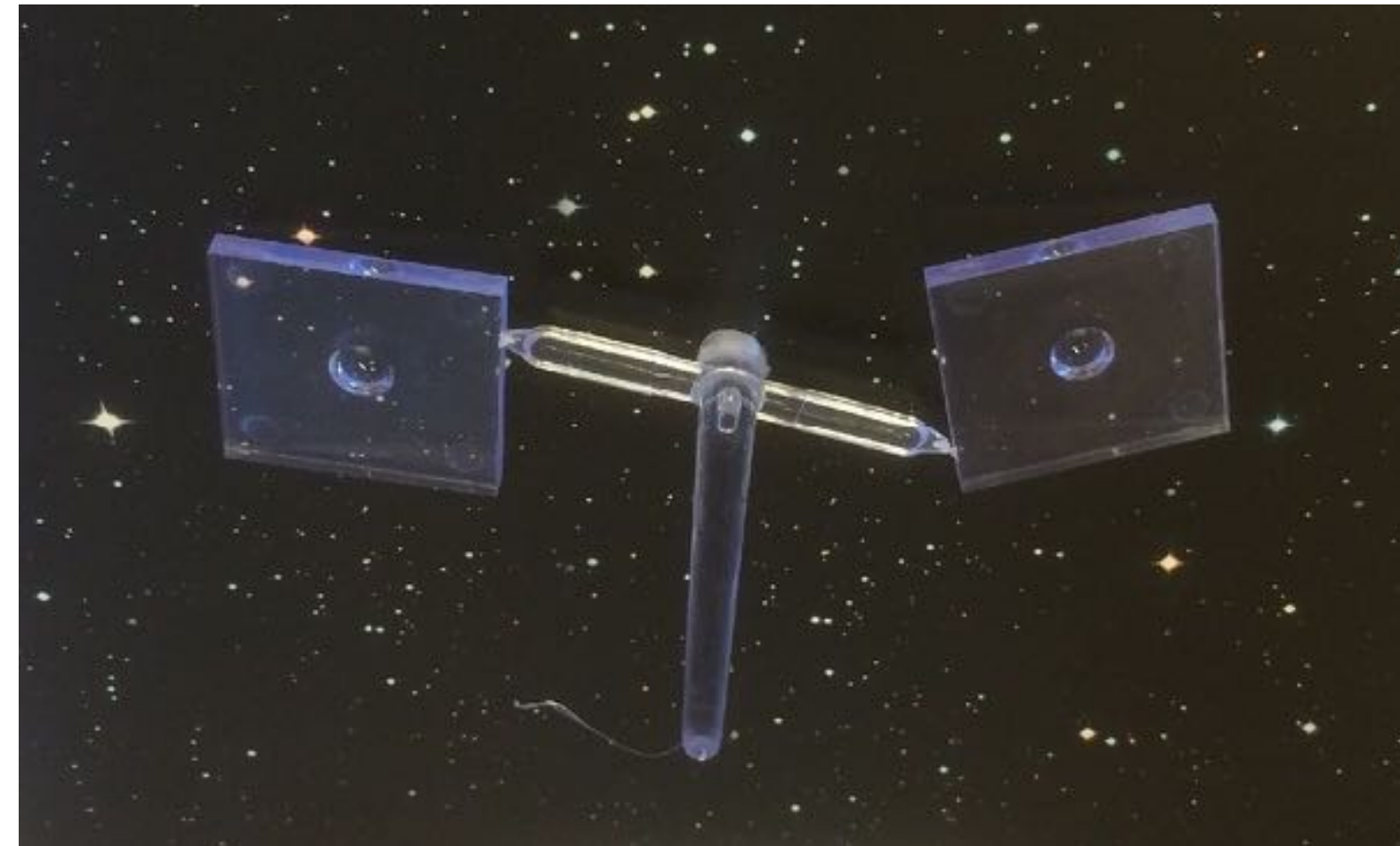
verification of tile performance in the lab

SiPM-on-Tile Technology

A closer look



- Mass production for a new 0.5 m³, 22k channel prototype
 - 24k tiles produced & wrapped

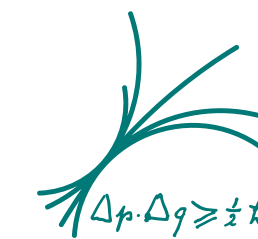


injection molding
of PS based
scintillator tiles

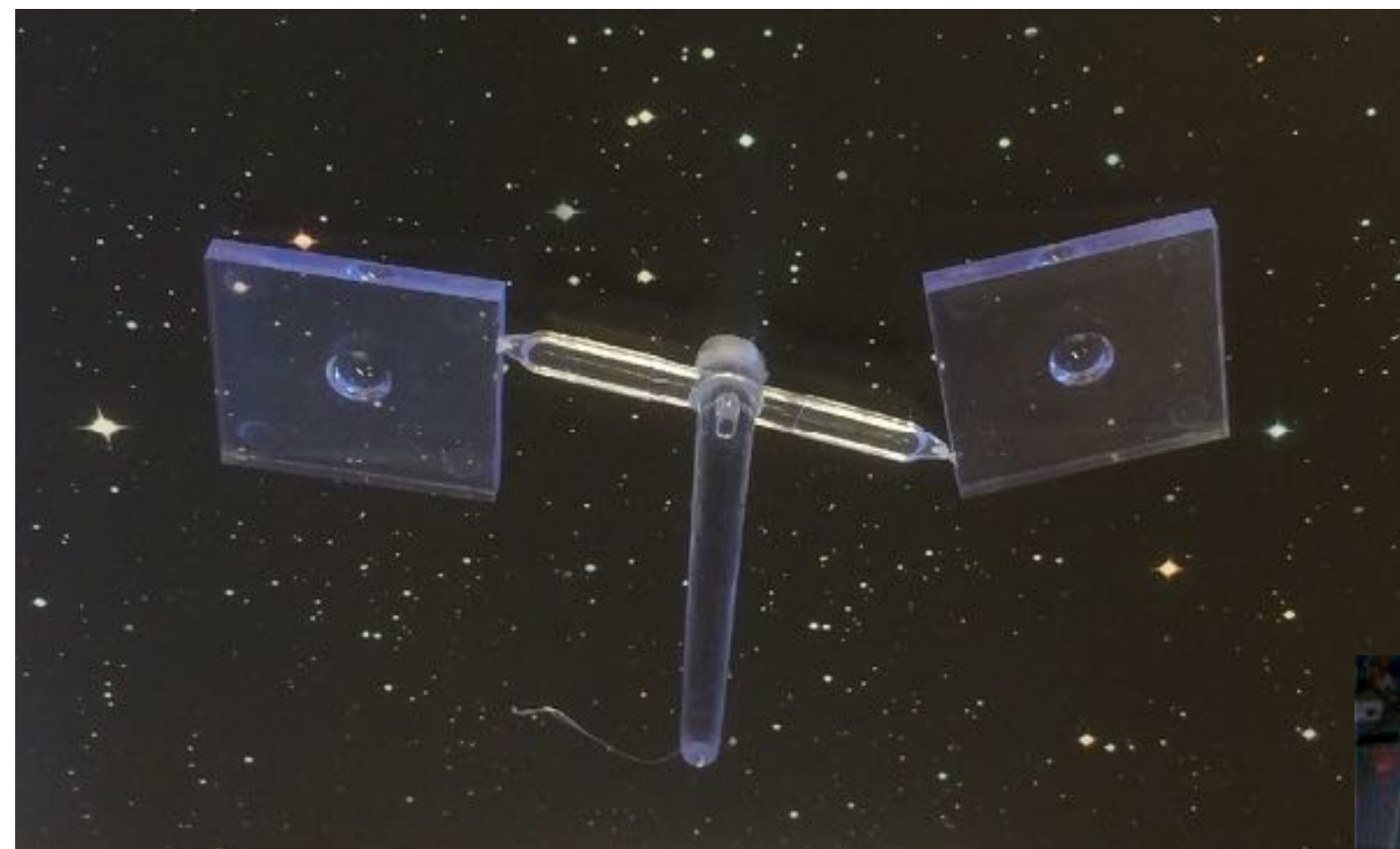
09/2017

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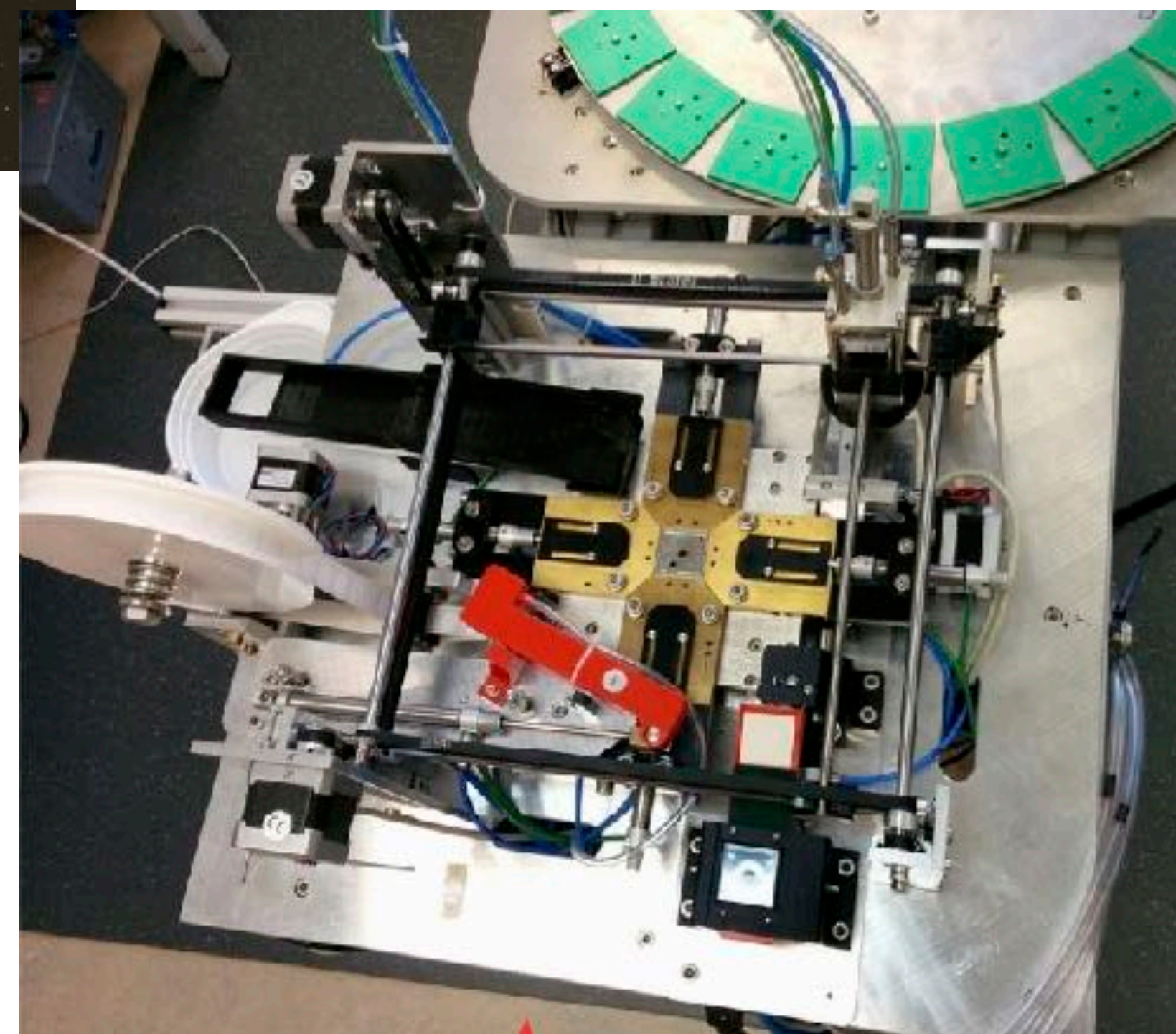
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09/2017



10/2017 - 01/2018

semi-automatic wrapping
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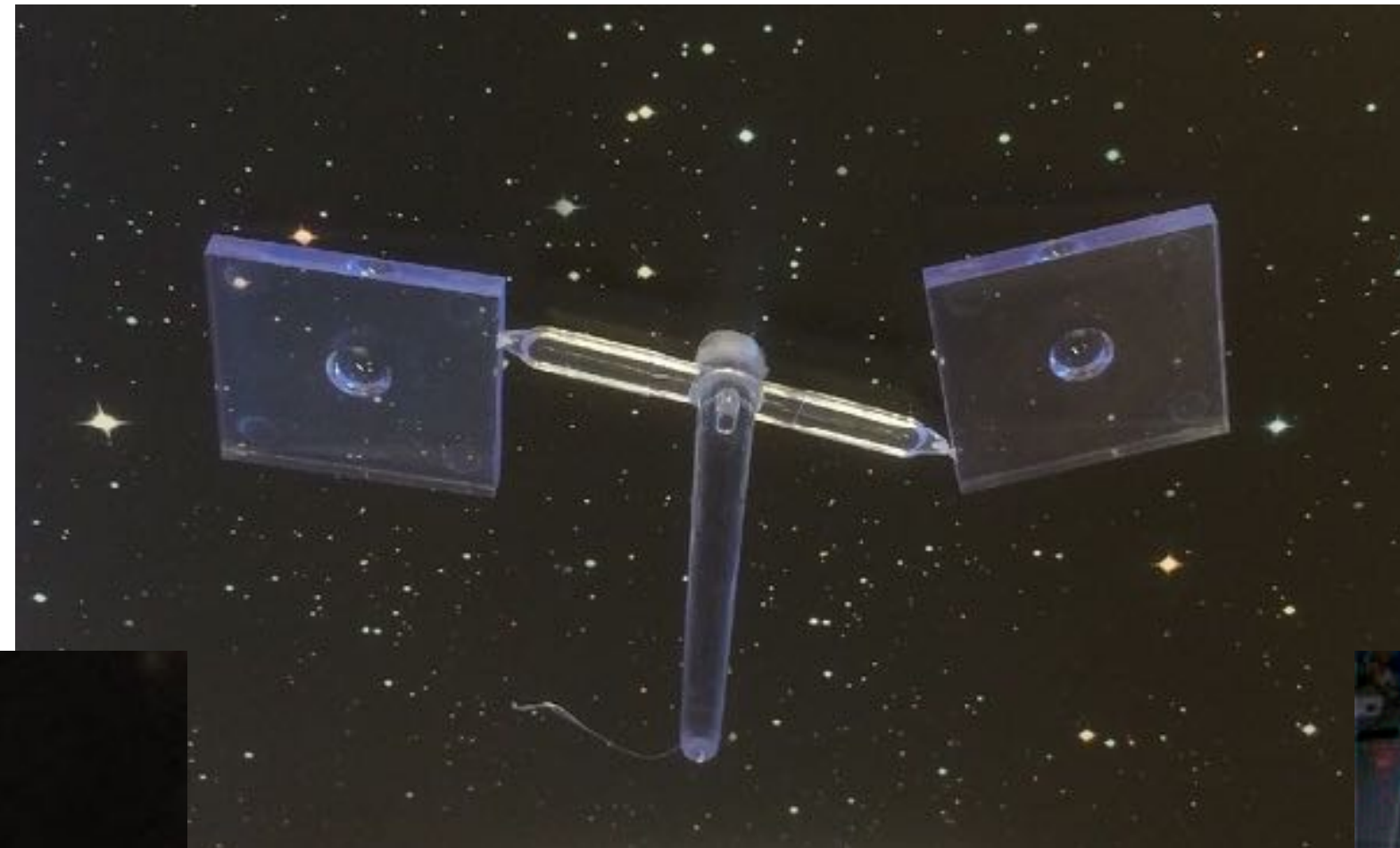


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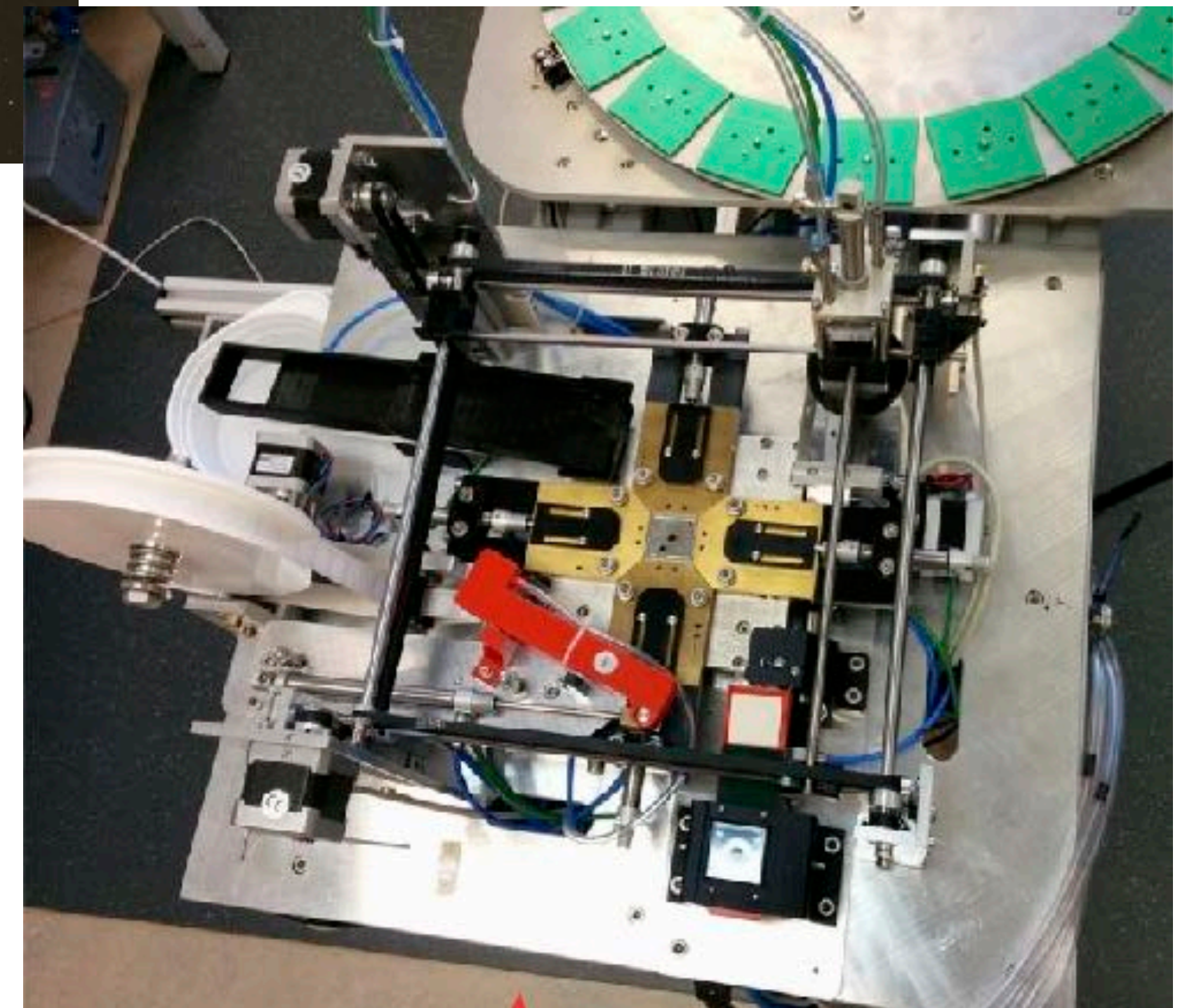
automatic placement of tiles on electronics board (HBU), fully assembled with SiPMs and ASICs

11/2017 - 02/2018



10/2017 - 01/2018

semi-automatic wrapping
of scintillator tiles

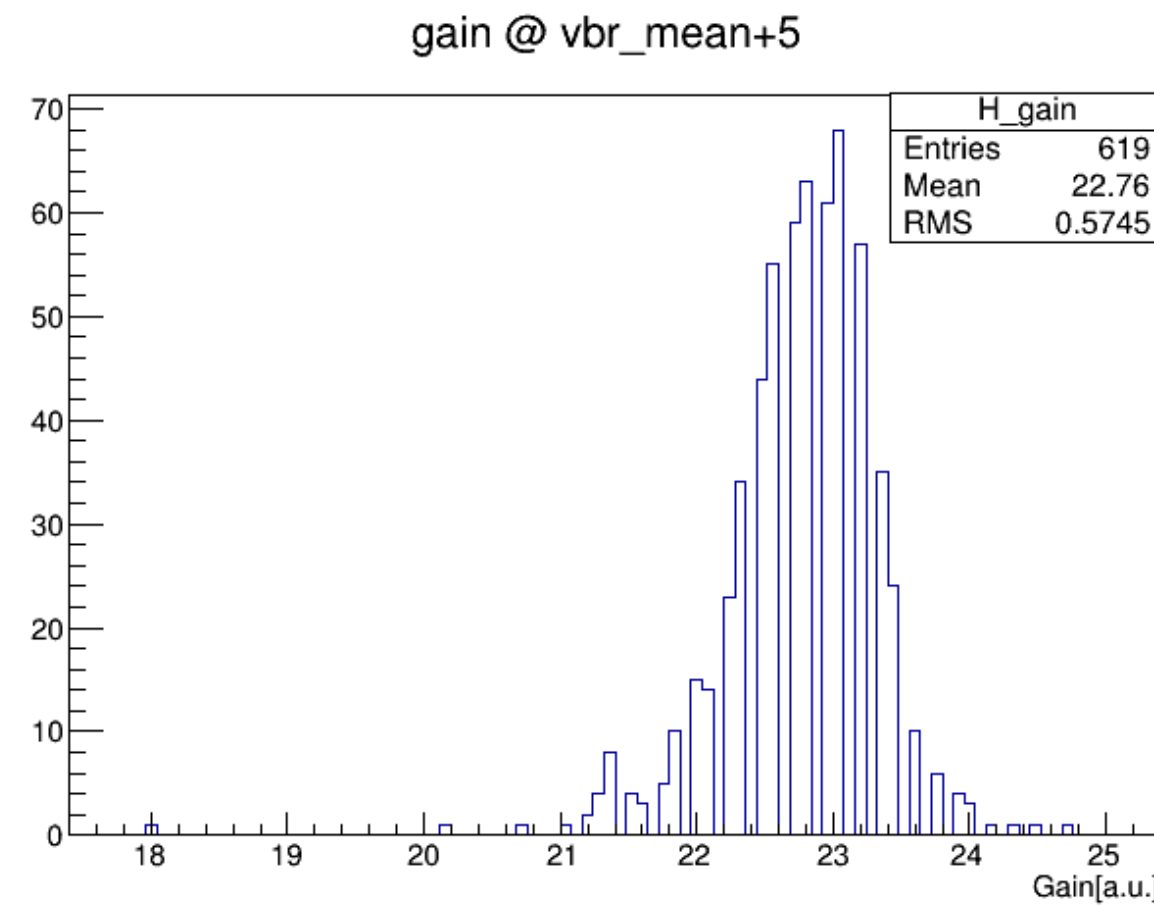


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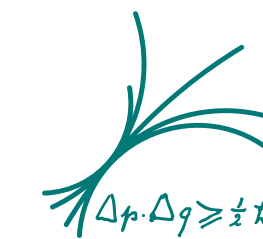
- A multi-step QA procedure



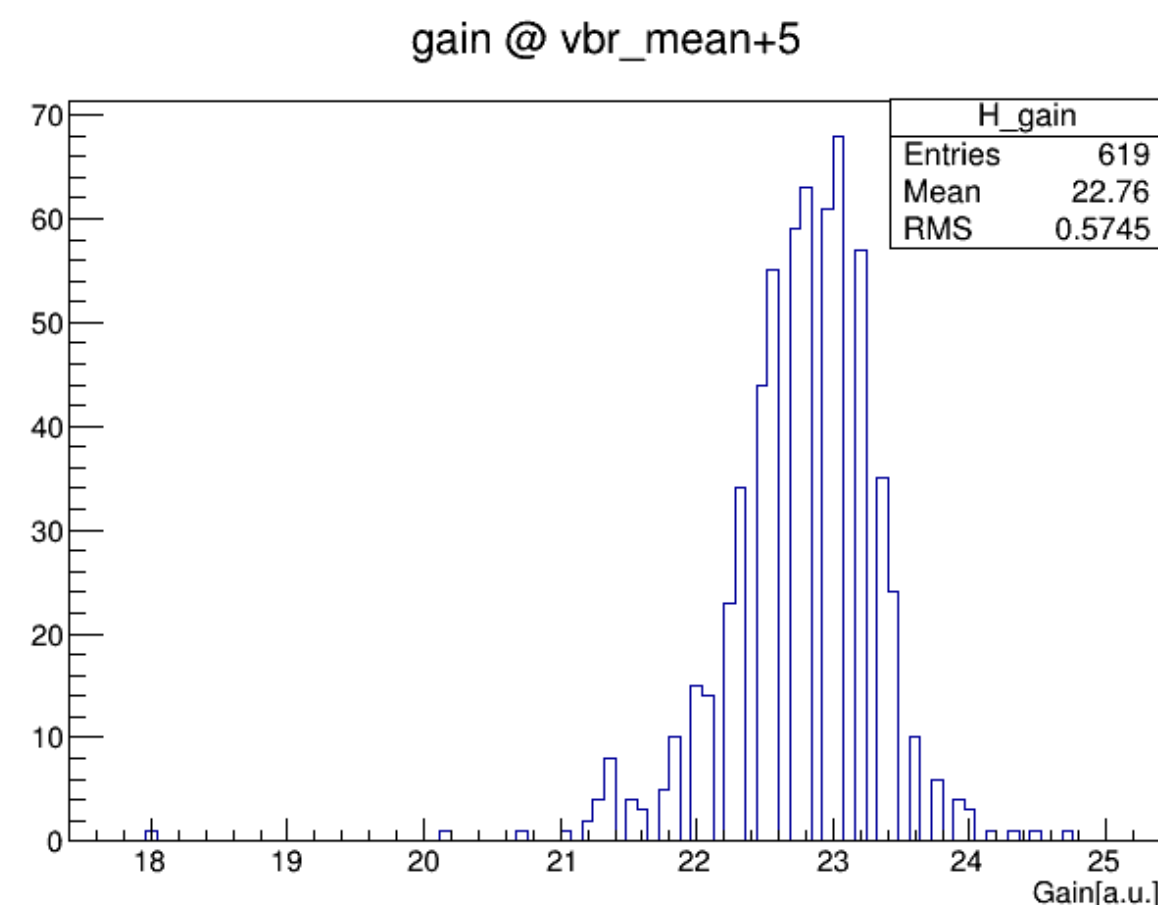
spot testing of few % of 22k SiPMs,
acceptance of 600 pc batches
according to pre-defined criteria -
all batches accepted

SiPM-on-Tile Technology

A closer look



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test of all ASICs (~80-90% yield)
test of all assembled boards using
built-in LEDs

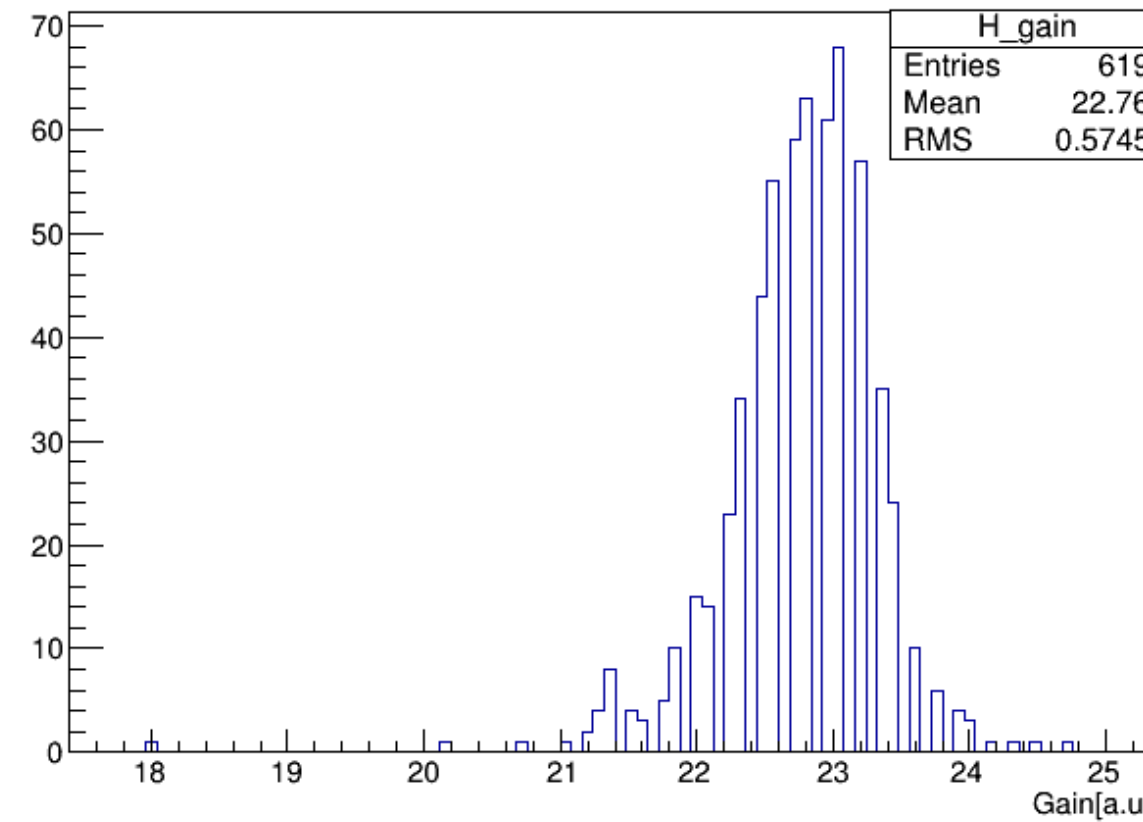
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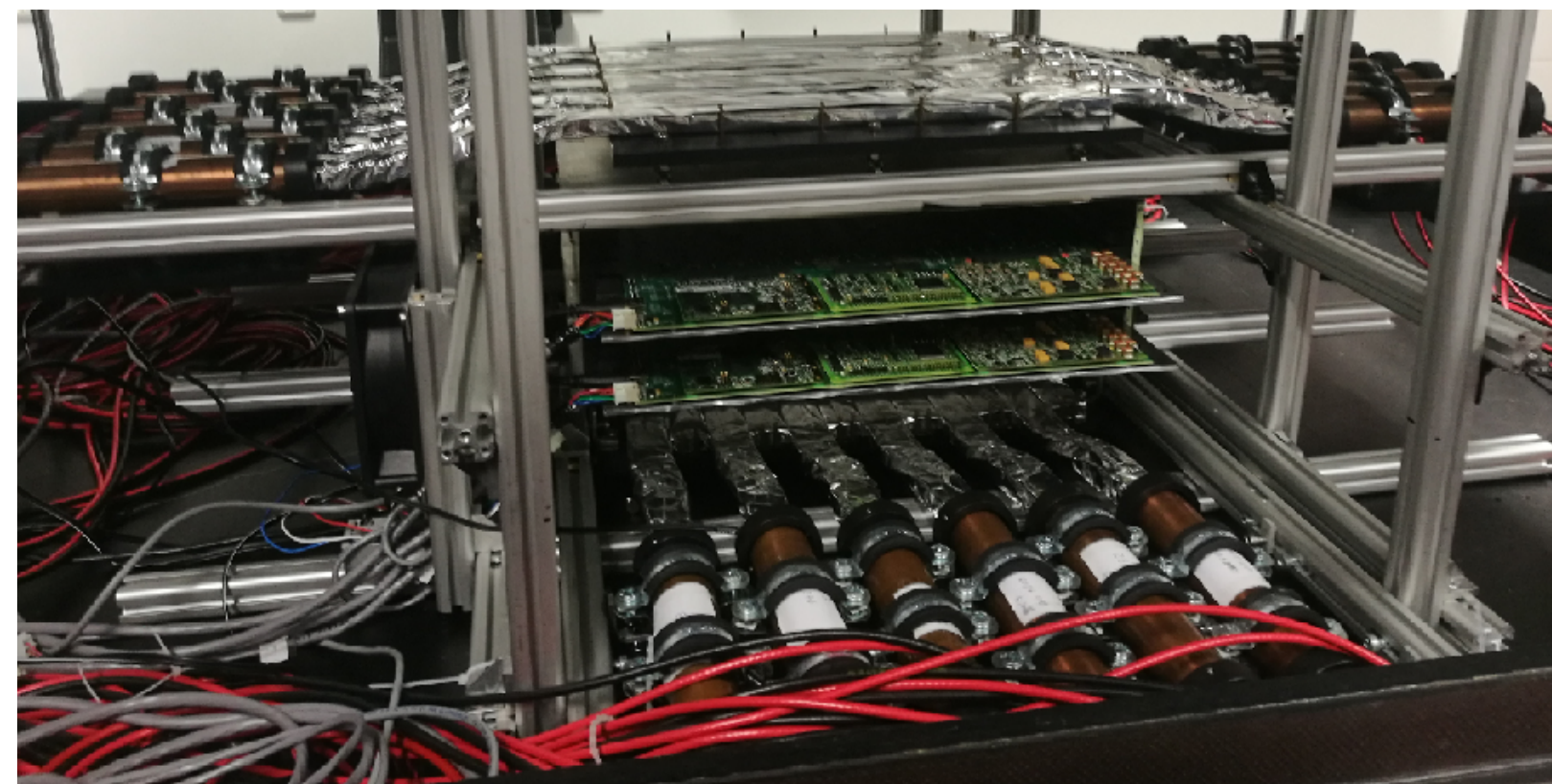
gain @ vbr_mean+5



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test and calibration of all
channels with cosmics



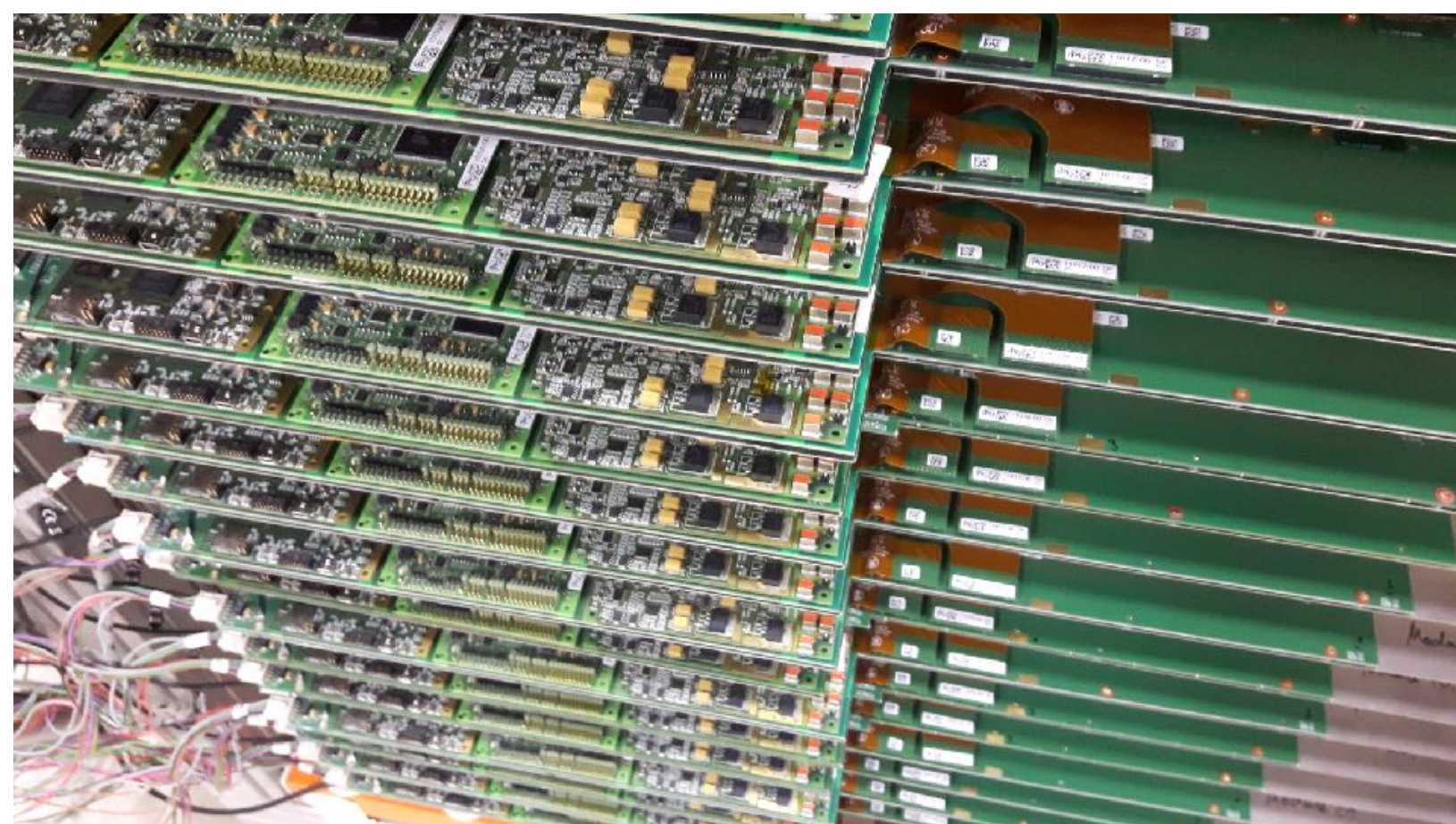
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SiPM-on-Tile Technology

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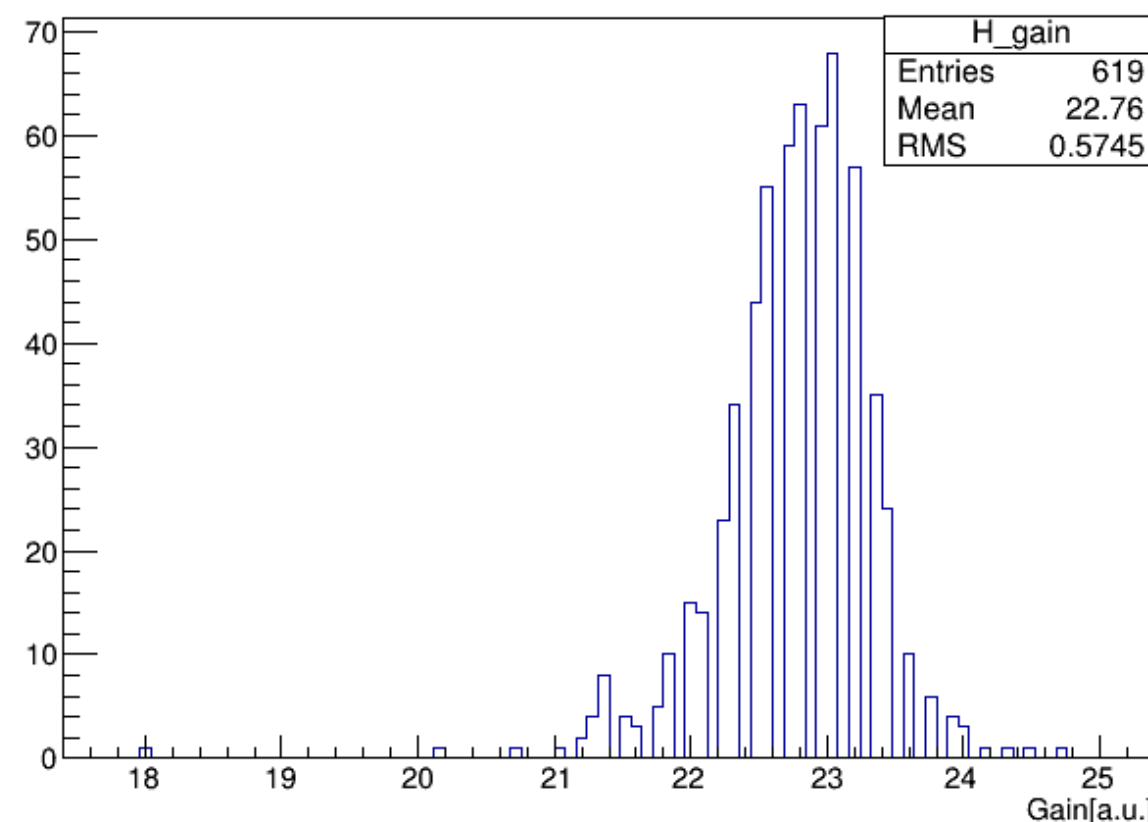


integration of layers & interfaces,
test in beam at DESY

test and calibration of all
channels with cosmics



gain @ vbr_mean+5



spot testing of few % of 22k SiPMs,
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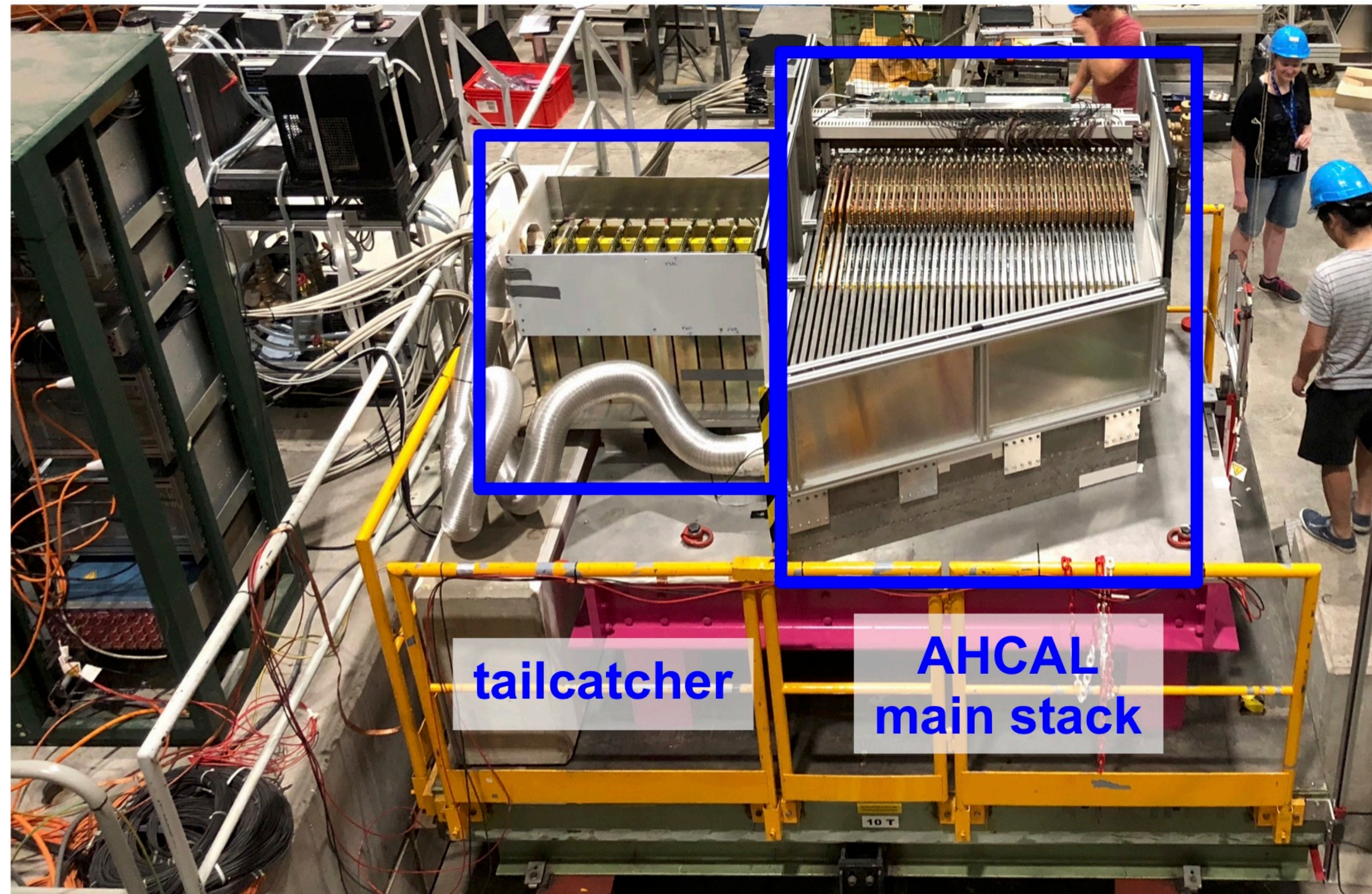
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SiPM-on-Tile Technology

A closer look



- In May and June 2018: Test beam at CERN SPS - the smoothest CALICE test beams ever.

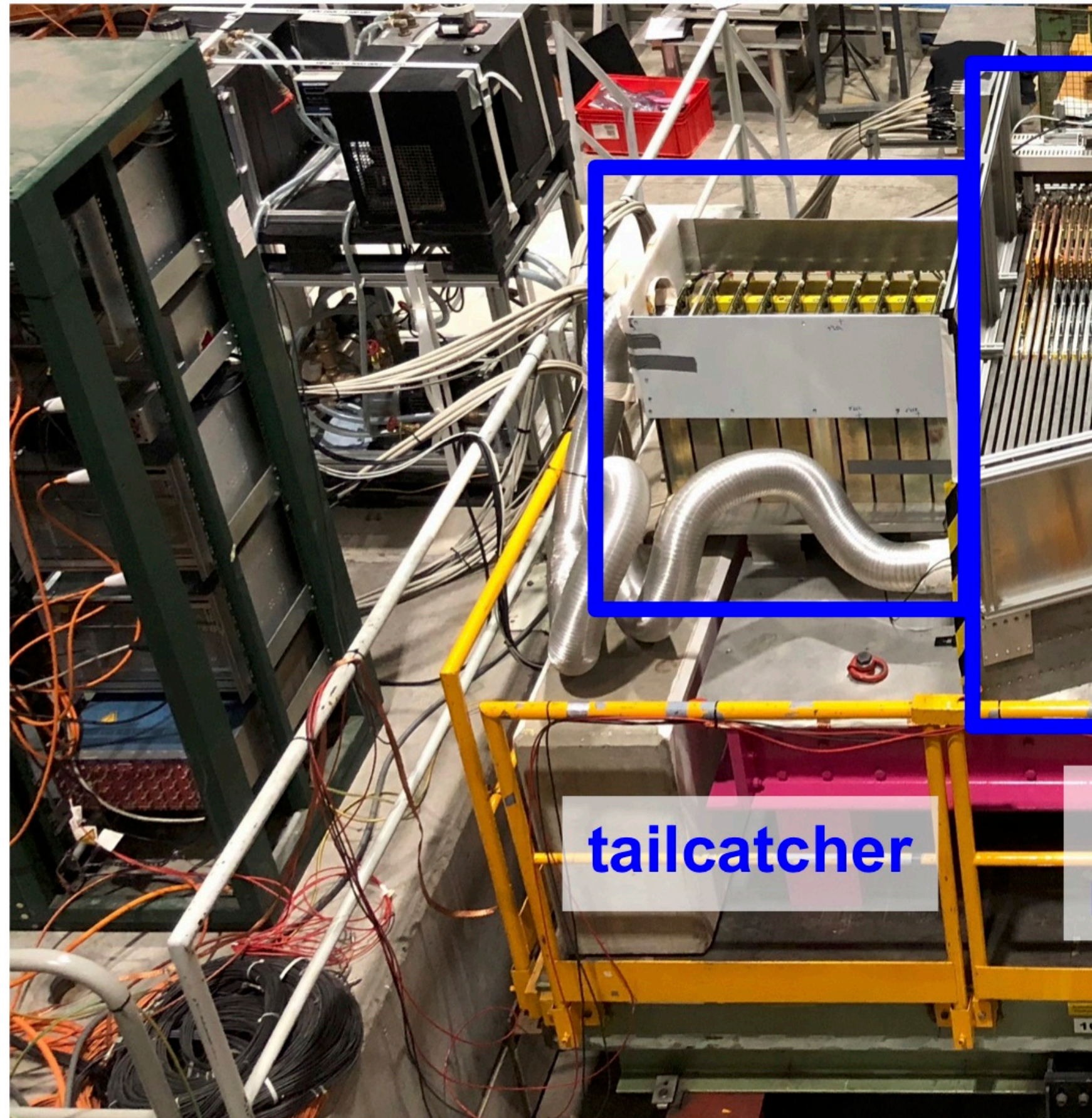


SiPM-on-Tile Technology

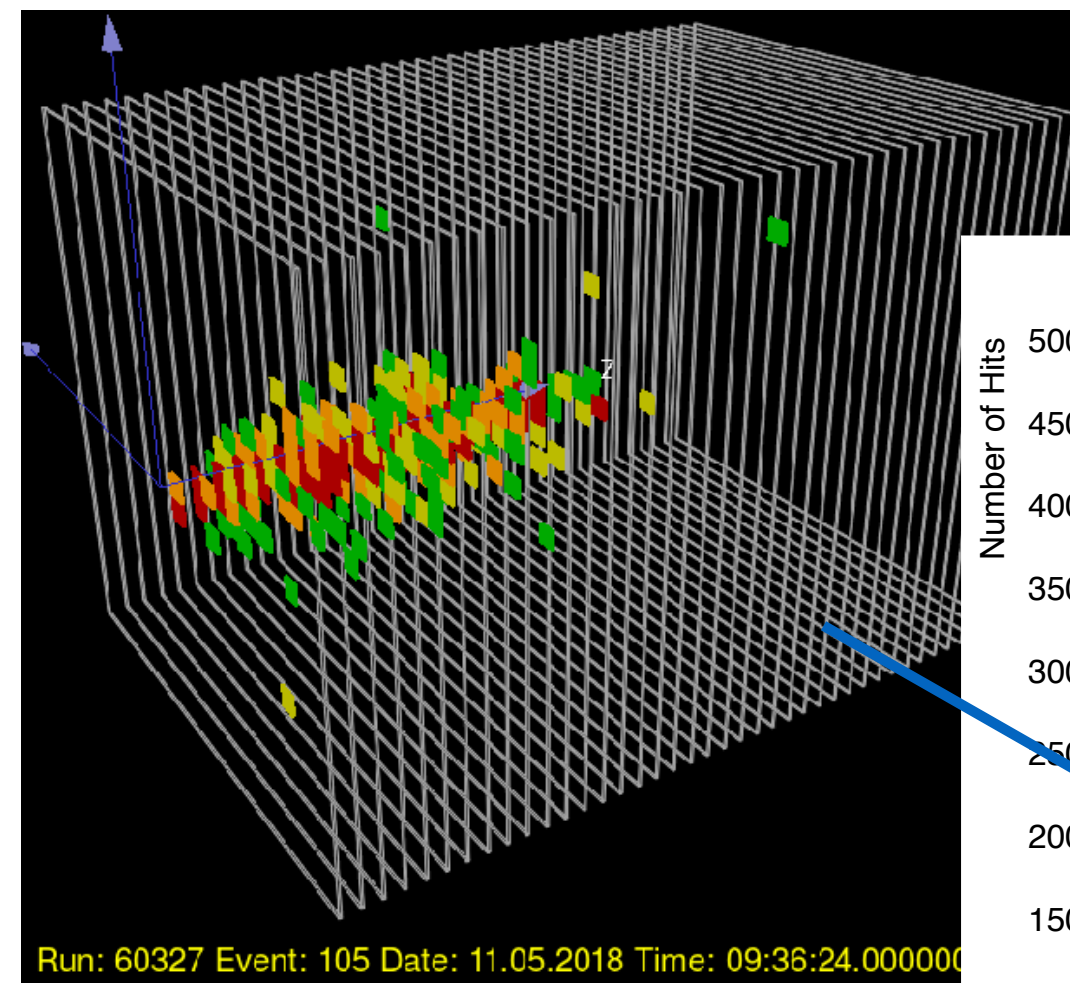
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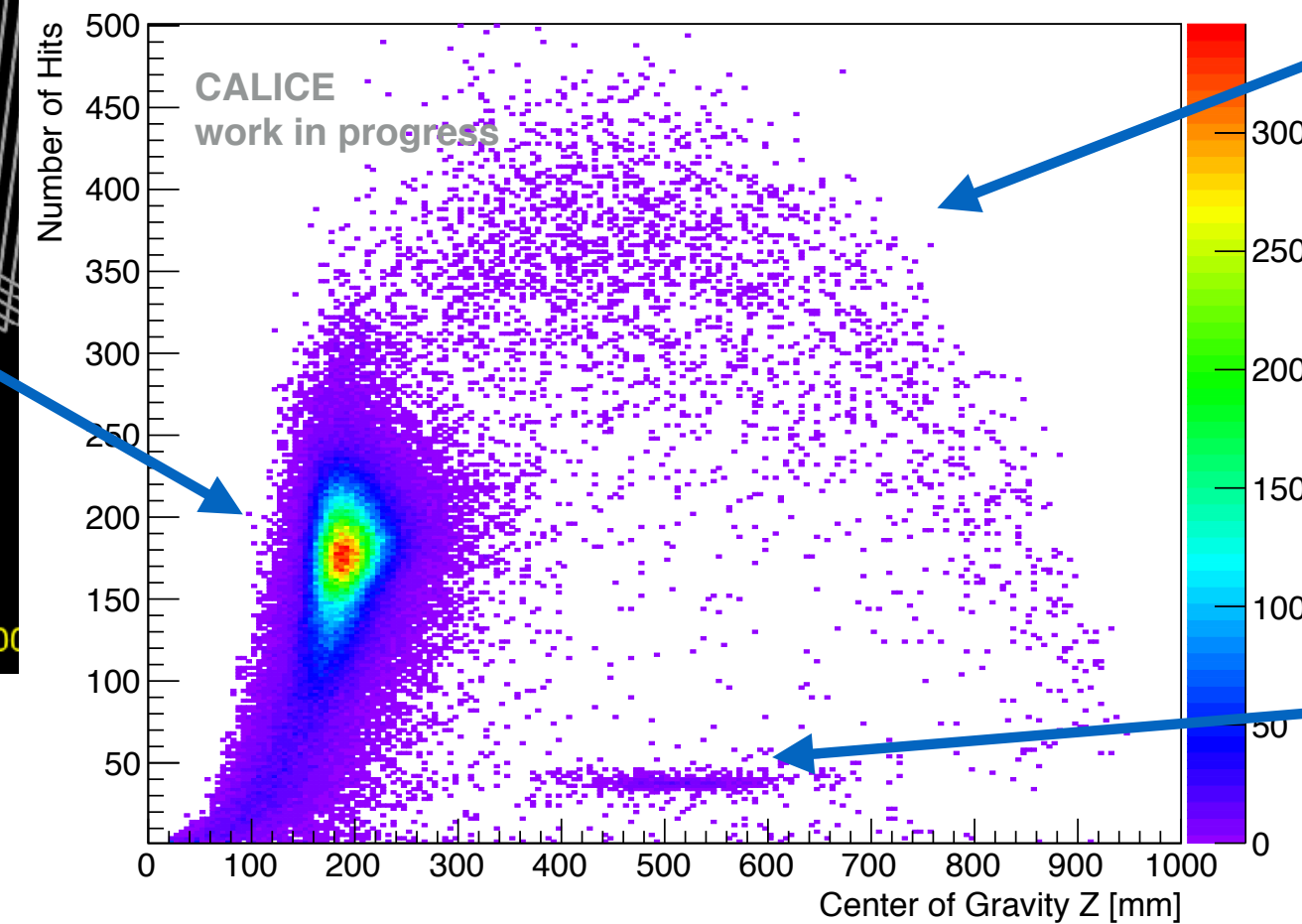


electron shower

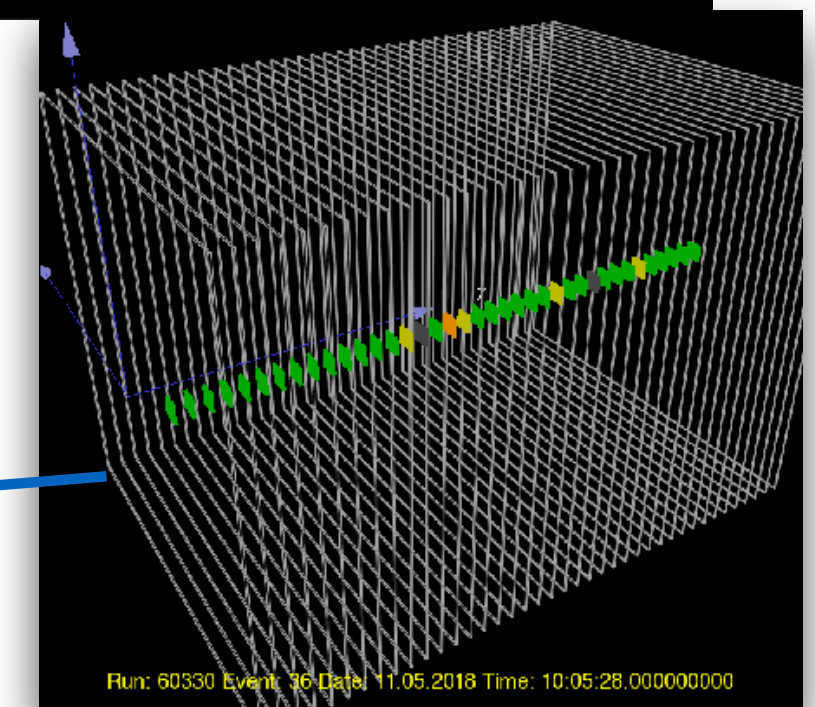
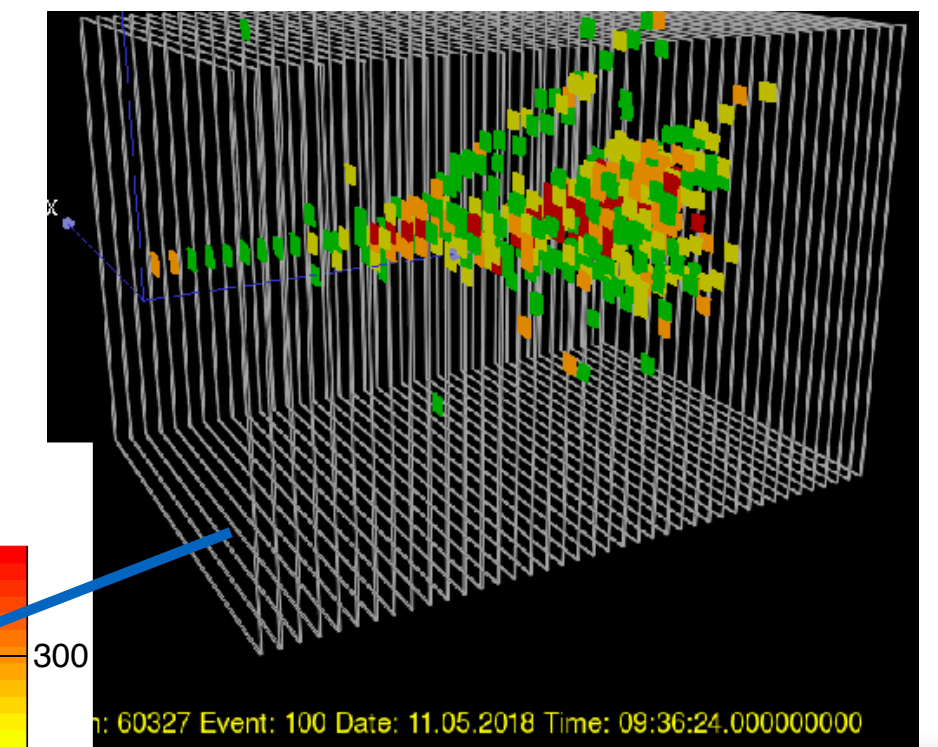


online data

50 GeV electron beam with pion and muon contamination



pion shower



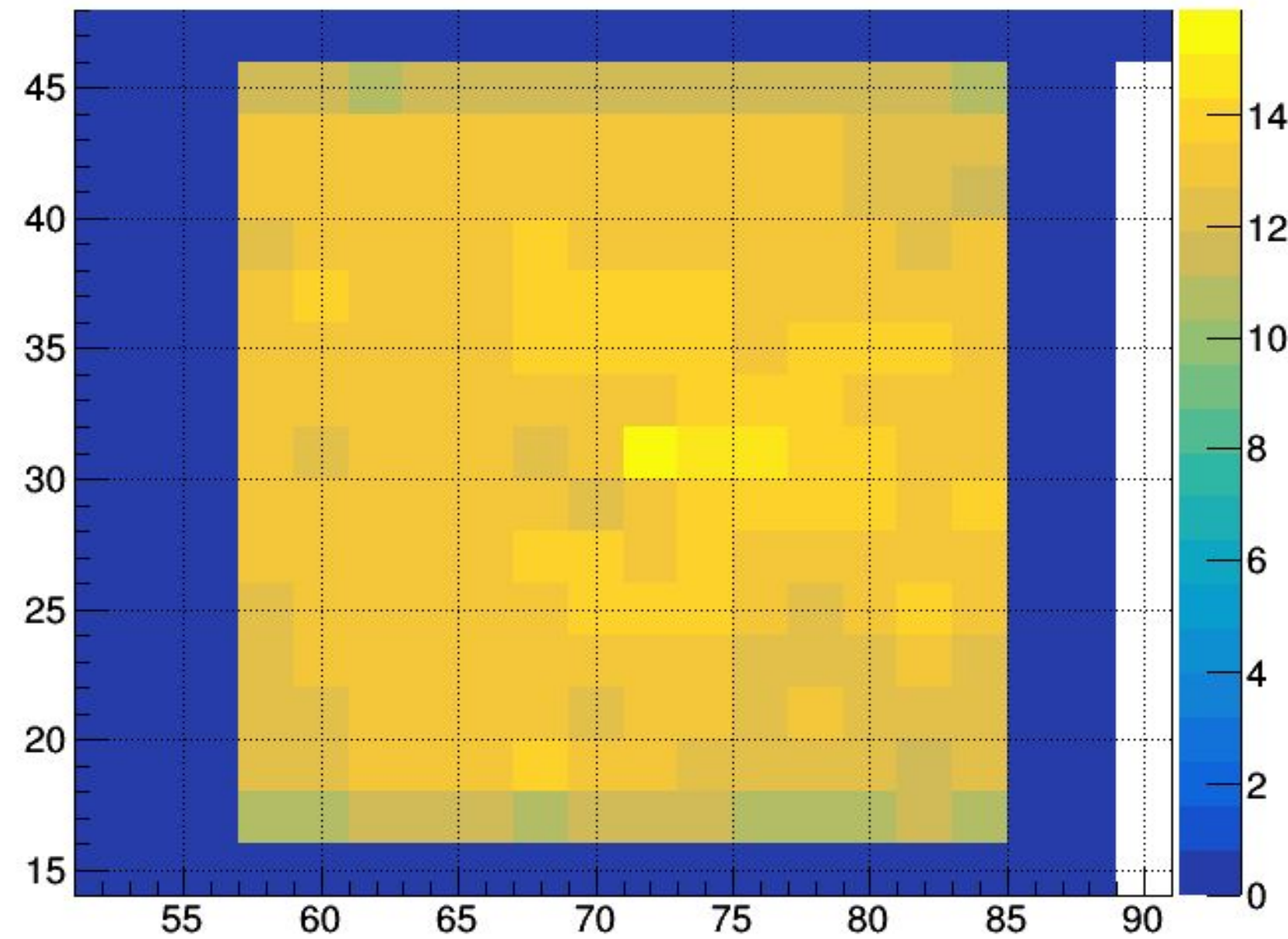
muon track

- Analysis ongoing - first results soon

SiPM-on-Tile for the ND ECAL

Understanding Impact of Tile imperfections

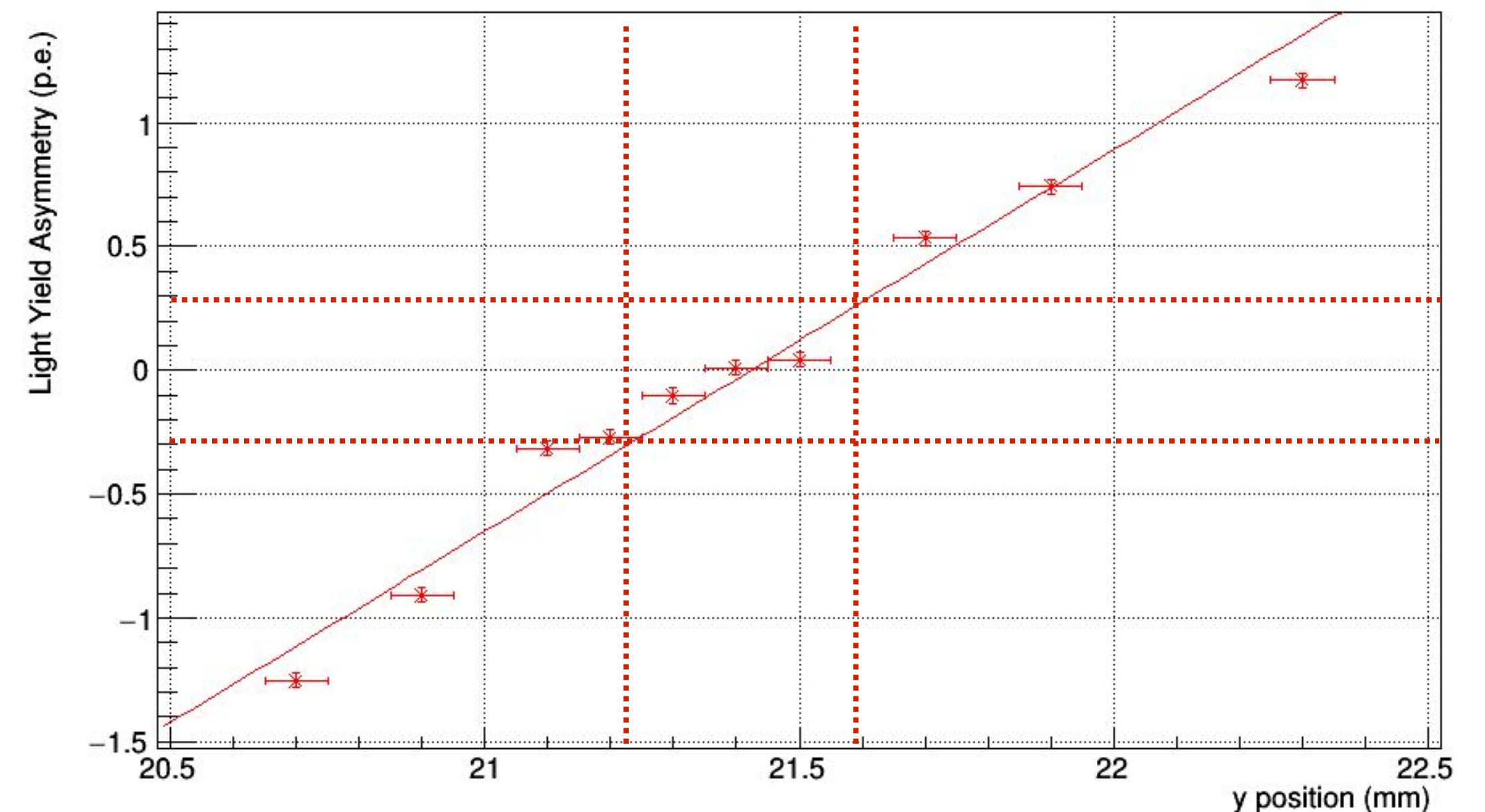
- Response of scintillator tiles not perfectly uniform



Typical variations 5 - 10% over tile surface, large fraction within a few % of mean

- Assembly tolerances leading to misalignment between SiPM and tile can lead to increased non-uniformity

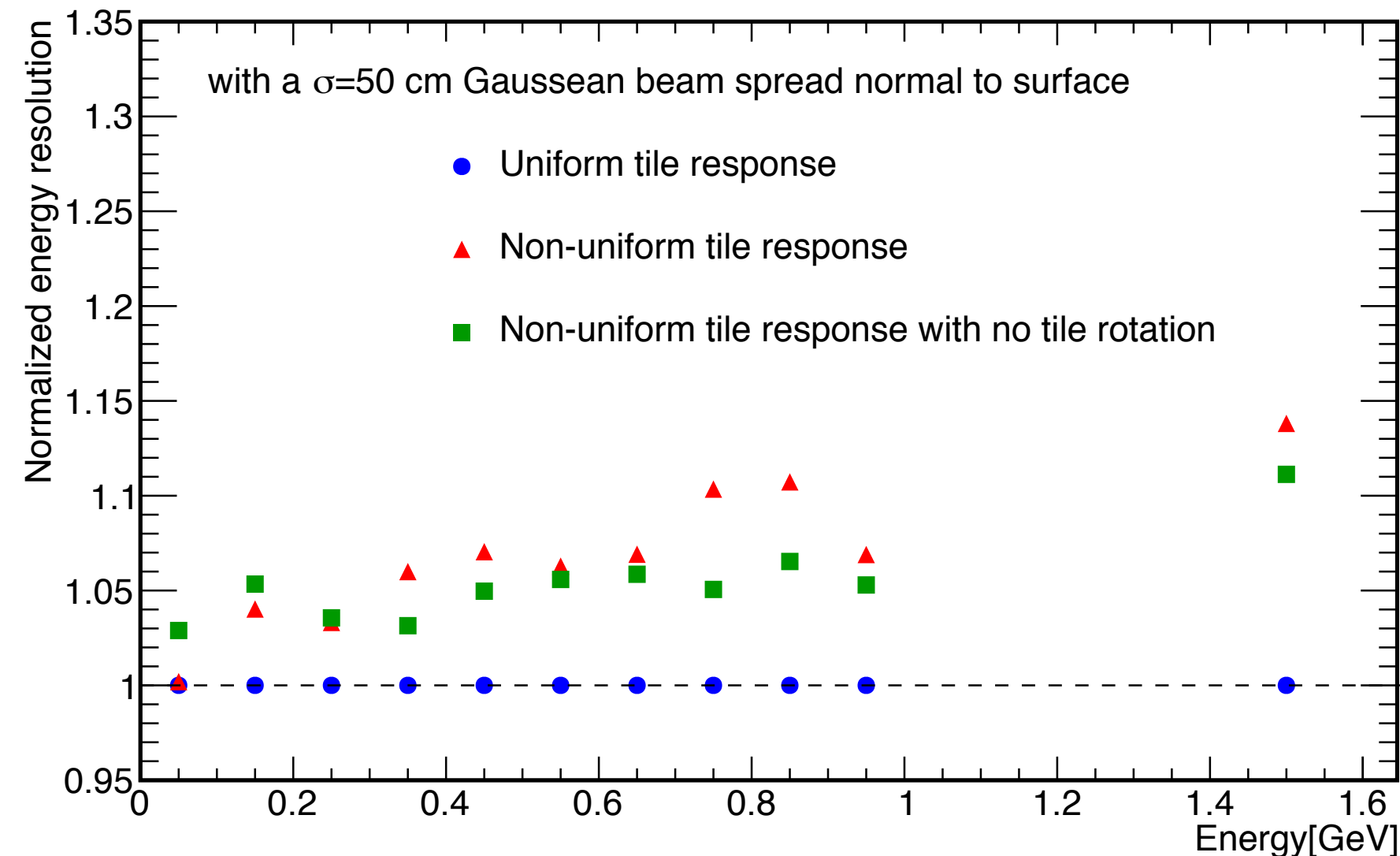
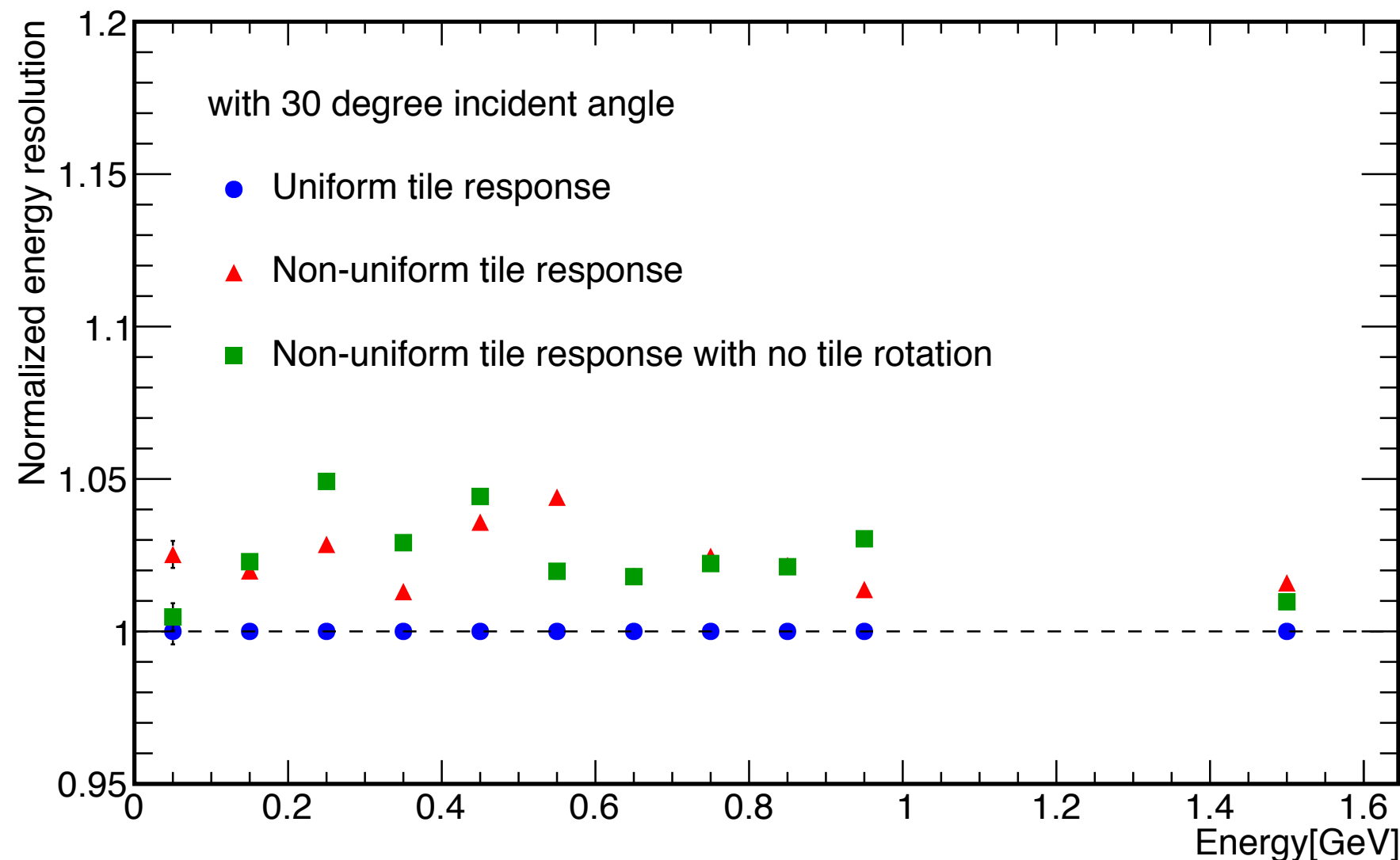
Misalignment generates a “dipole” in the response:
global asymmetry in direction of misalignment
2% asymmetry for 175 μm offset
Expect 100 μm easily achievable



SiPM-on-Tile for the ND ECAL

Understanding Impact of Tile imperfections

- Simulations of an “infinitely thick” tile-only ECAL with realistic non-uniformities implemented, including effects of $\sim 100 \mu\text{m}$ SiPM / tile misalignment
 - at present all layers the same: expected to be more damaging than random alignment
 - random orientation within each layer also studied



typically $\sim 5\%$ degradation,
worse for near-normal
incidence at high energy

200 μm dead zone around
each tile adds a
comparable degradation

Bottom line: By no means a show-stopper - SiPM-on-tile useable also for high-resolution ECAL

⇒ Next step: Understand impact of non-uniform material distribution induced by ASICs inside layers...

Rethinking the Strip Solution

A possible alternative - capitalizing on timing

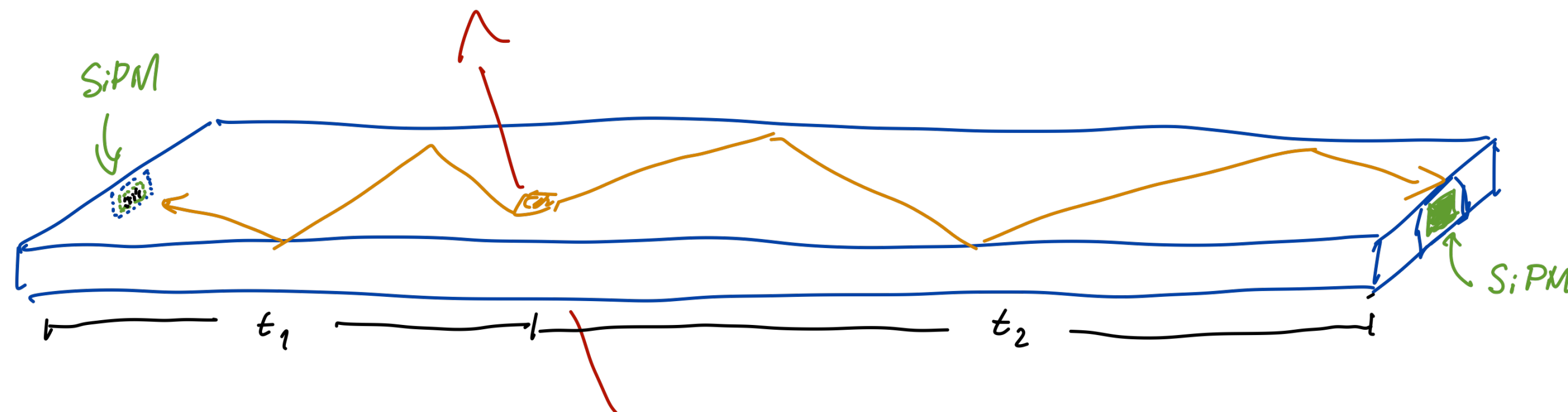


- Scintillator strips with embedded wavelength-shifting fibers a “standard technology”, but:
 - Fibers have a negative impact on timing
 - Fibers are a relevant cost driver

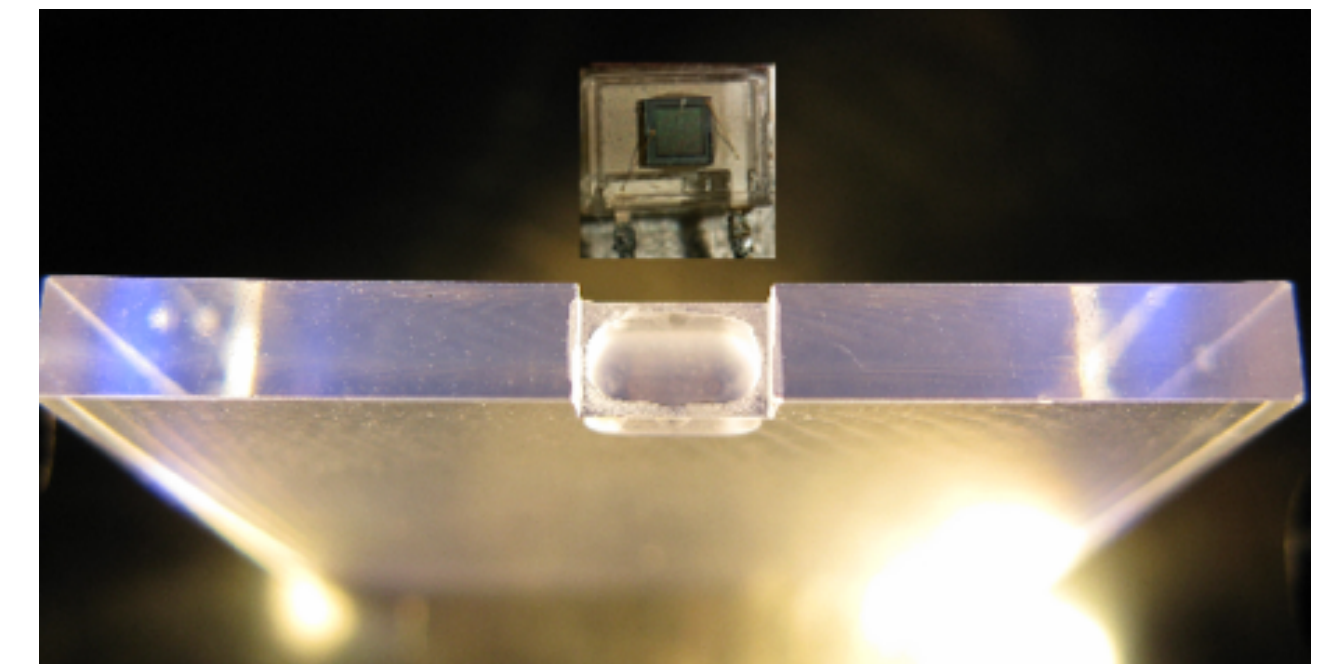
Rethinking the Strip Solution

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 - Fibers have a negative impact on timing
 - Fibers are a relevant cost driver
- ⇒ Consider strips with direct readout at both ends - position resolution within strip via timing
 - May require a larger SiPM for increased light yield: Offsets cost advantage of eliminating fiber
 - Requires highly transparent scintillator, possibly shorter strips for sufficiently high and uniform light yield



Profit from earlier studies of direct side coupling at MPP

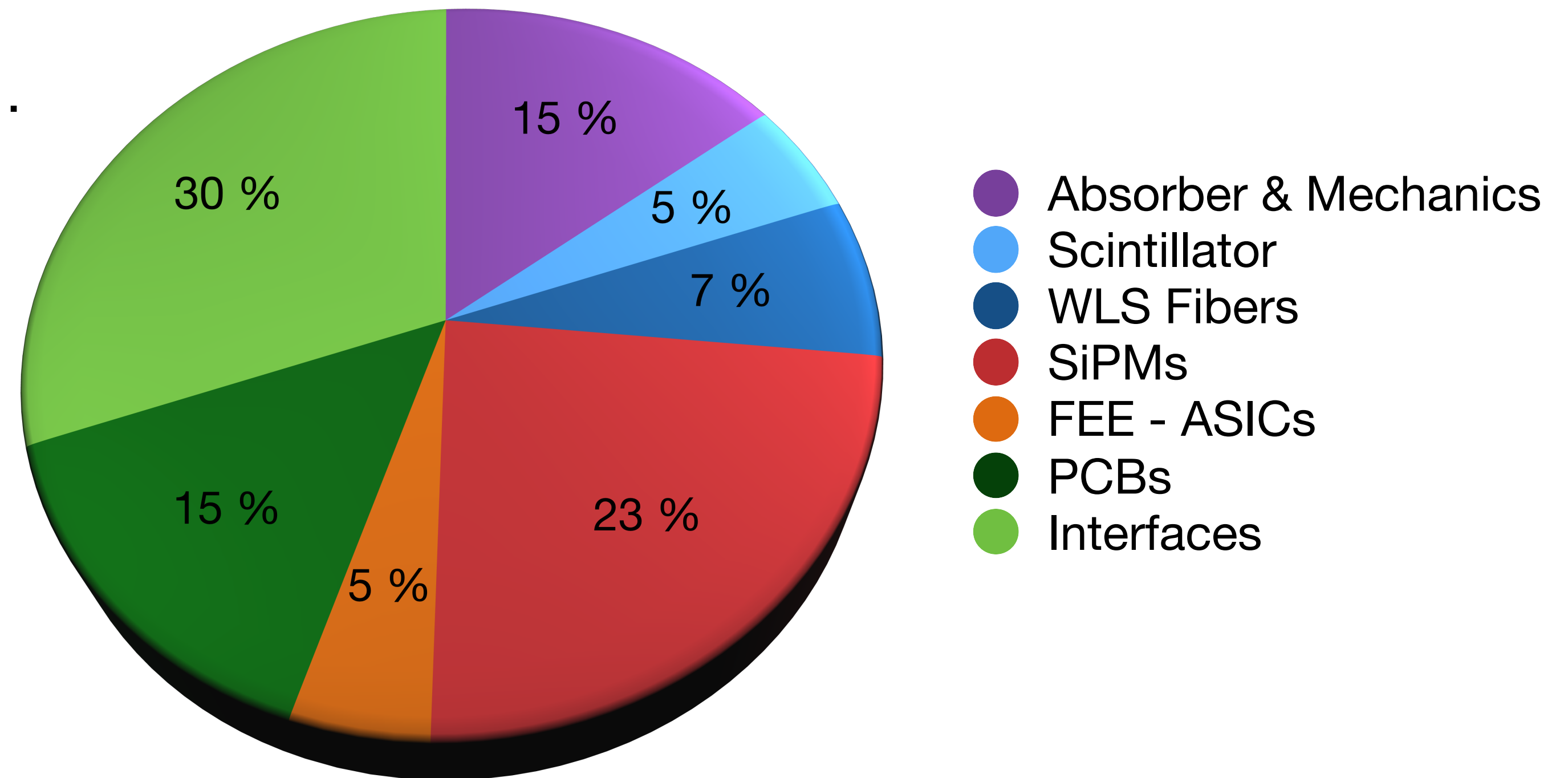


A Few Words on Cost

Without concrete numbers - work in progress

- Based on the current design presented by Eldwan (8 HG, 72 LG layers DS, 6 HG, 54 LG layers US)
 - Results in ~3.3 M channels, ~ 90% in the HG elements
 - Cost estimates based on CALICE AHCAL, CMS HGCAL, Belle II KLM,...

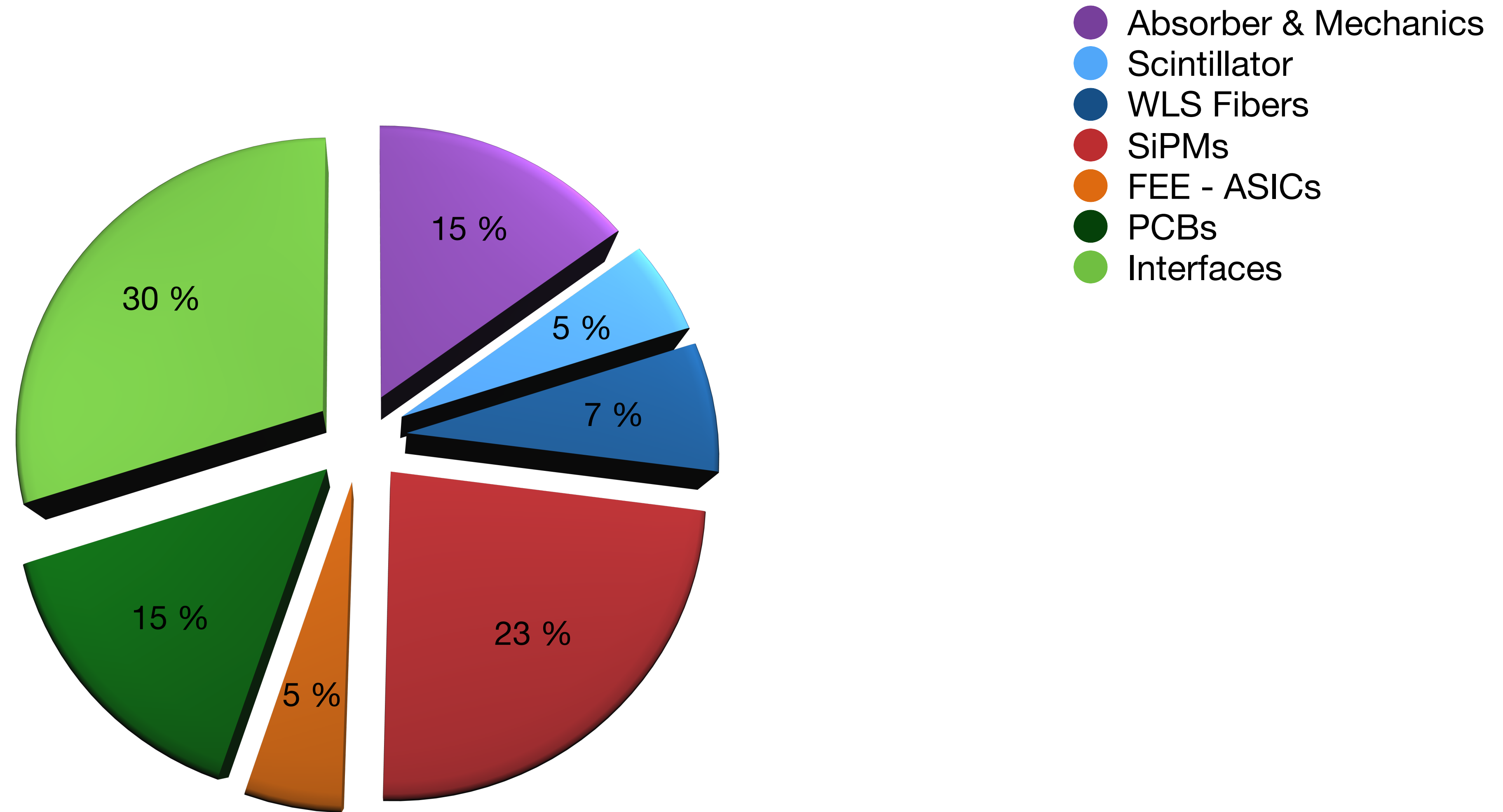
- Size matters:
 - ~ 35 m³ absorber (when using Cu)
 - ~ 85 m³ scintillator
 - ~ 400 km fibers
 - ~ 1900 m² PCB for HG layers



- Channel count the main cost driver - clearly need to understand how much is needed / can be justified (*also remarked by LBNC*)
- ⇒ Have to find an optimal working point in terms of performance, feasibility and “technological interest”

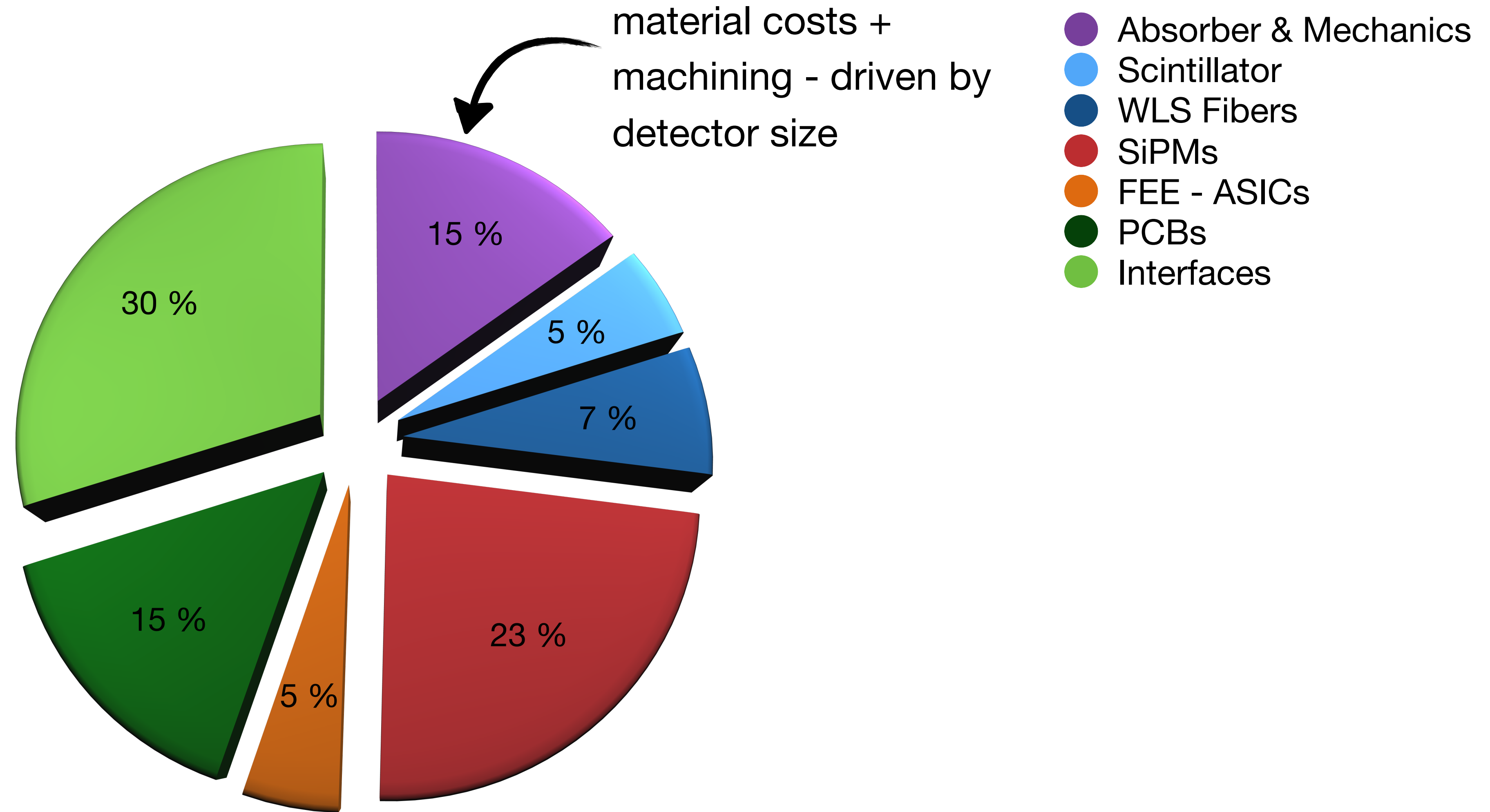
A Few Words on Cost

Zooming in on scaling expectations



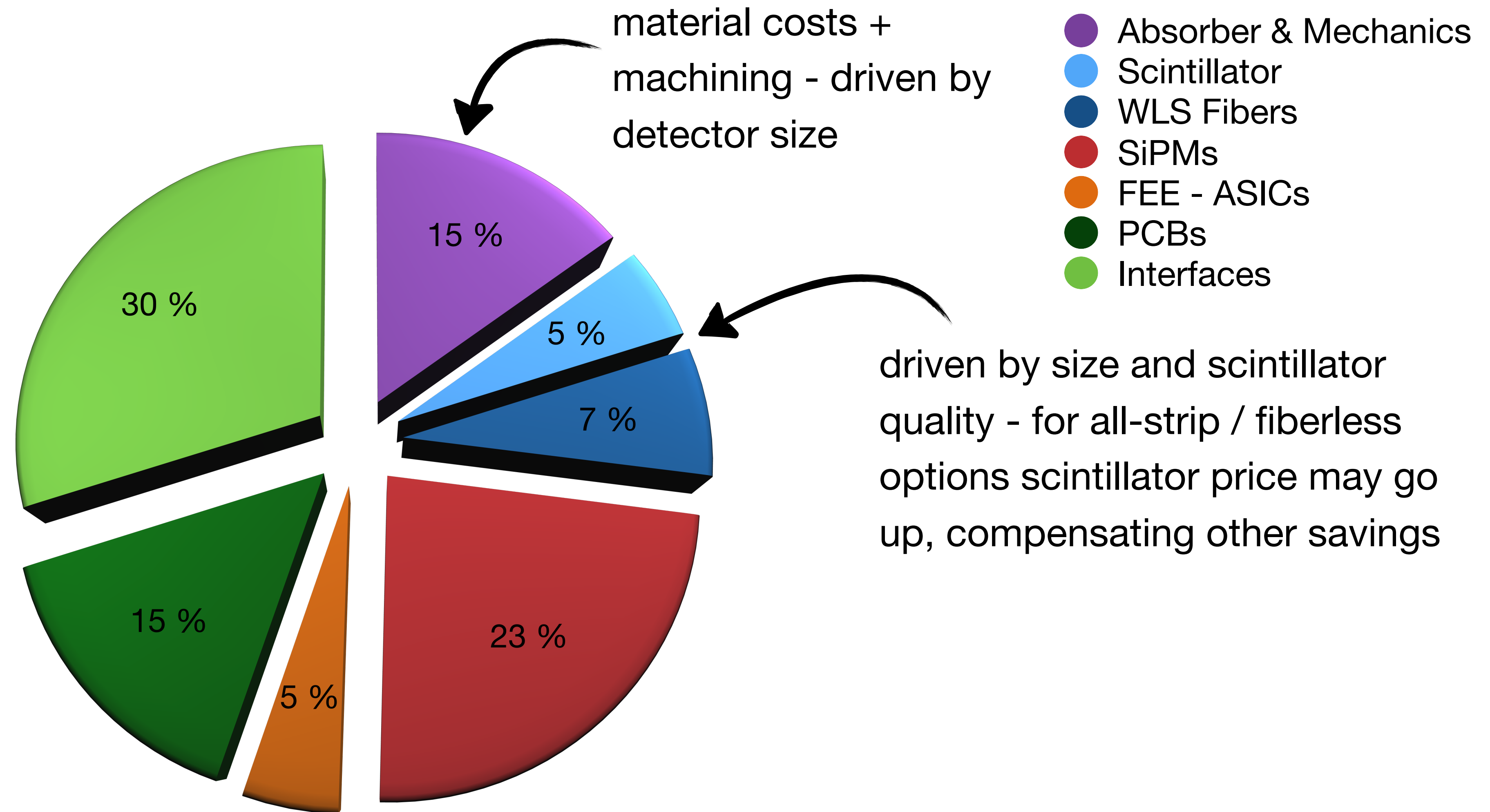
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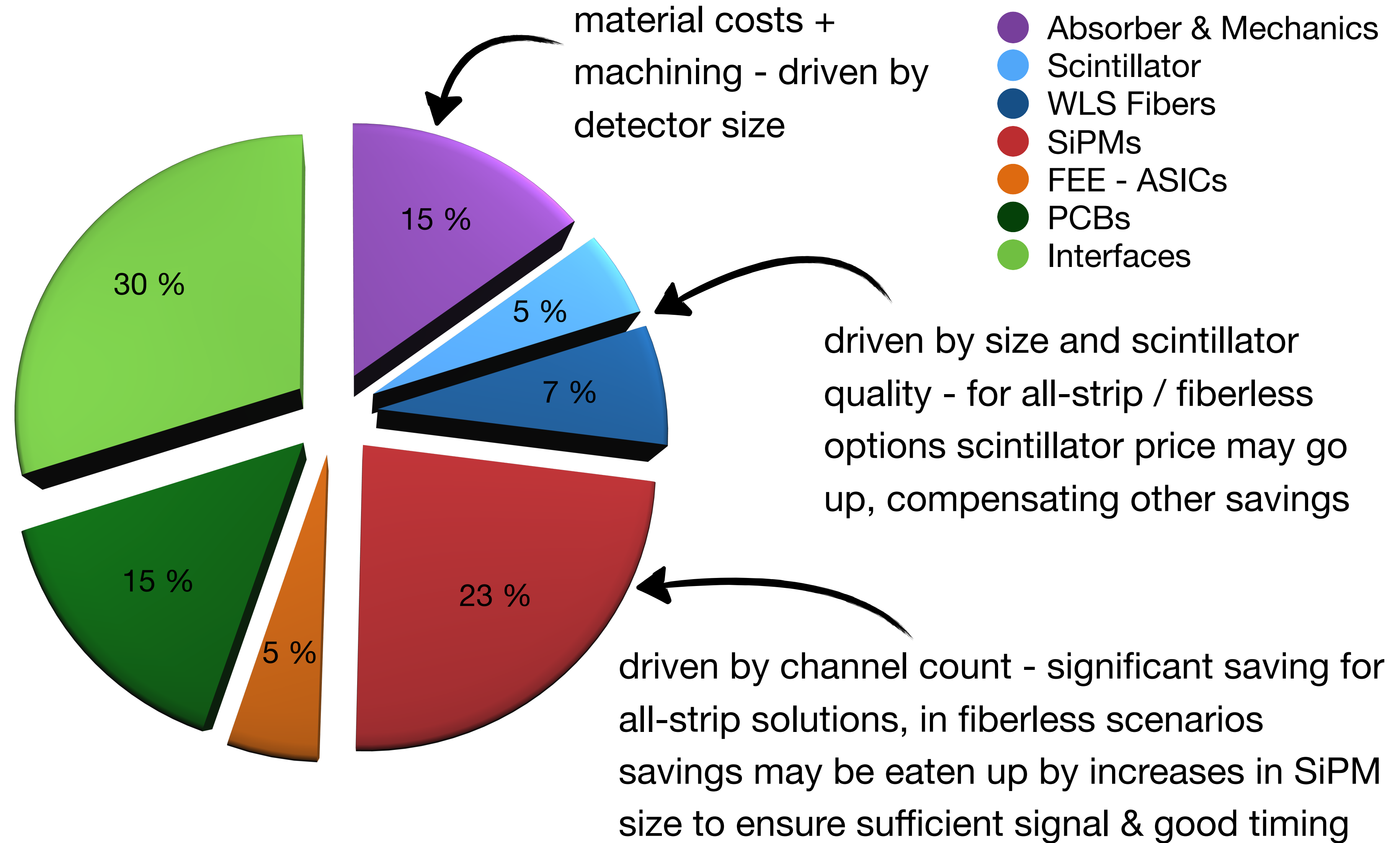
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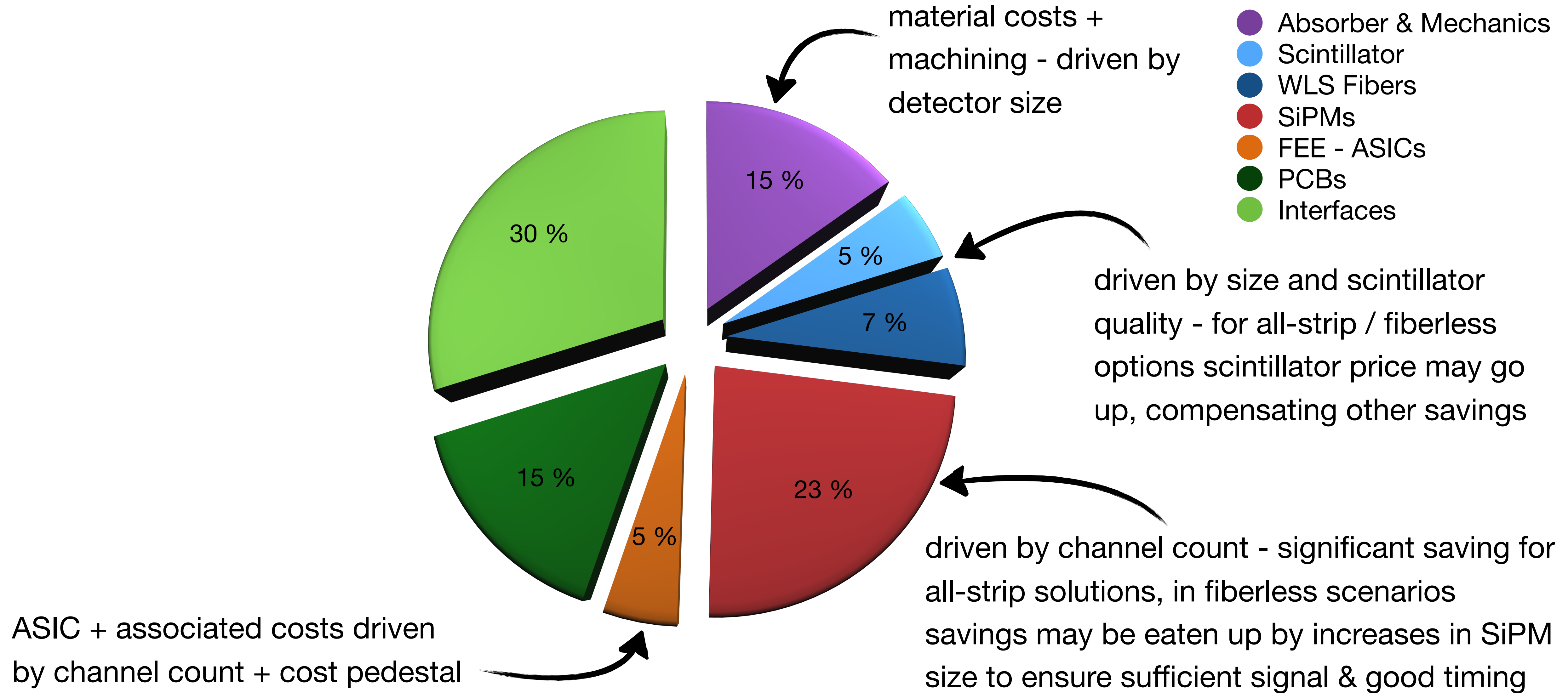
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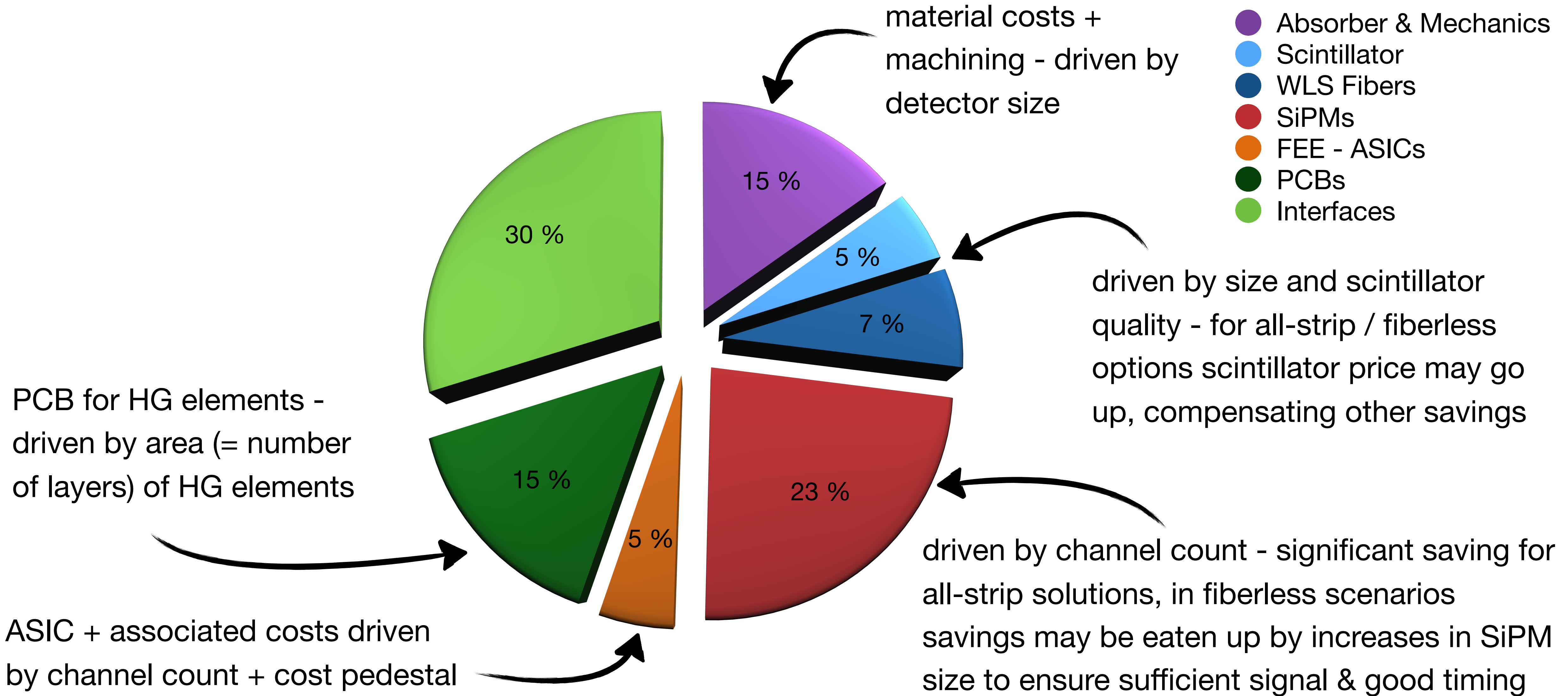
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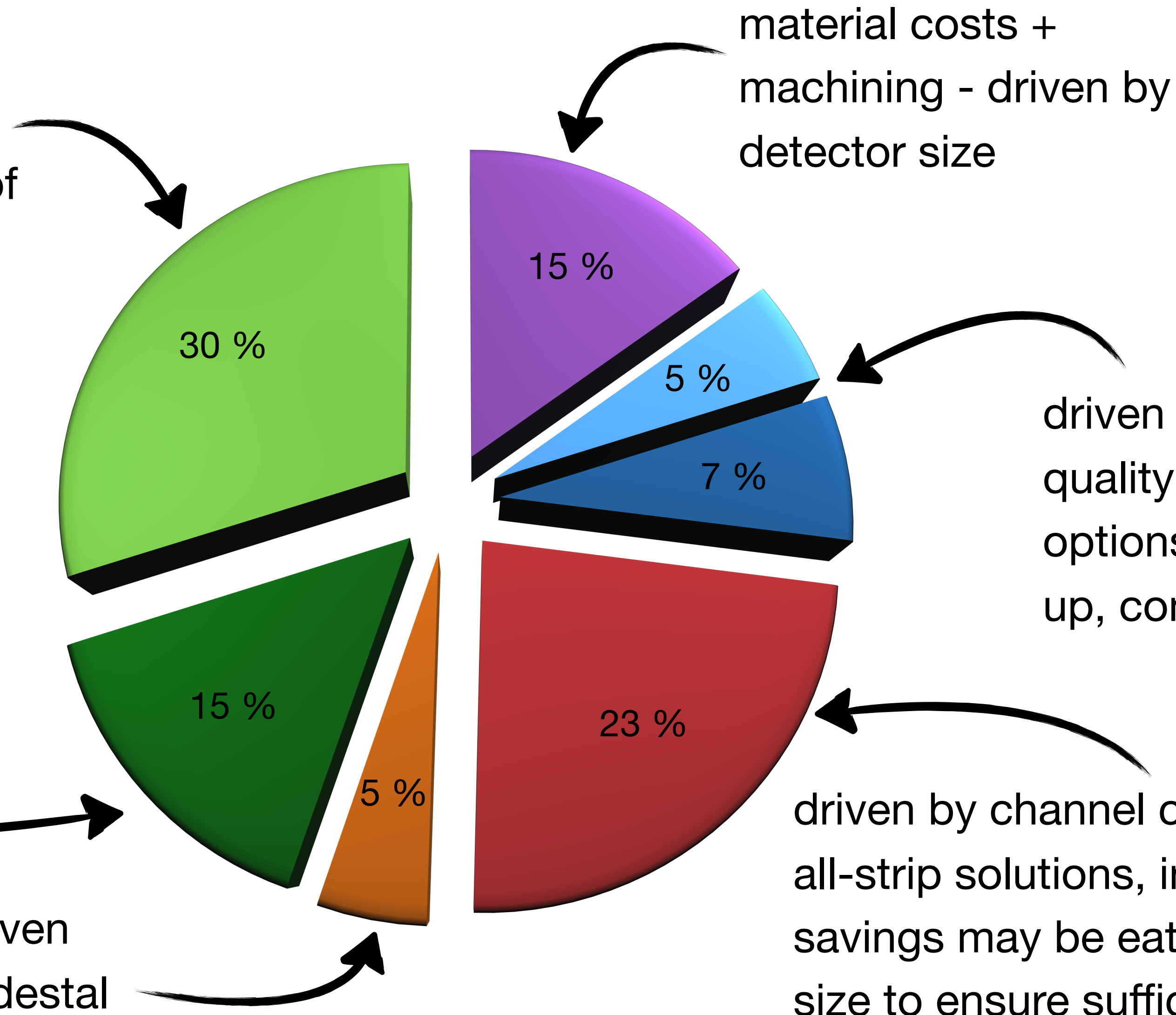
A Few Words on Cost

Zooming in on scaling expectations

Interfaces (data collection, calibration, control) - at present driven by number of layers - significant savings possible for non-HG layers by grouping layers

PCB for HG elements - driven by area (= number of layers) of HG elements

ASIC + associated costs driven by channel count + cost pedestal



- Absorber & Mechanics
- Scintillator
- WLS Fibers
- SiPMs
- FEE - ASICs
- PCBs
- Interfaces

material costs + machining - driven by detector size

driven by size and scintillator quality - for all-strip / fiberless options scintillator price may go up, compensating other savings

driven by channel count - significant saving for all-strip solutions, in fiberless scenarios savings may be eaten up by increases in SiPM size to ensure sufficient signal & good timing

Upcoming R&D activities

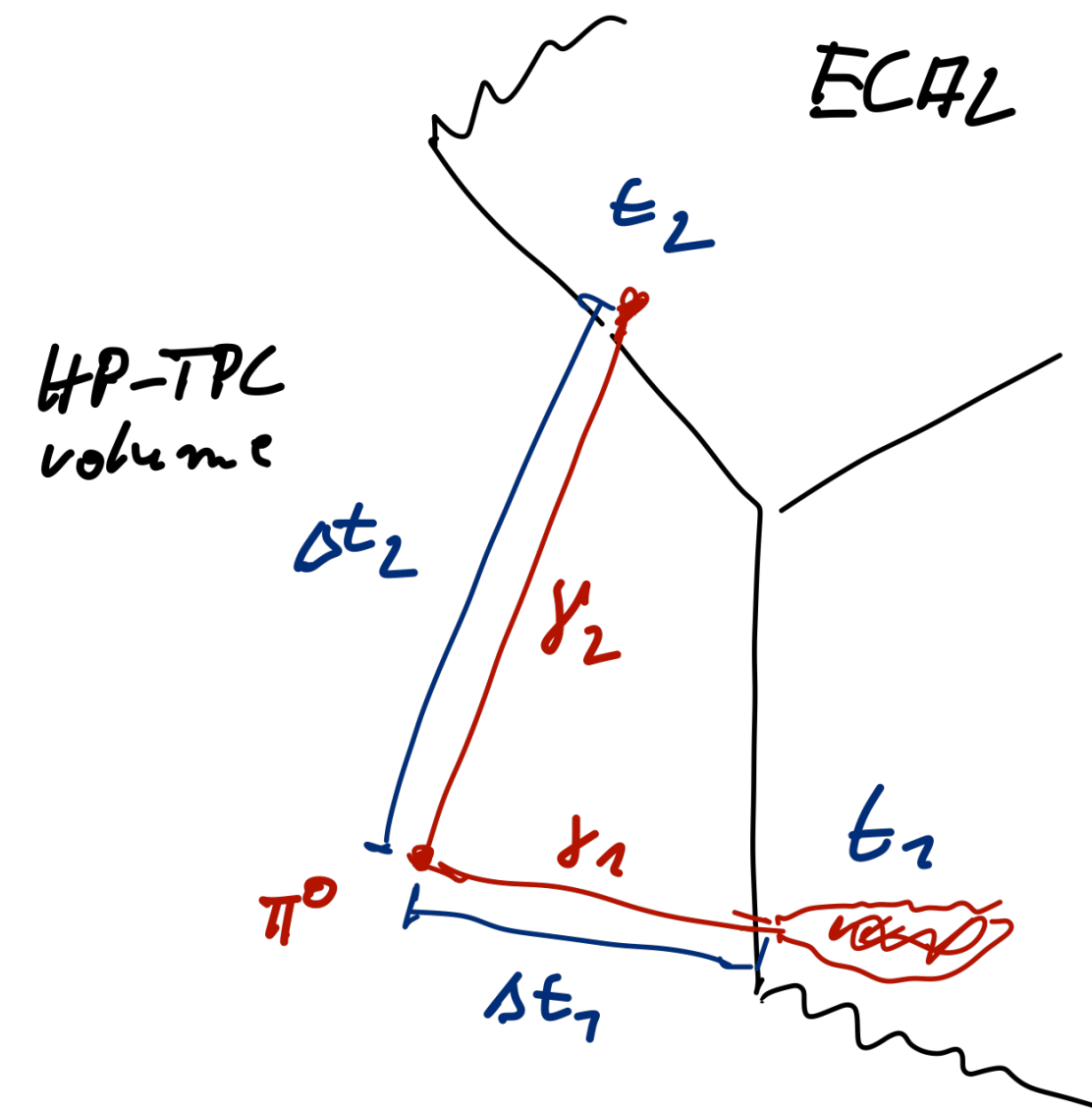
The path forward

- Understand perspectives for key goals (including neutrons!) in *realistic background environment*
- Further understand / develop reconstruction/ performance of all relevant objects
- One example: “Timing-assisted π^0 reconstruction”

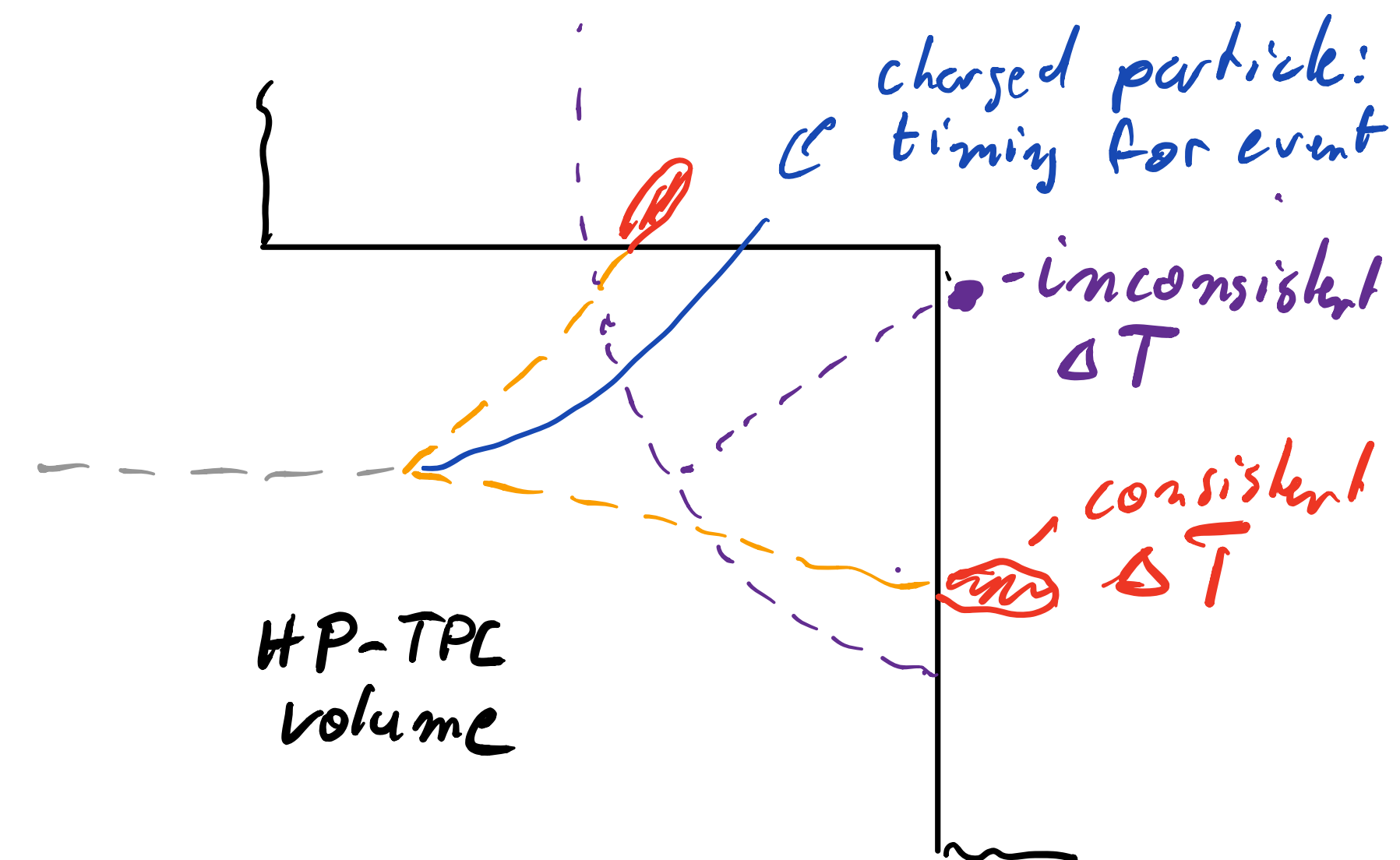
In first MPP studies:
direction + energy of cluster
(challenging for low energies!)

with few 100 ps timing:
may improve π^0 localization

$$\Rightarrow \Delta t_2 - \Delta t_1 \approx t_2 - t_1$$



also: general use of timing
in particle association



- On the hardware side:
 - Start exploring strip options
 - Possibly investigate boron-doped scintillators as a possibility to boost low-energy neutron sensitivity
 - ...

Conclusions

Well, not really

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But:

- Need to understand what features are actually needed to achieve the needed performance
- Need to understand the which aspects of the goals are achievable in a realistic background environment
- Develop reconstruction to get fully realistic performance estimates
- Perform hardware R&D to identify optimal (performance, cost) technological solutions

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- And, last but not least: Need to get the ECAL on the real axis