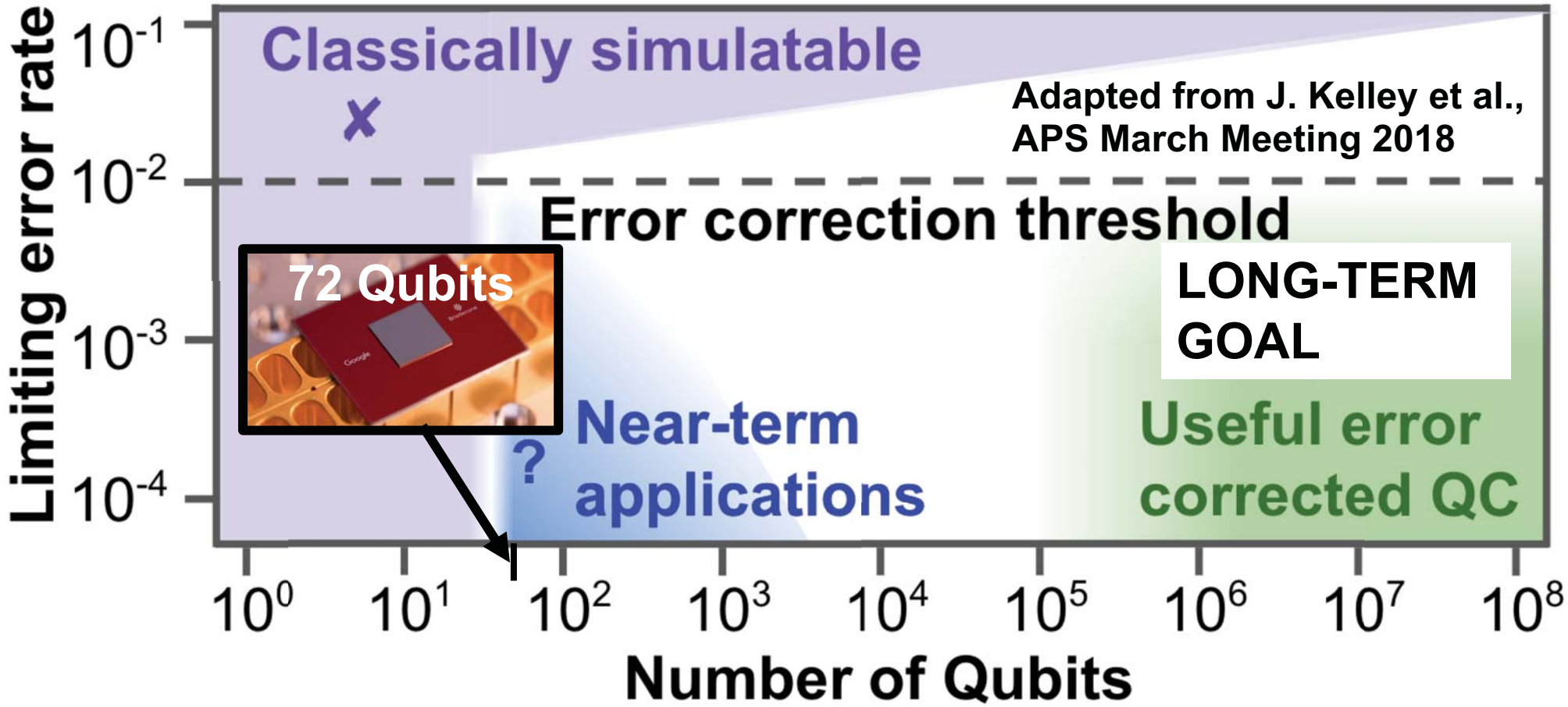
XY Control of Transmon Qubits

Joseph Bardin

UMass Amherst/Google AI Quantum

06/17/2019

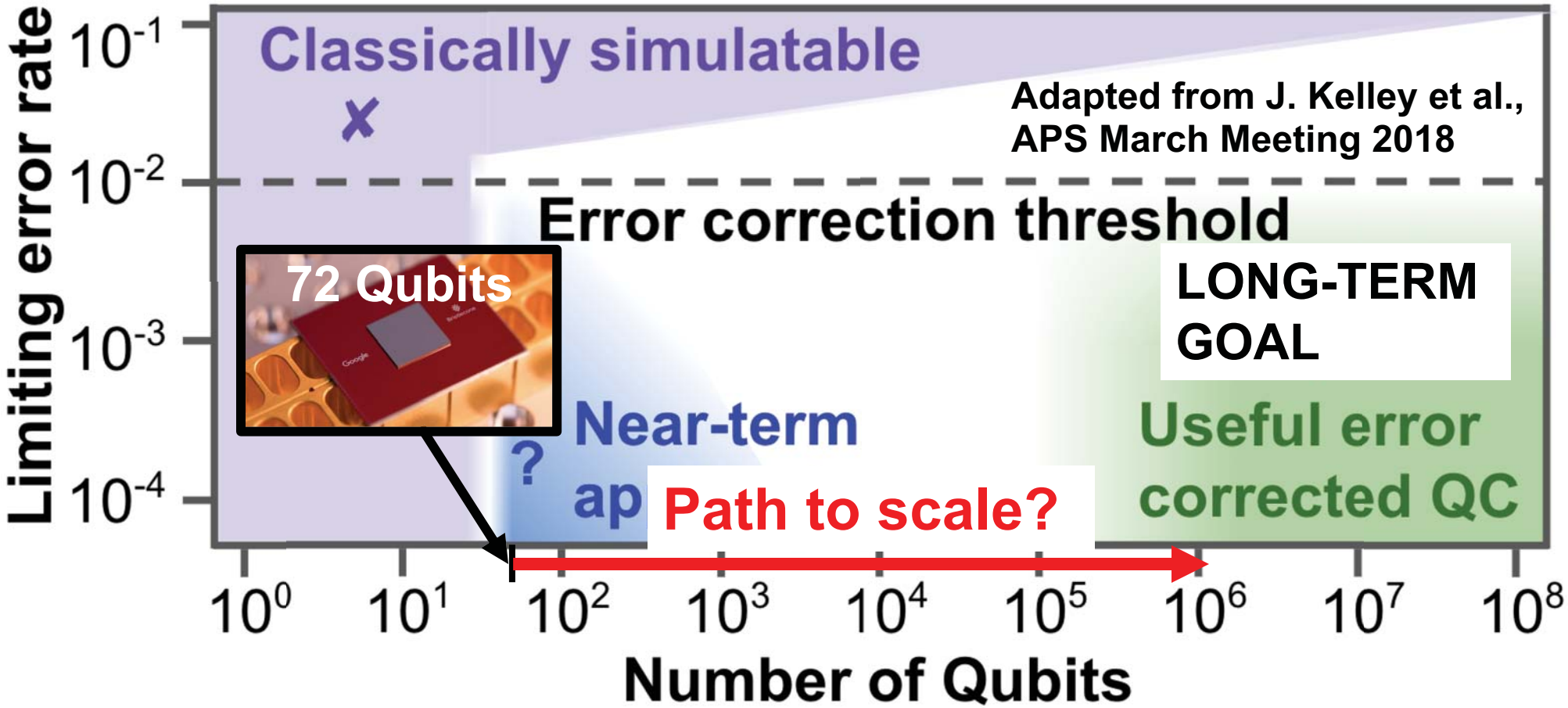
How many qubits for practical QC?



State of the art today: 72 qubits

Error corrected quantum computer: 1e6 qubits

There is a long way to go!



State of the art today: 72 qubits

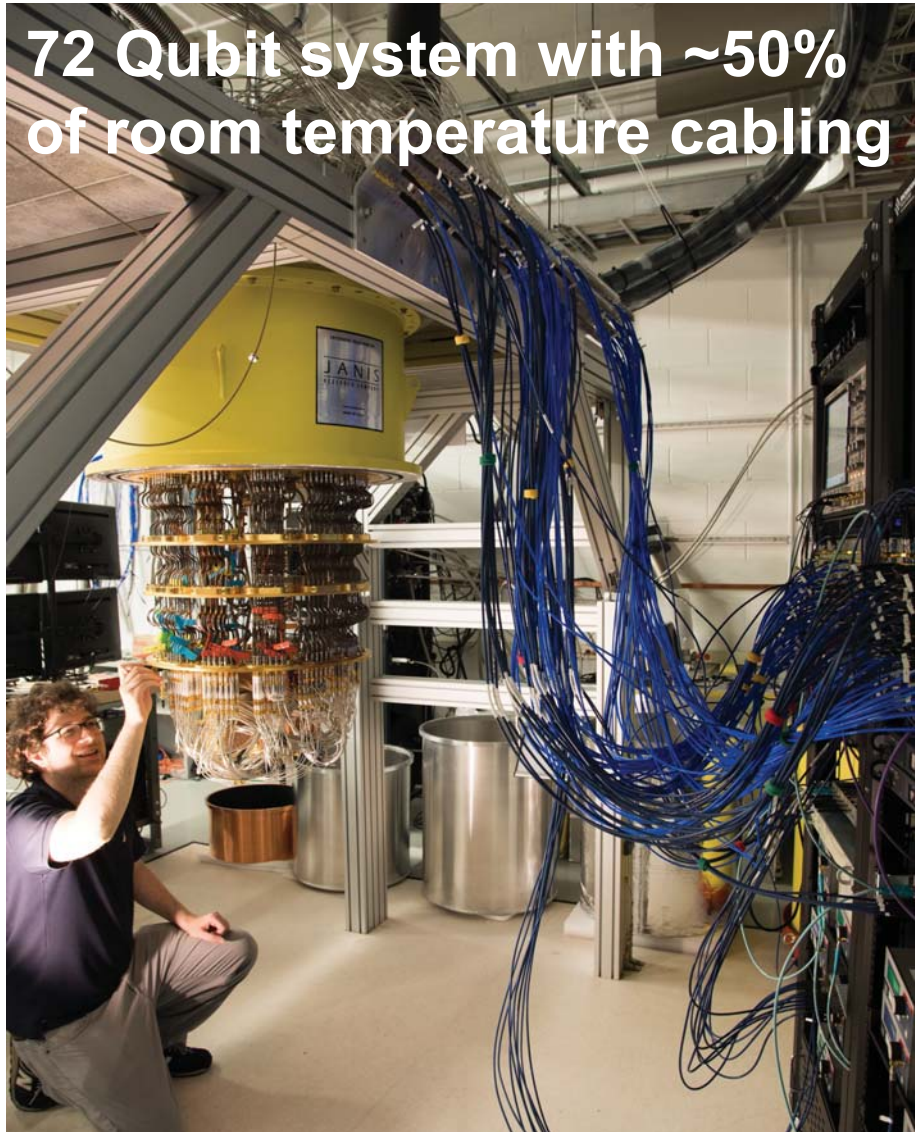
Error corrected quantum computer: 1e6 qubits

What Does a 72-Qubit System Look Like?

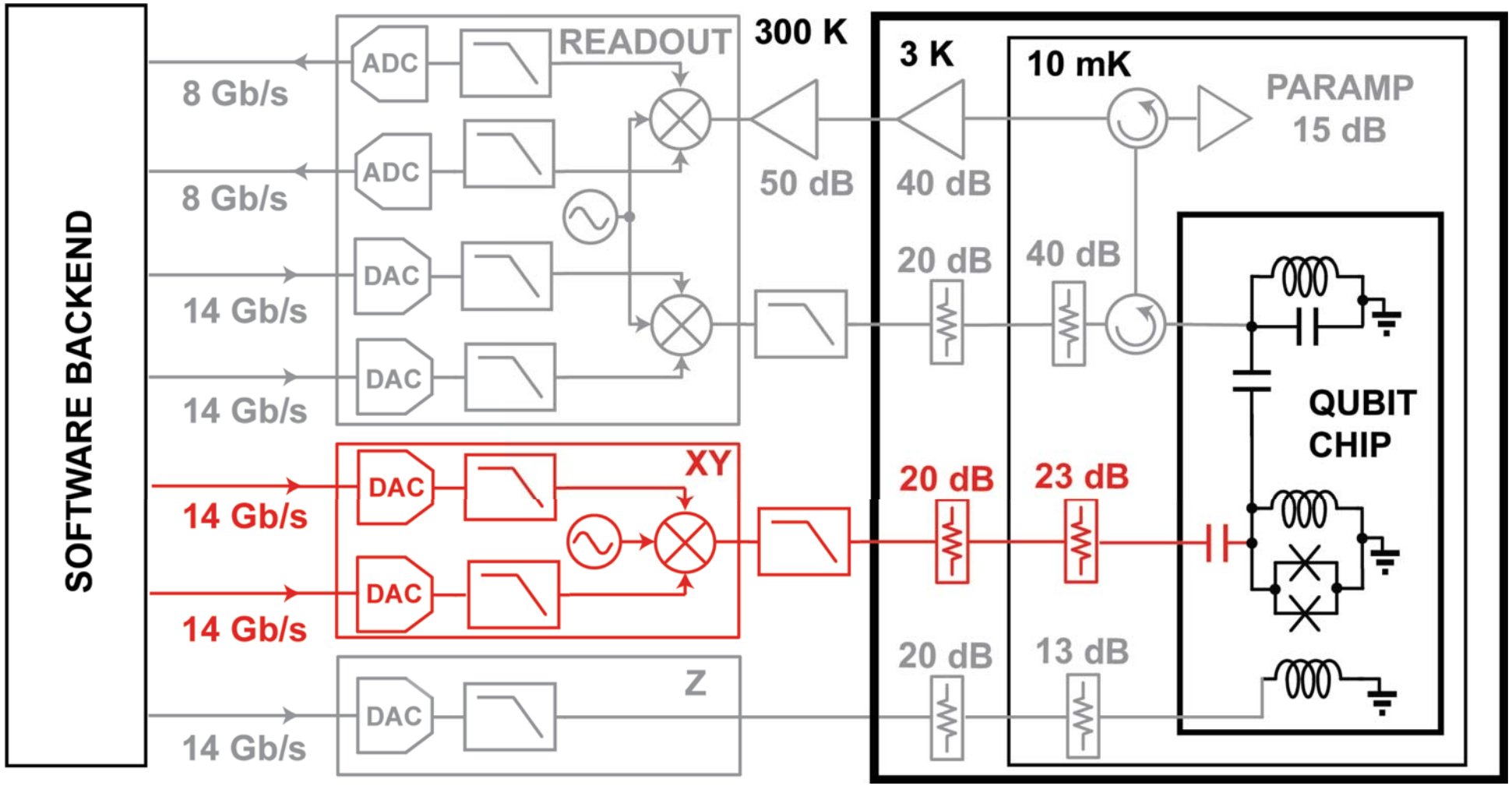
72 qubit quantum processor requires:

- 240 high speed AWGs
- 84 upconverters
- 12 downconverters
- 24 high speed ADCs
- 168 long & lossy coax paths from 300K-to-4K
- 168 superconducting coax (4K-to-10mK)
- >3Tb/s data stream

Brute force approach OK for "small-scale" demo



Typical Single Qubit Control/Measurement Hardware

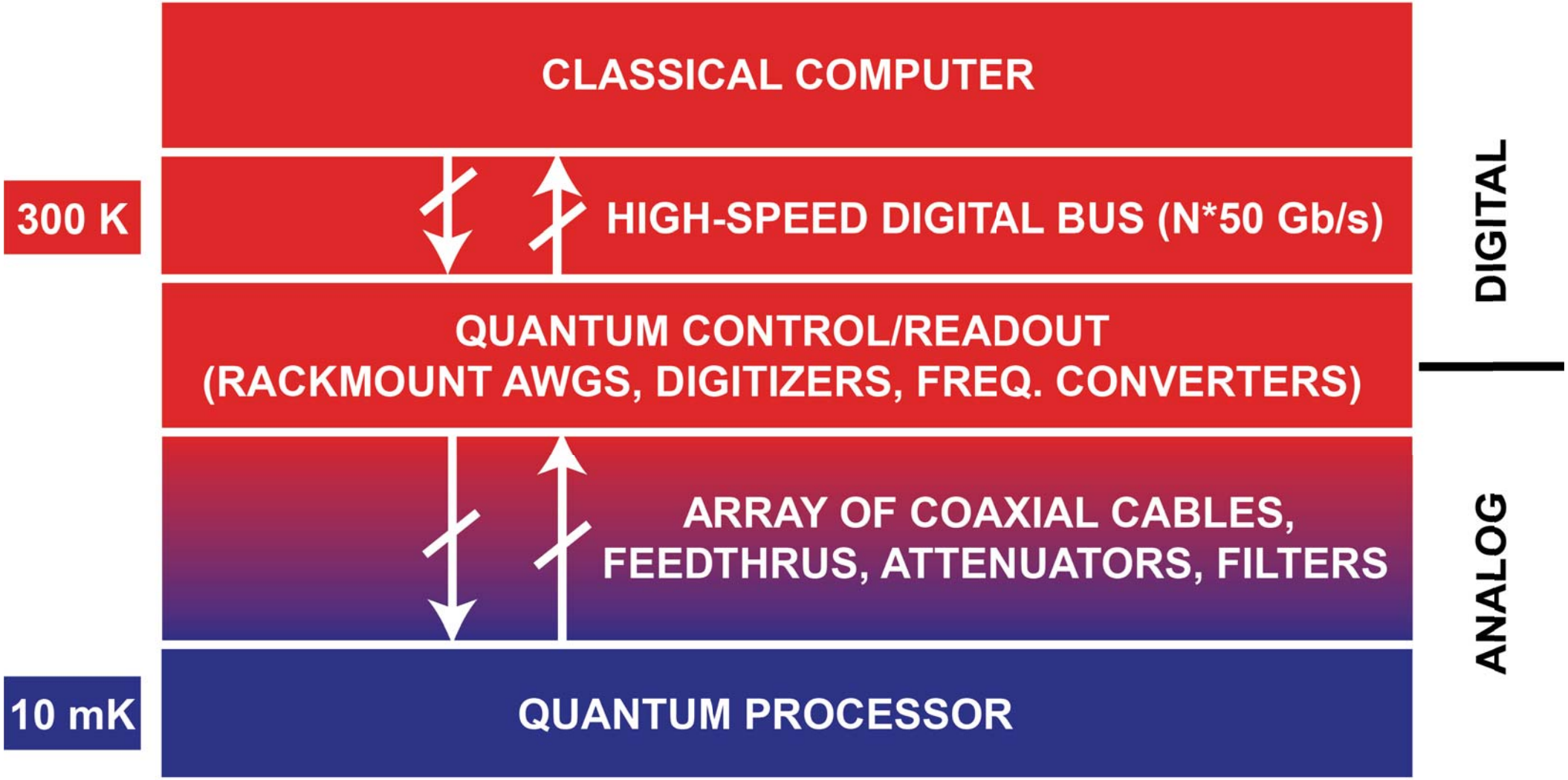


DACs:
14-bit
1Gs/s

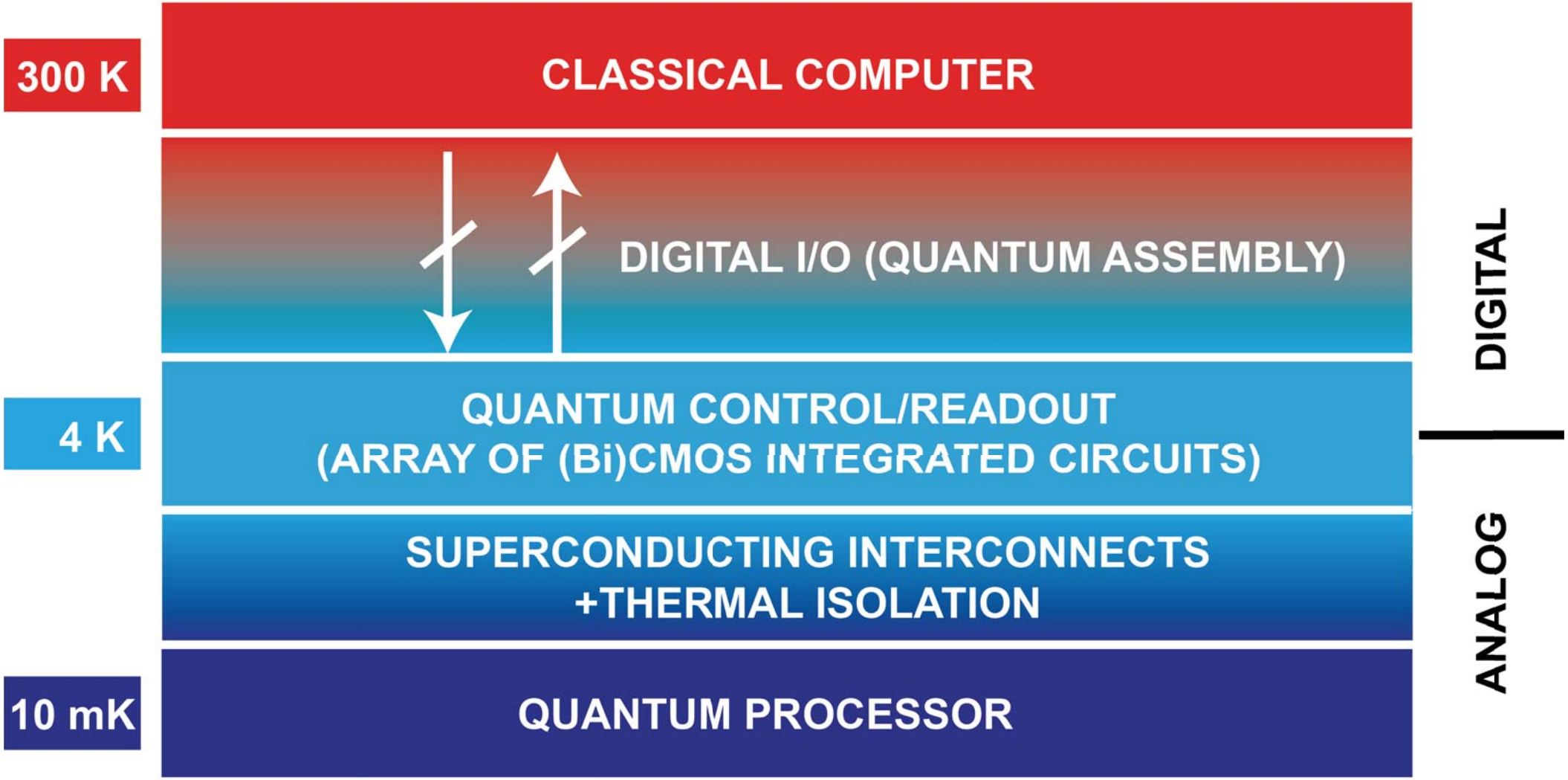
ADCs:
8-bit
1Gs/s

A lot of overhead to control/measure 1 qubit!

Architecture Suitable for 72 Qubit Computer



Possible Hardware Architecture for 1M Qubit System

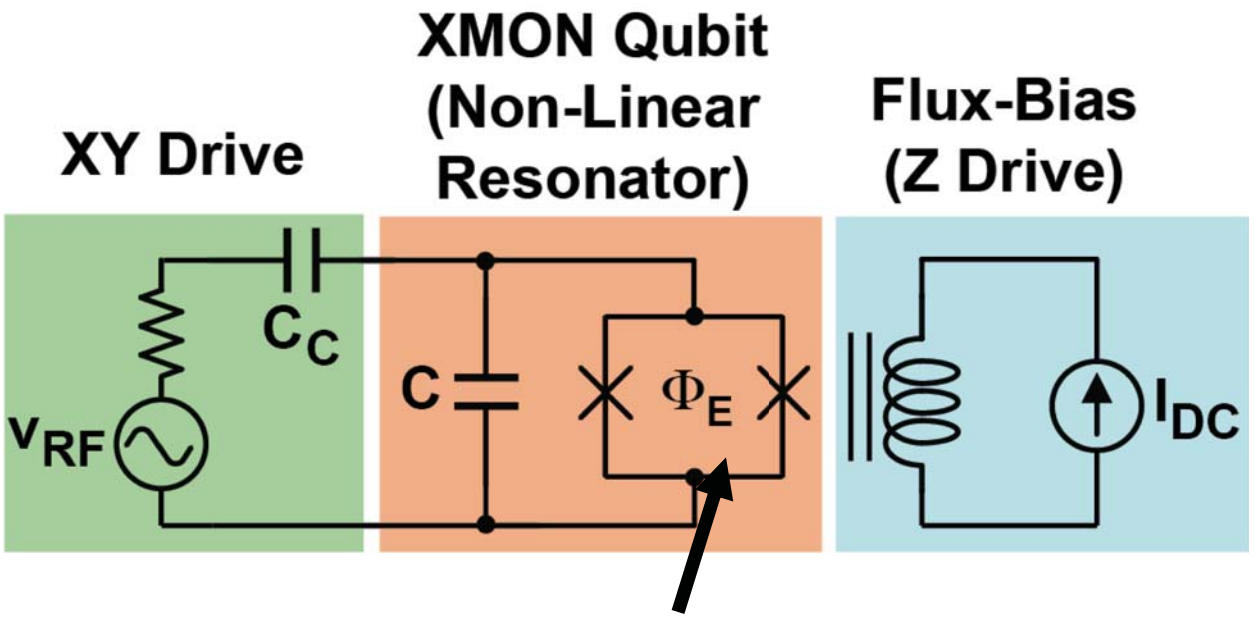


See Charbon ISSCC 2017, Patra JSSC 2018

Outline

- **Transmon Qubit**
- **XYControl of XMON(s)**
- **Cryo-CMOS XY Controller**
- **Experimental Results**
- **Conclusions**

Transmon Superconducting Qubit



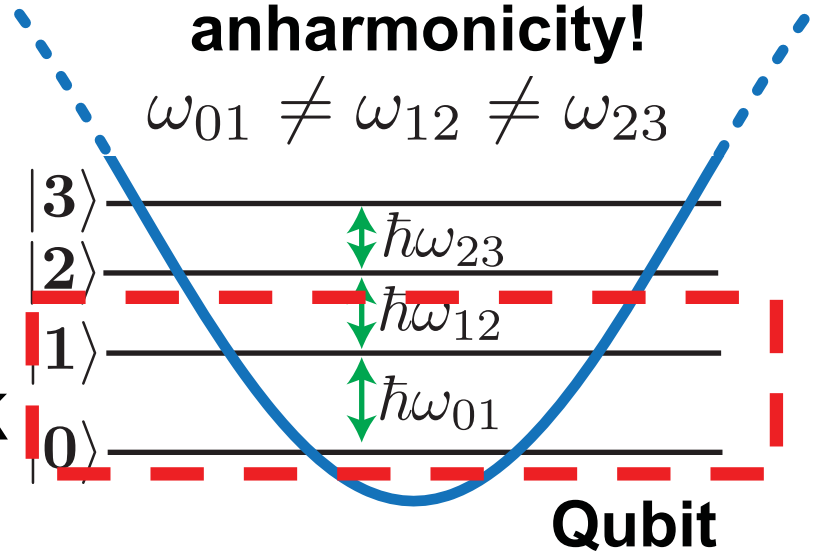
Josephson Junction loop ⇒ flux-tunable lossless nonlinear inductor

$$T \ll \frac{\hbar\omega_{01}}{k}$$

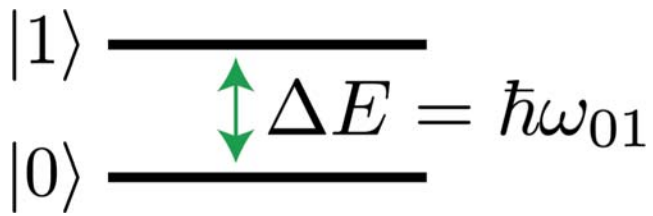
Cool to ~10mK

Nonlinearity creates anharmonicity!

$$\omega_{01} \neq \omega_{12} \neq \omega_{23}$$



Behaves as 2-level qubit if we selectively drive ω_{01}



$$\omega_{01} \approx \frac{1}{\sqrt{L_{\mathrm{J0,e}}(\Phi_{\mathrm{E}})\,C}}$$ **⇒ 4-8GHz**

$$\omega_{01} - \omega_{12} = \frac{q^2}{2\hbar C}$$ **⇒ 0.15-0.35GHz**

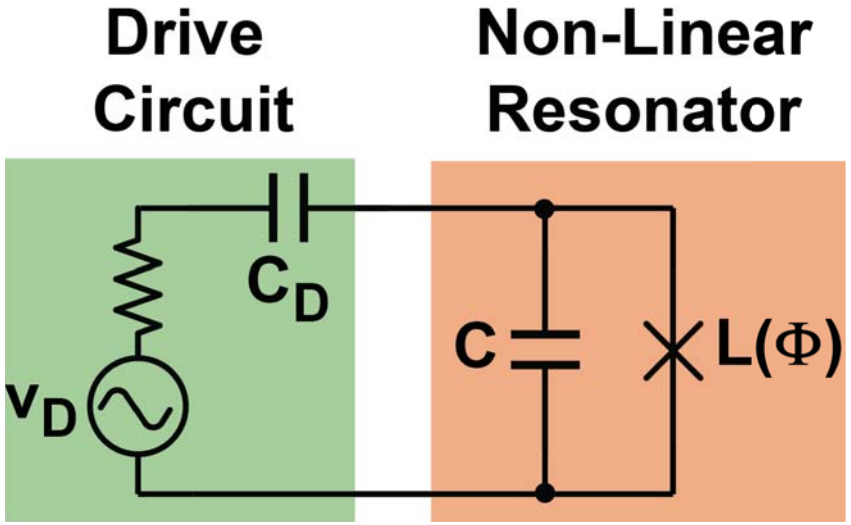
Single Qubit Gate Operations

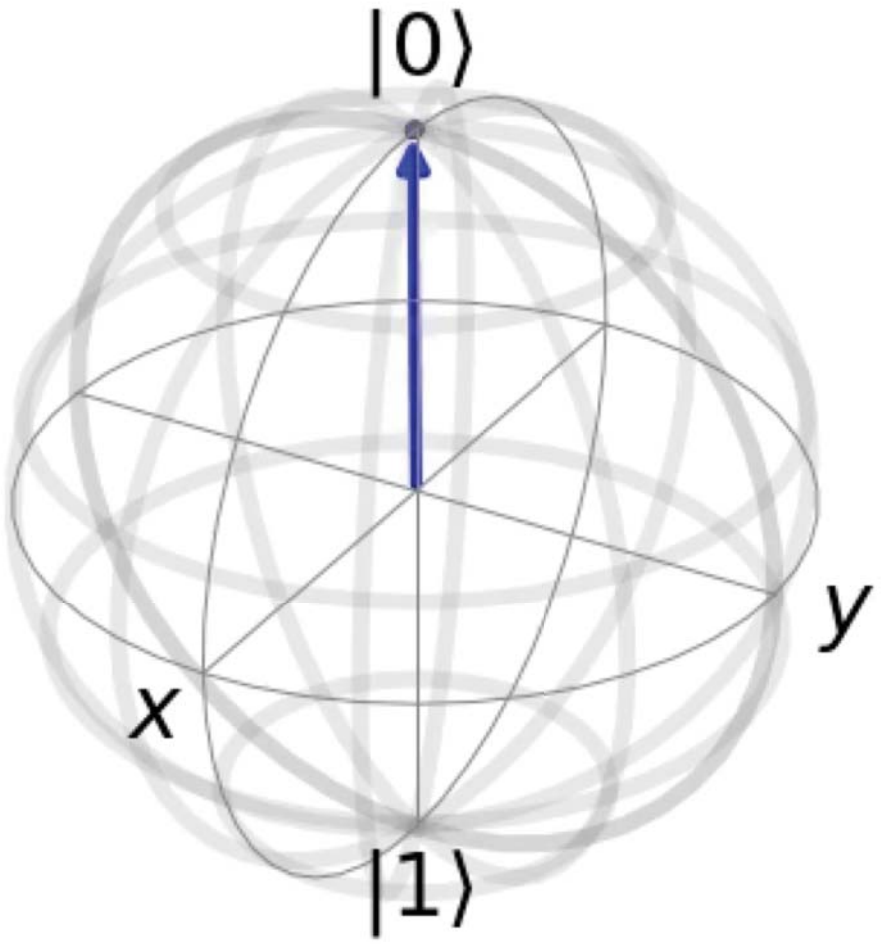
$$|\psi(t)\rangle = \underbrace{\exp\left\{-\frac{j}{\hbar}\int_{t_0}^{t} \hat{\mathrm{H}}(t')\mathrm{d}t'\right\}}_{\hat{\mathrm{U}}} |\psi(t_0)\rangle$$

Rotate about X	Rotate about Y	Rotate about Z
$\hat{\mathrm{H}}_{\mathrm{X}} = \frac{\hbar\omega_{\mathrm{r}}}{2}\hat{\sigma}_{\mathrm{X}}$	$\hat{\mathrm{H}}_{\mathrm{Y}} = \frac{\hbar\omega_{\mathrm{r}}}{2}\hat{\sigma}_{\mathrm{Y}}$	$\hat{\mathrm{H}}_{\mathrm{Z}} = \frac{\hbar\omega_{\mathrm{r}}}{2}\hat{\sigma}_{\mathrm{Z}}$
$\hat{\sigma}_{\mathrm{X}} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \end{bmatrix}$	$\hat{\sigma}_{\mathrm{Y}} = \begin{bmatrix} 0 & -j \\ j & 0 \end{bmatrix}$	$\hat{\sigma}_{\mathrm{Z}} = \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}$

XY Gates **Free Precession/Z Gates**

Driven Transmon ("Lab Frame")





$$\hat{\mathrm{H}}_{\mathrm{D}} = \frac{\hbar\omega_{01}}{2}\left(-\hat{\sigma}_{\mathrm{Z}}\right) + \underbrace{E_0 \cos\left(\omega_{01} t\right)}_{v_{\mathrm{D}}(t)} \sqrt{\frac{\hbar}{2Z_{\mathrm{Q}}}} \frac{C_{\mathrm{D}}}{C} \hat{\sigma}_{\mathrm{Y}}$$

Precession about -Z

Rotation about Y

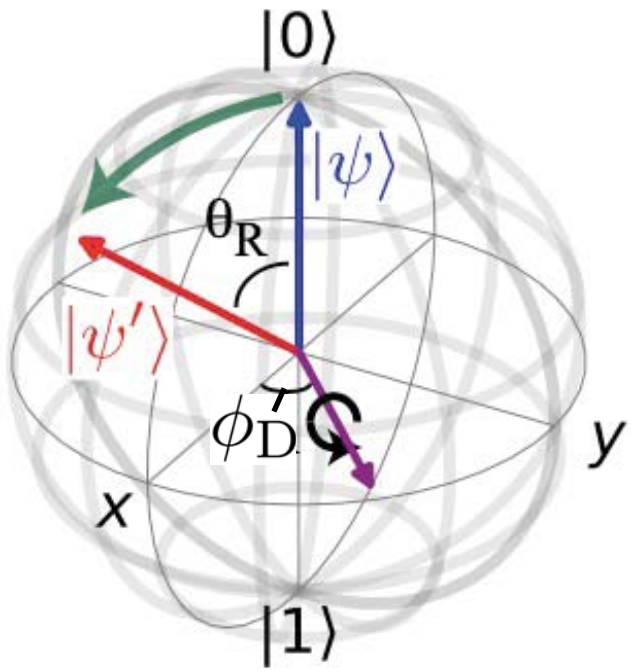
Driven Transmon in Rotating Frame (RWA)

- **Drive qubit at ω_{01}**

$$v_{\mathrm{D}}(t) = e(t)\sin(\omega_{01}t + (\pi - \phi_{\mathrm{D}}))$$

- **Neglect 2*w01 term (rotating wave approx.)**

$$\hat{\mathrm{H}}_{\mathrm{RWA,D}}(t) = \frac{e(t)}{2}\sqrt{\frac{\hbar}{2Z_{\mathrm{Q}}}}\frac{C_{\mathrm{D}}}{C}\left(\cos(\phi_{\mathrm{D}})\,\hat{\sigma}_{\mathrm{X}} + \sin(\phi_{\mathrm{D}})\,\hat{\sigma}_{\mathrm{Y}}\right)$$



Amount of rotation: integrated envelope amplitude

Axis of rotation: carrier phase (ϕ_R=ϕ_D)

How to pick e(t)?

Tradeoff Between Coherence Time & Gate Duration

Gate time (avoid ω_{12}) $$\omega_{12} - \omega_{01} = -\frac{q^2}{2\hbar C}$$

- Smaller C enables faster gates!

Relaxation time (T1) $$T_1 \approx \frac{Q_L}{\omega_{01}}$$

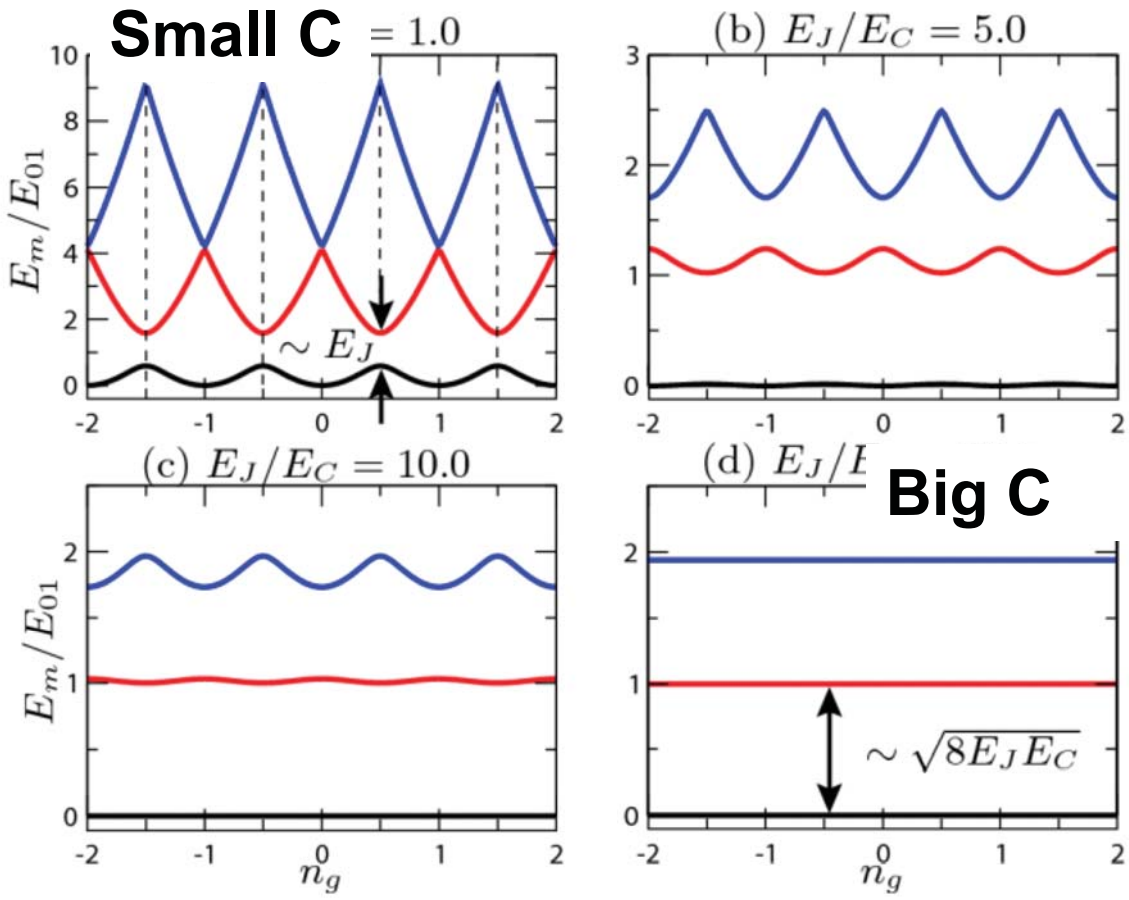
- Higher Q and lower frequency

Dephasing time (T2)

- Minimize effect of charge noise (1/f). Big C for small charge dispersion

1/2Q gates typically: 10-20ns & 50ns

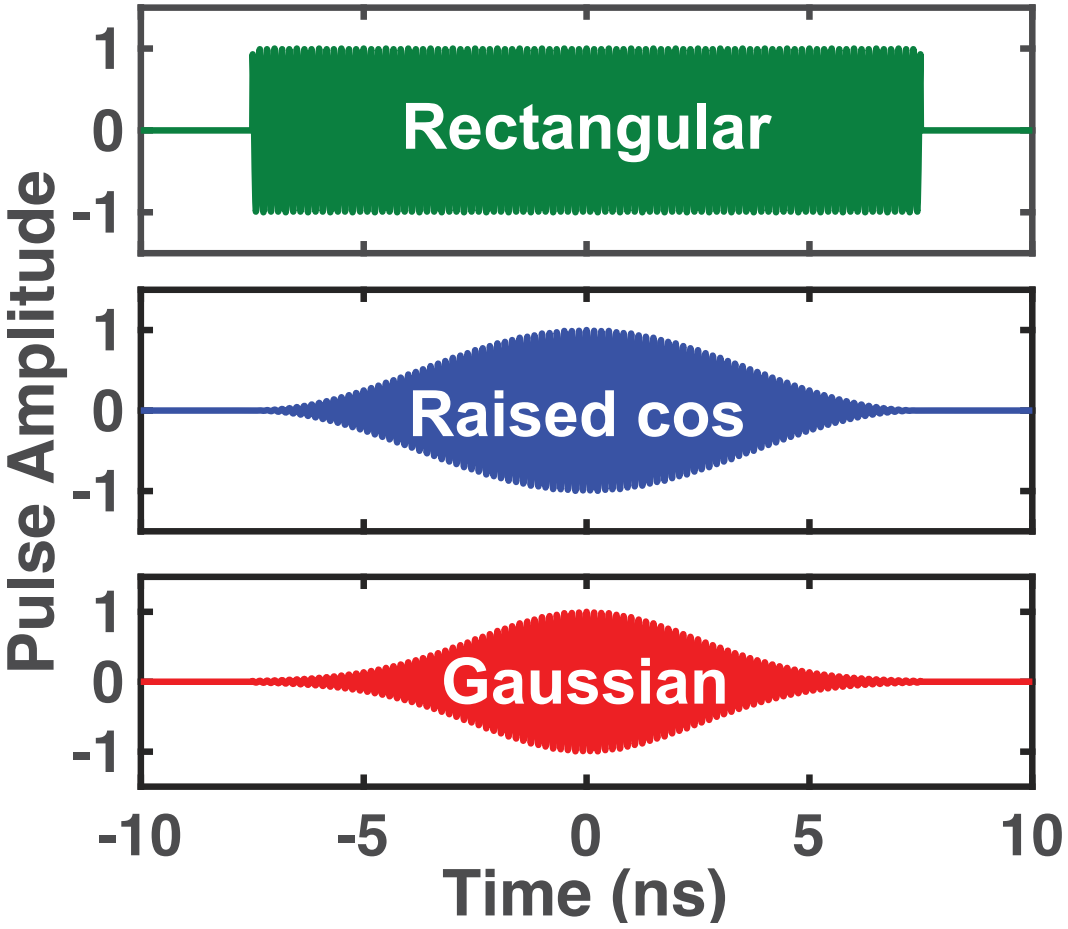
Coherence time 30-100us.

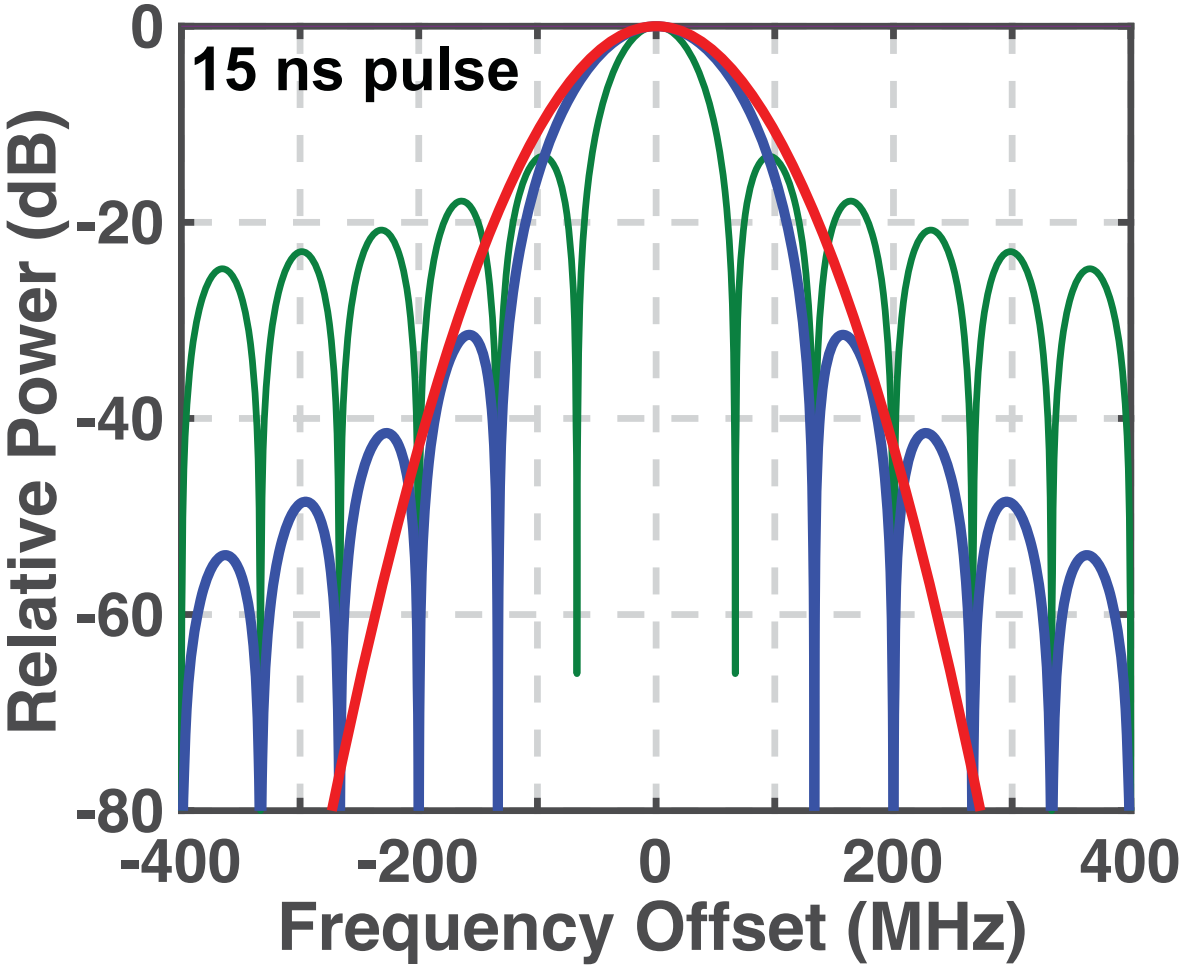


Koch, Phys. Rev A, 2007

>1000 Gates/Coherence time (limiting SQ and 2Q fidelities to ~99.99% and ~99.9%)

Pulse Shaping to Avoid ω_{12} Transition





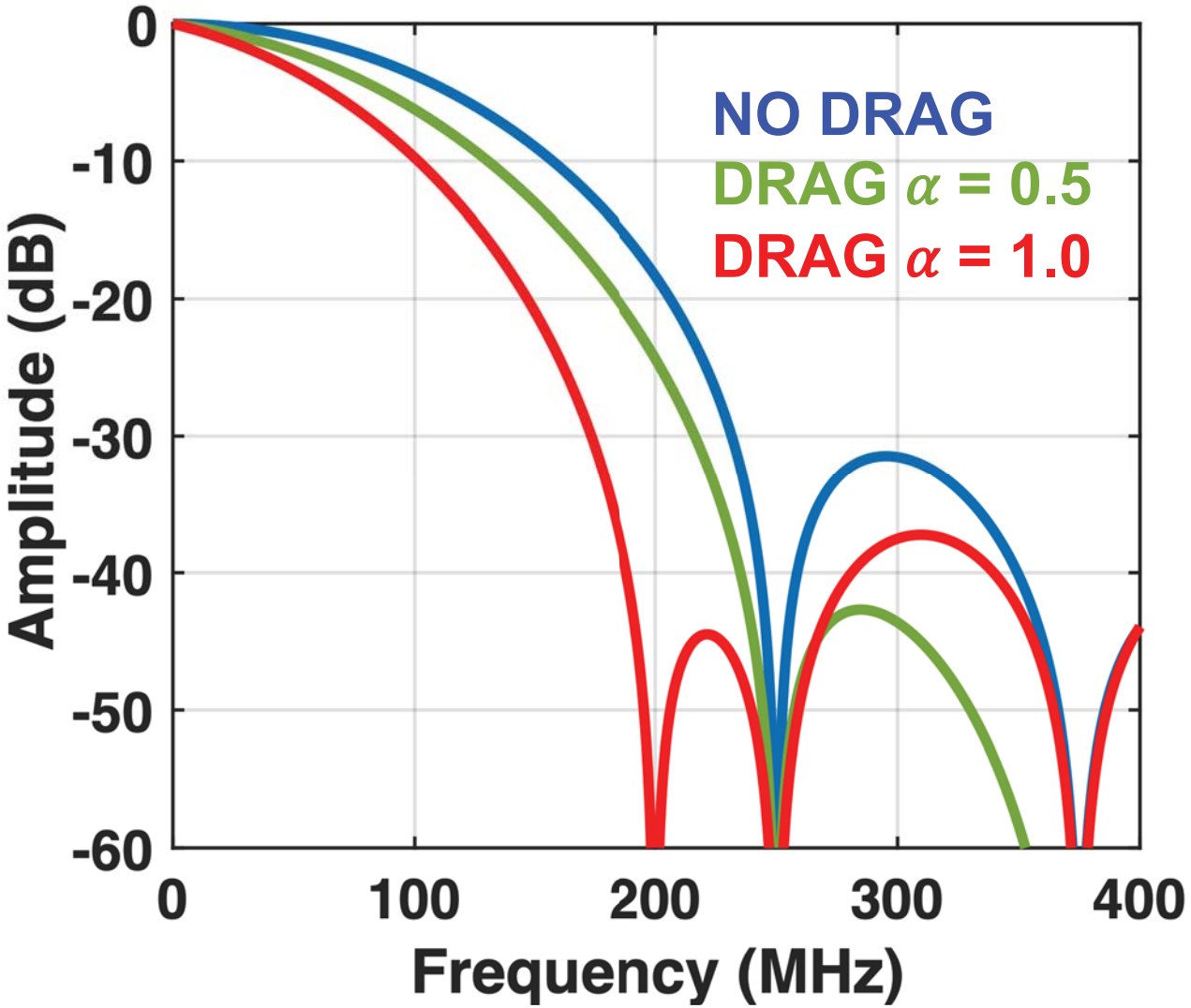
Raised cosine: good compromise between sidelobes and pulse duration

Higher-Order Envelope Shaping

- Shortcomings of basic envelope shaping:
  1. Pulses still too-long
  2. AC stark shift (dynamic qubit detuning)
- DRAG used to reduce pulse duration

$$e'(t) = e(t) + j\frac{\alpha}{\eta}\dot{e}(t)$$

- Amplitude-dependent frequency detuning to remove AC Stark effect
- >99.9% fidelity possible



Drive Strength (pi-pulse)

$$\hat{\mathrm{H}}_{\mathrm{RWA,D}}(t) = \frac{e(t)}{2}\sqrt{\frac{\hbar}{2Z_{\mathrm{Q}}}}\frac{C_{\mathrm{D}}}{C}\left(\cos(\phi_{\mathrm{D}})\,\hat{\sigma}_{\mathrm{X}} + \sin(\phi_{\mathrm{D}})\,\hat{\sigma}_{\mathrm{Y}}\right)$$

Rotation Angle

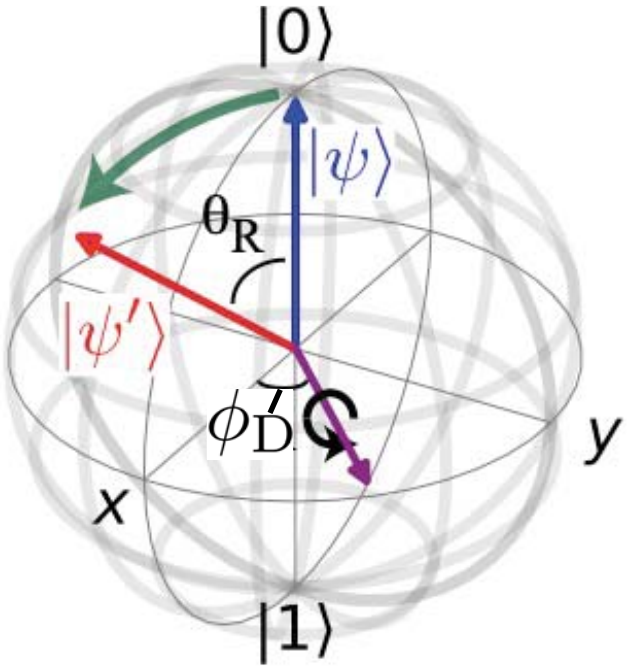
$$\theta_{\mathrm{R}} = \sqrt{\frac{\hbar}{2Z_{\mathrm{Q}}}}\frac{C_{\mathrm{D}}}{C}\int_{t_0}^{t} e(t')\,\mathrm{d}t'$$

$$\theta_{\mathrm{R}} = \pi$$

Raised cos env.
amp=E_0, duration=Δt

$$\int_0^{\Delta t} e(t)\,\mathrm{d}t = E_0\frac{\Delta t}{2}$$

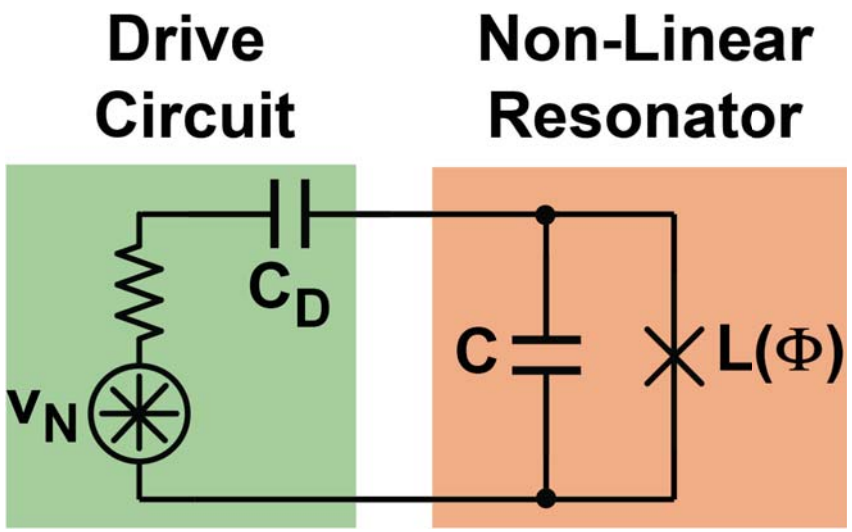
$$E_0 = 2\pi\frac{C}{C_{\mathrm{D}}\Delta t}\sqrt{\frac{2Z_{\mathrm{Q}}}{\hbar}}$$



E_0 typically 50-500 μV at qubit drive port

Noise Floor

Noise on drive line can excite transitions



Effective generator noise temp

$$R_{\uparrow\downarrow} = 2\pi \frac{T_e(f_0)}{T_{\text{Photon}}} \Delta f$$

$$\frac{f_{01}}{Q_D}$$

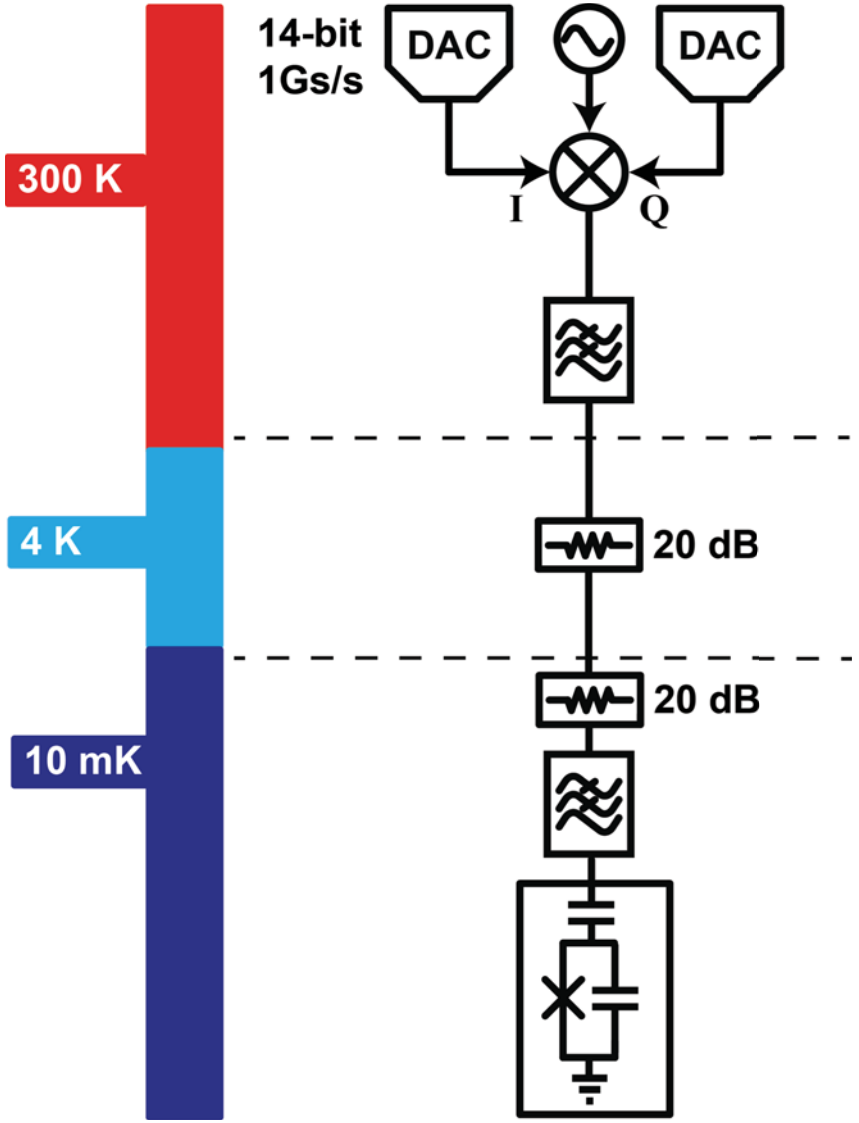
Transition rate

Effective temperature of photon at f_0 (50mK/GHz)

Noise temp on drive line << T_{photon}

Typical Approach

- Standard approach: Baseband AWG + SSB up-conversion
- Challenges/Limitations
  - LO feedthrough
  - Data rate >> information bandwidth
  - Synchronization
  - Interconnect density



Outline

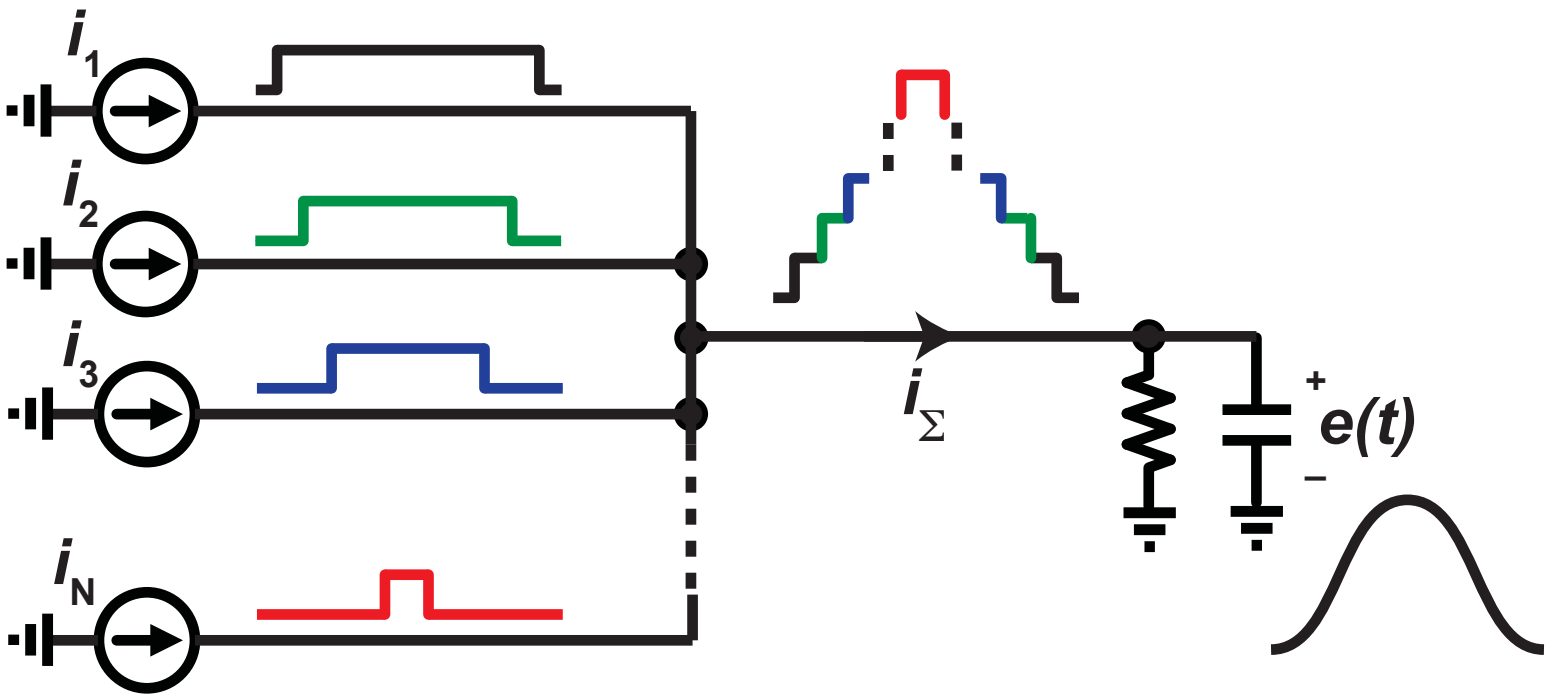
- Transmon Qubit
- XY Control of XMON(s)
- Cryo-CMOS XY Controller
- Experimental Results
- Conclusions

Cryo-CMOS XY Controller Specifications

Key design challenges: (1) No device models for 3K (2) dissipation

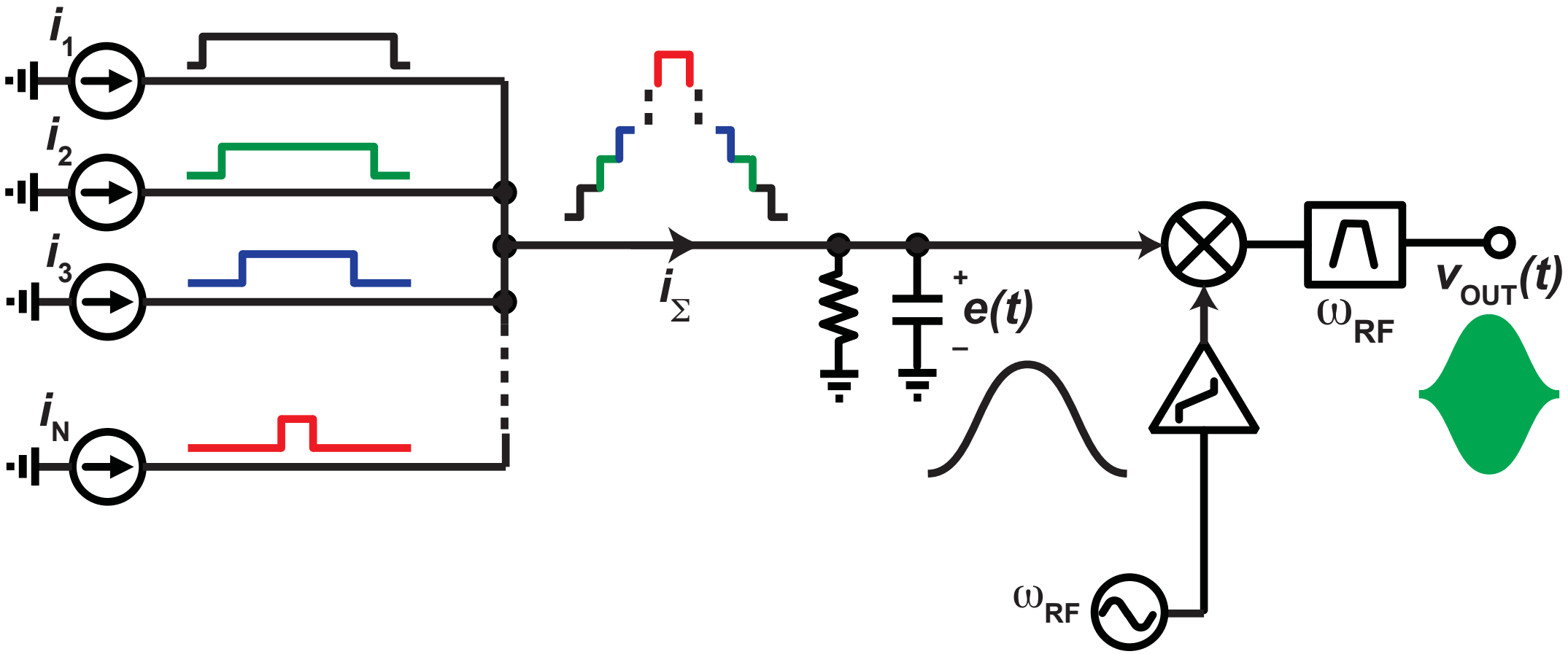
	Driving Parameter	Long Term	Gen 1 XY IC
Phys Temp	Superconducting cables	≤4.2K	**3K**
AC+DC PWR	Cryocooler heat lift	≤0.3mW	**Few mW**
Carrier	Qubit frequency range	TBD	**4-8GHz**
Pulse amp	Qubit coupling, design uncertainty	≥1mV	**≥10mV**
Instruction set	Algorithm	TBD	**4-bit**
Env Type	Error Rates	DRAG+	**No DRAG**
Pulse dur. (T_G)	1-2 leakage & coherence time	10ns	**10-30ns**
Pulse BW	1-2 leakage	≤200 MHz	**≤200 MHz**
ENV Error	Assoc. error rates < 0.01%	≤0.25%	**≤0.25%**
Phase Error	Assoc. error rates < 0.01%	≤1°	**≤1°**

Waveform Generation Approach



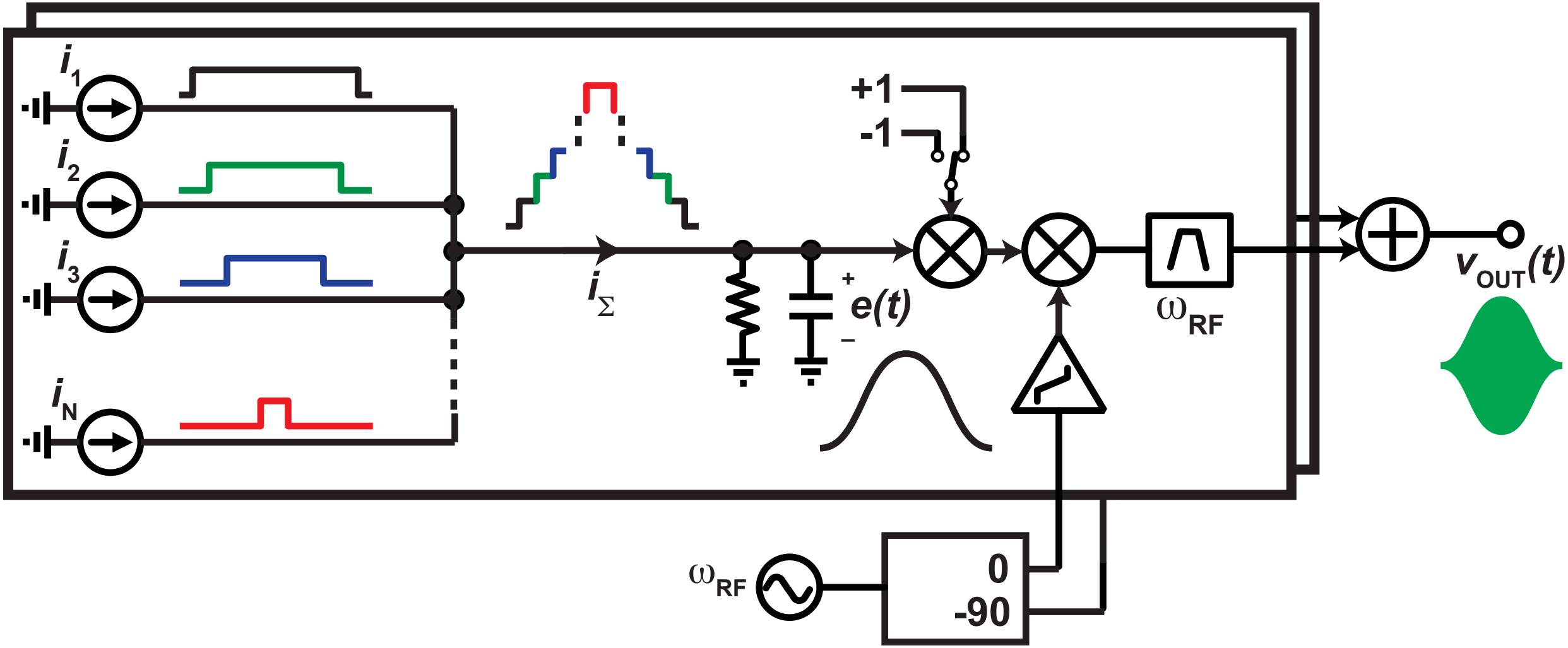
Symmetric envelope generated using superposition of current sources

Waveform Generation Approach



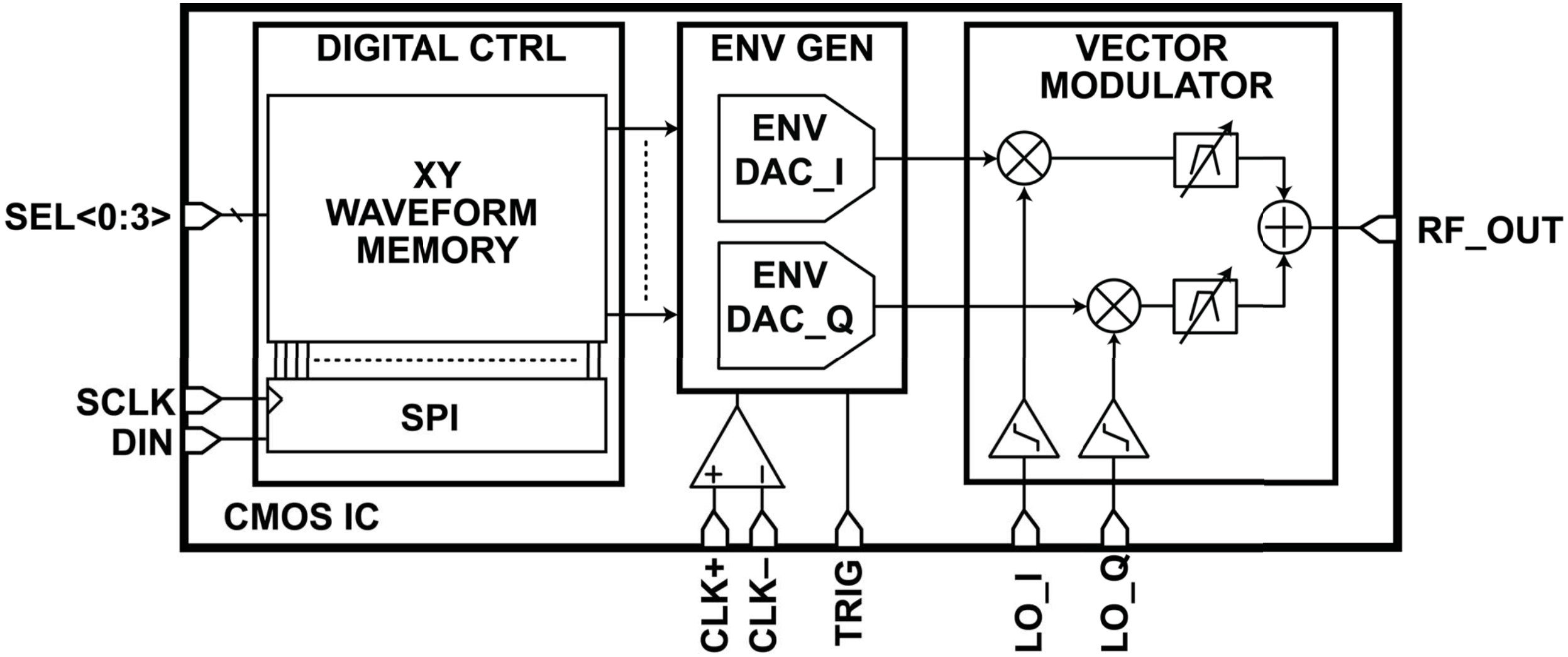
Mix with RF carrier frequency (direct conversion)

Waveform Generation Approach

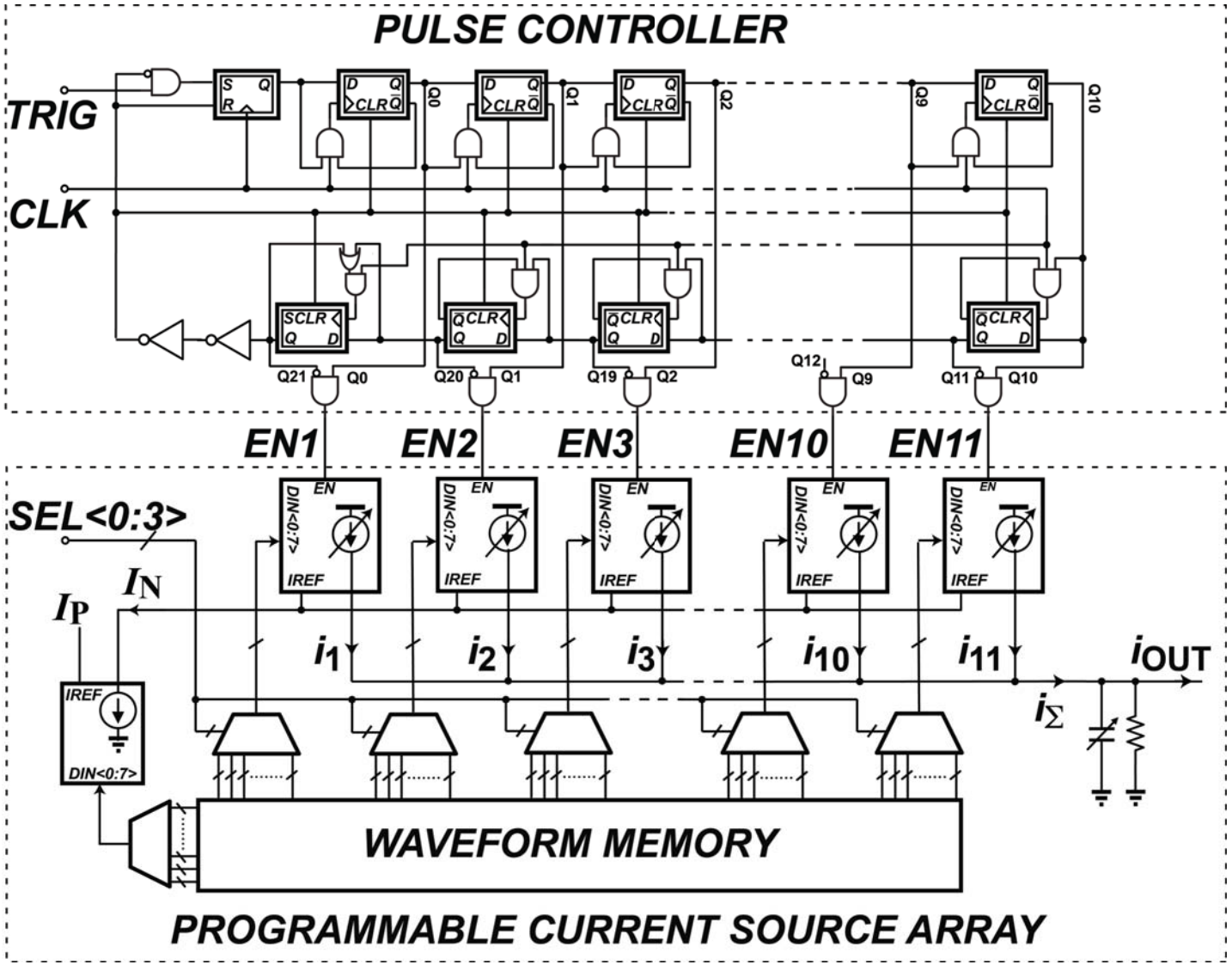


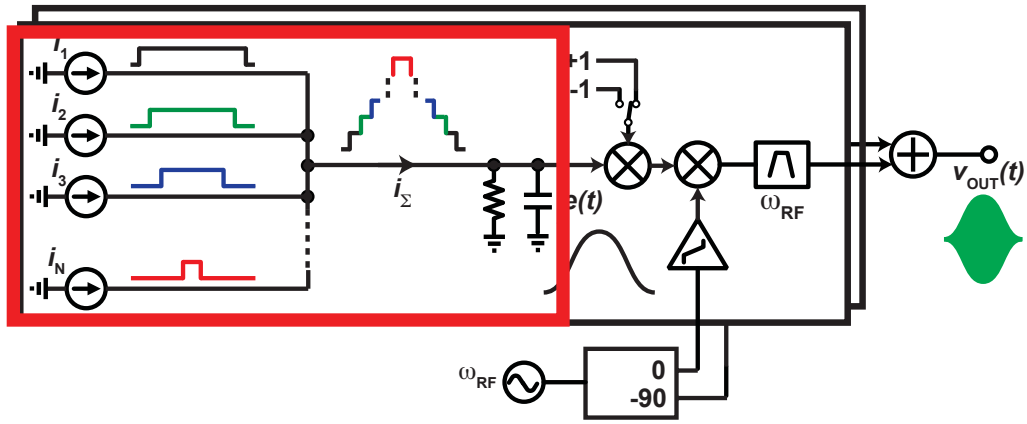
Add quadrature channel and phase switch for full 360° range of carrier phase

Block Diagram



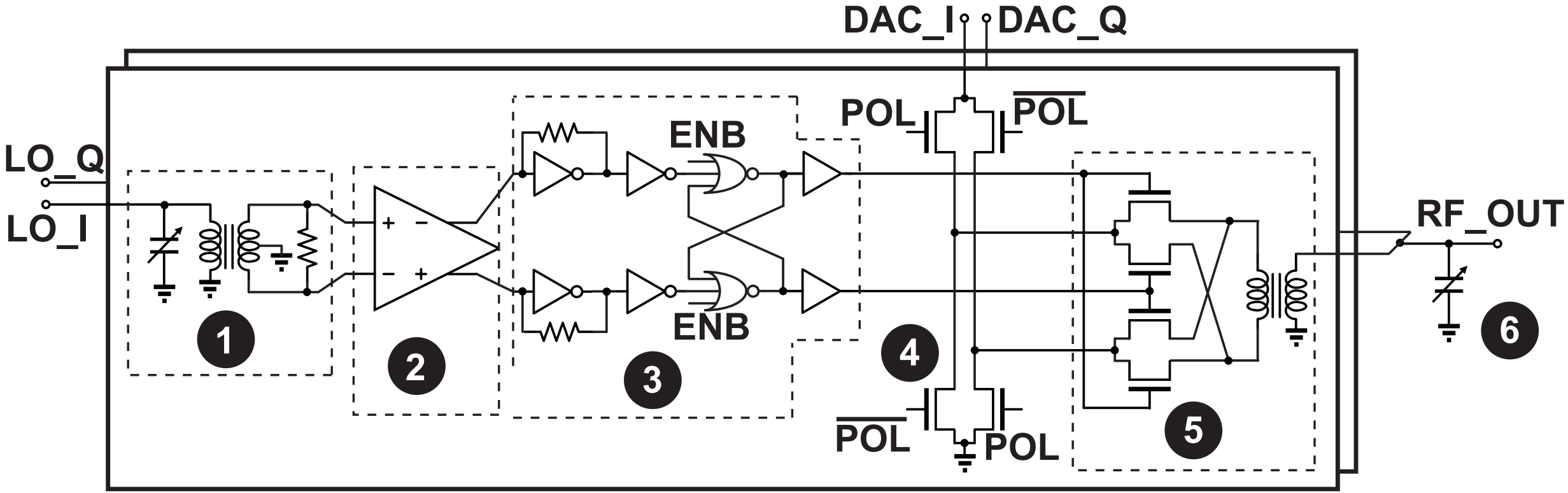
Envelope DAC





- 11 8-bit current sources to define env shape
- 8-bit reference for env amplitude
- 4-bit XY instruction set

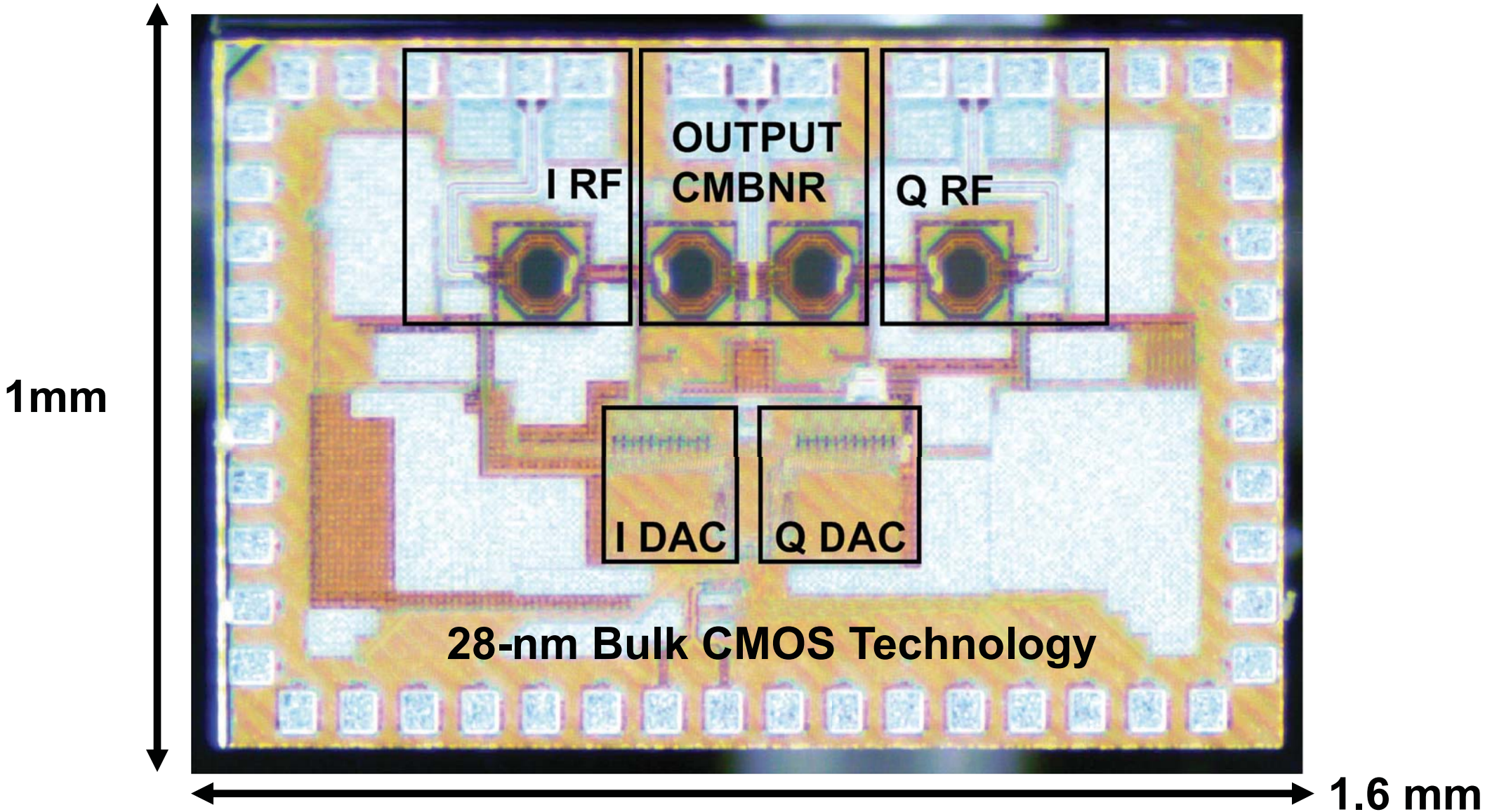
Vector Modulator



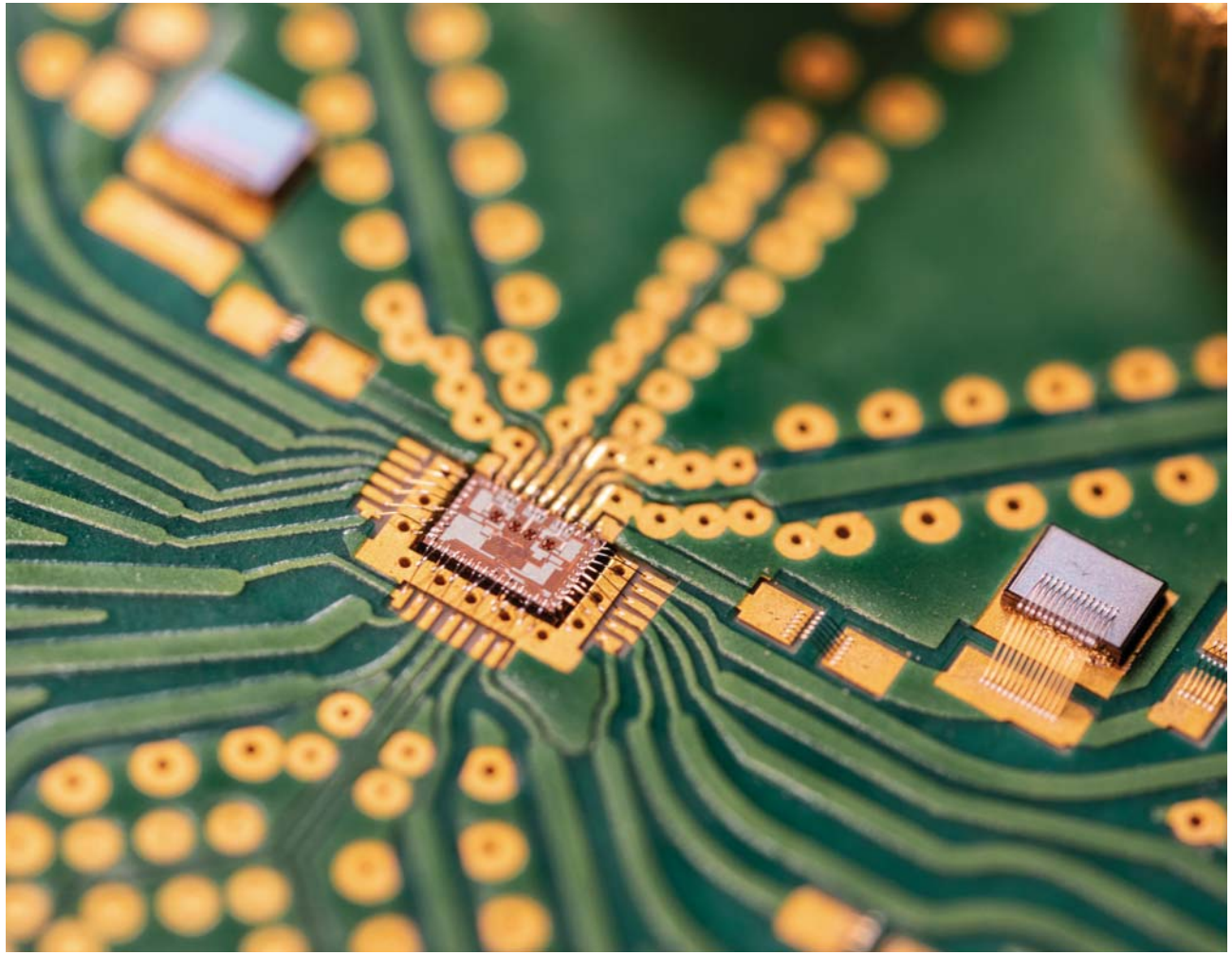
Designed for 4-8 GHz and < 0.5mW/channel w/LO below -13dBm

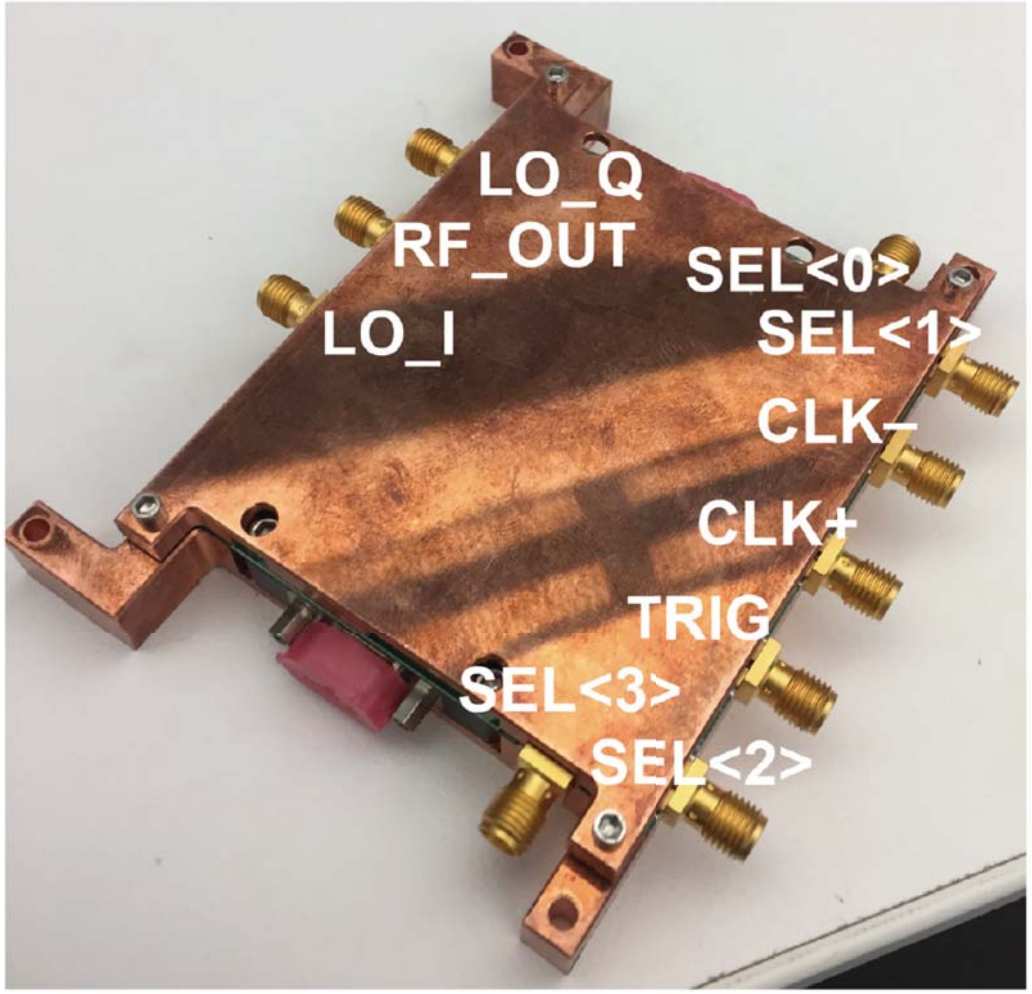
1. Tunable balun
2. Diff. amp for CMRR
3. Std. cell based amp chain
4. Polarity switch
5. XFRM coupled passive mxr
6. XFRM tuning

Die Photo

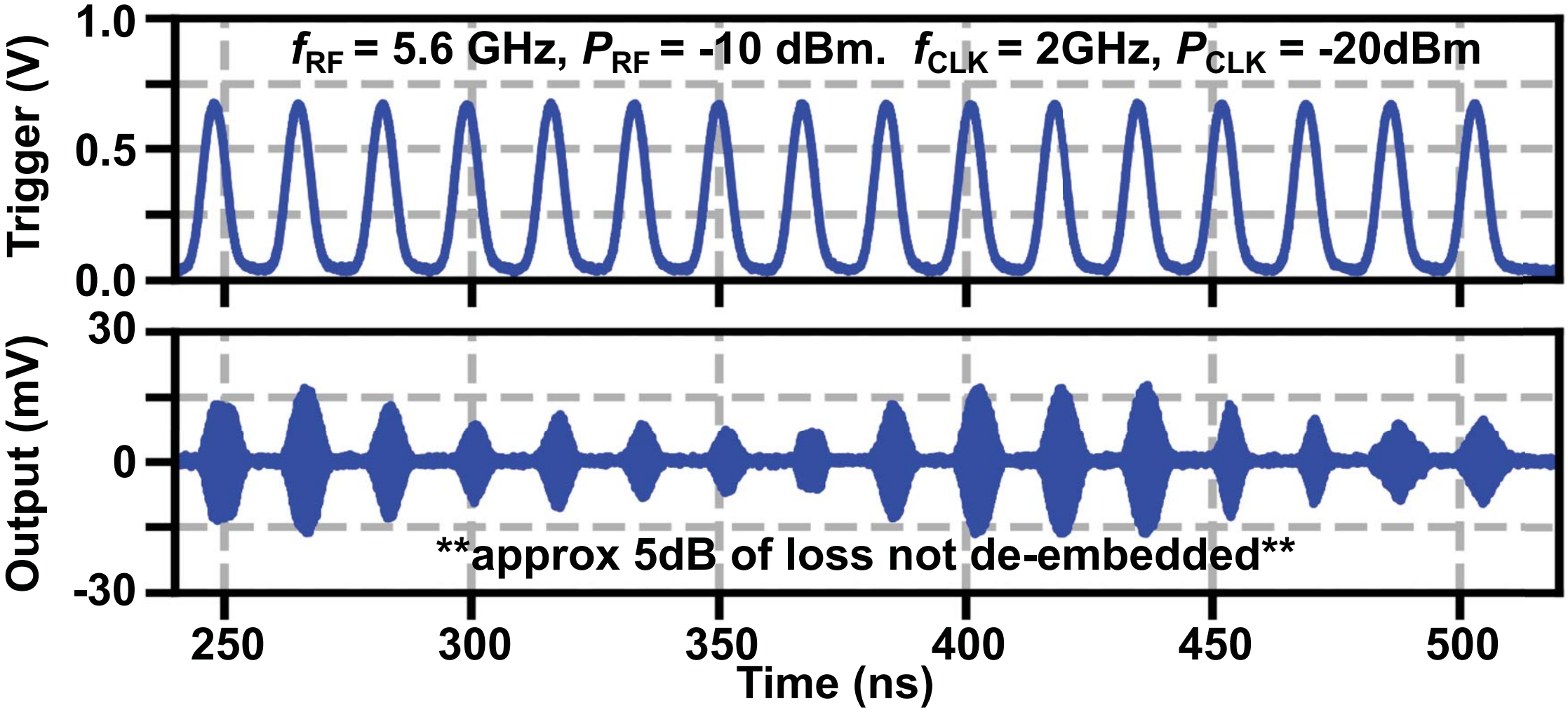

I RF
OUTPUT
CMBNR
Q RF
I DAC
Q DAC
28-nm Bulk CMOS Technology
1mm
1.6 mm

Packaging



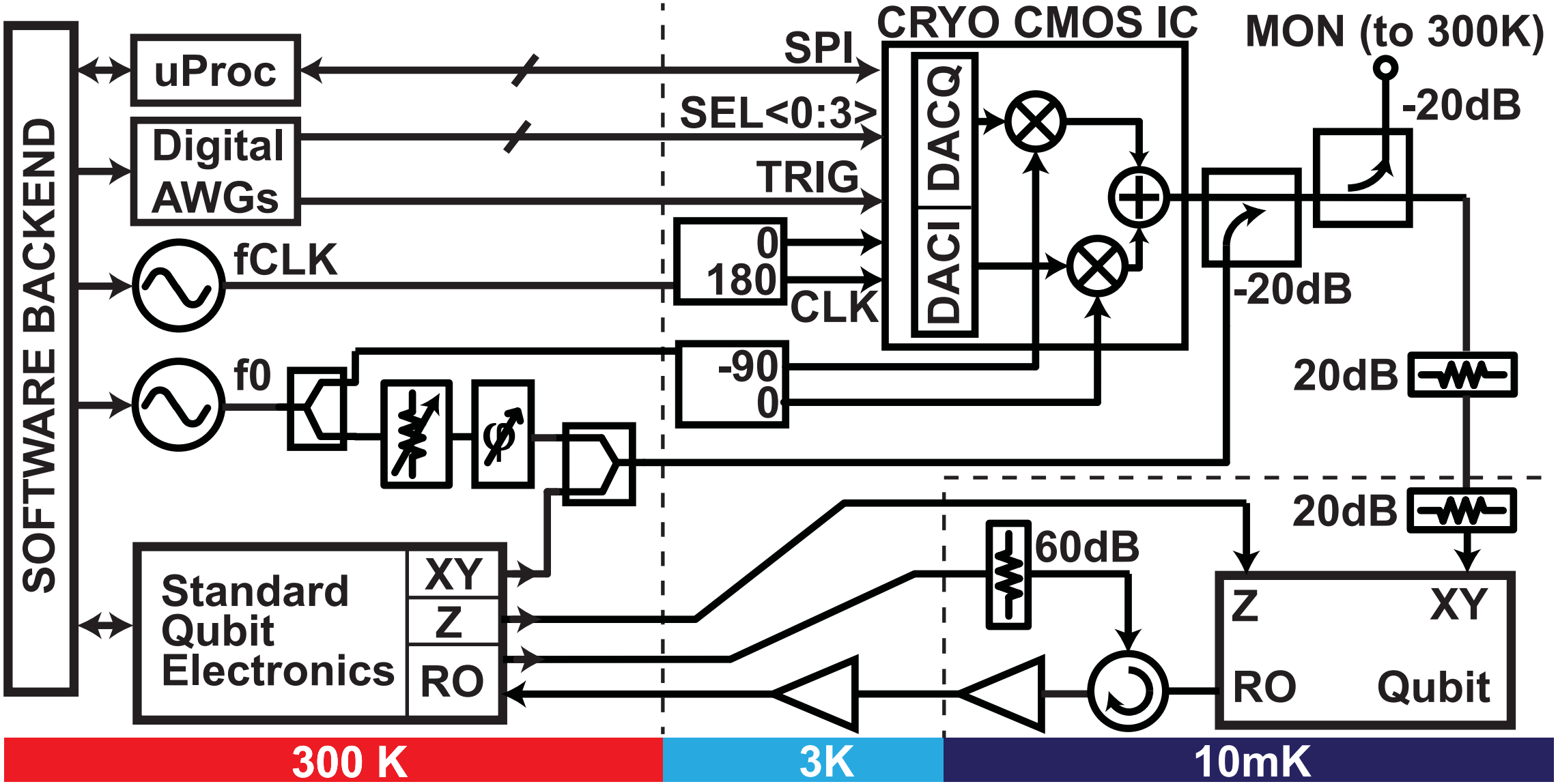


Example Room Temperature Measurements

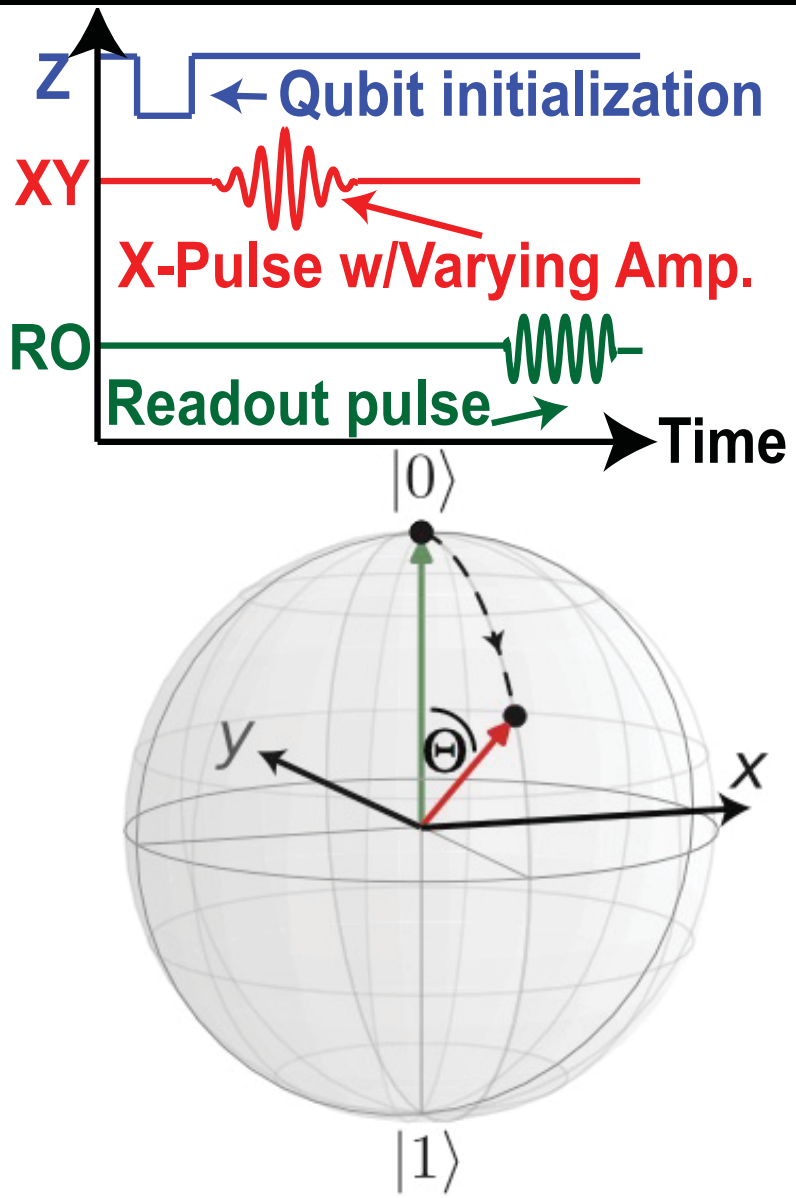


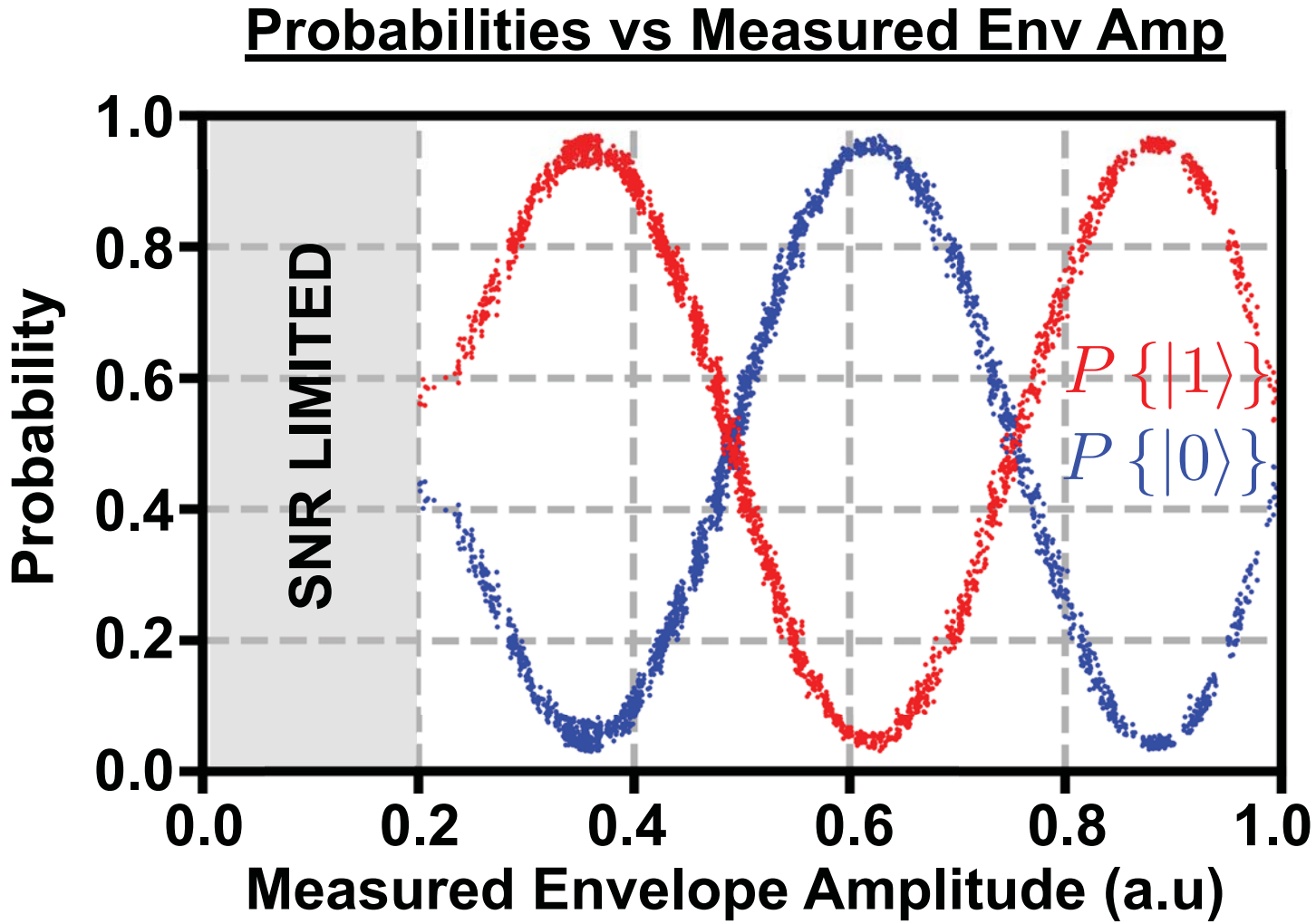
Works w/RF and CLK signals from 4-8 GHz & 0.3-3 GHz, respectively

Integration into Quantum System for Experiments

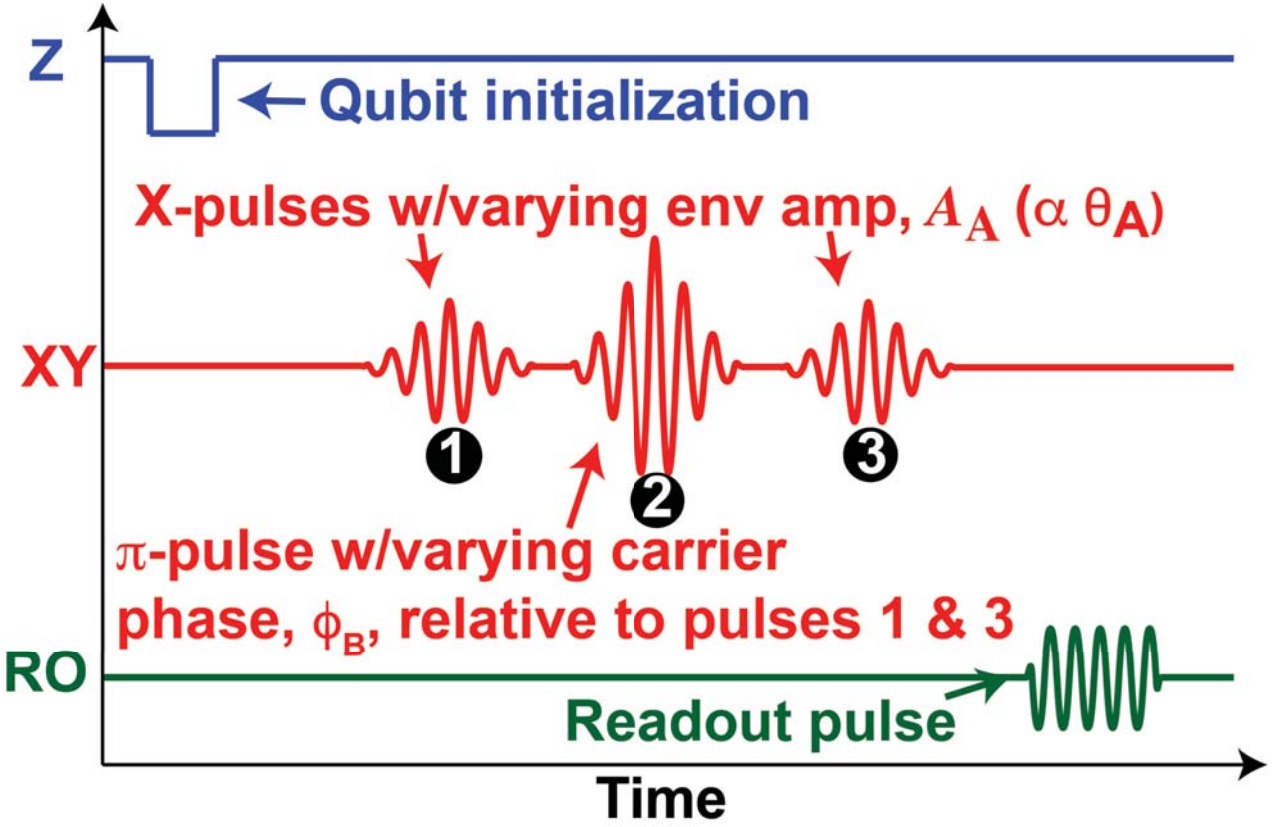


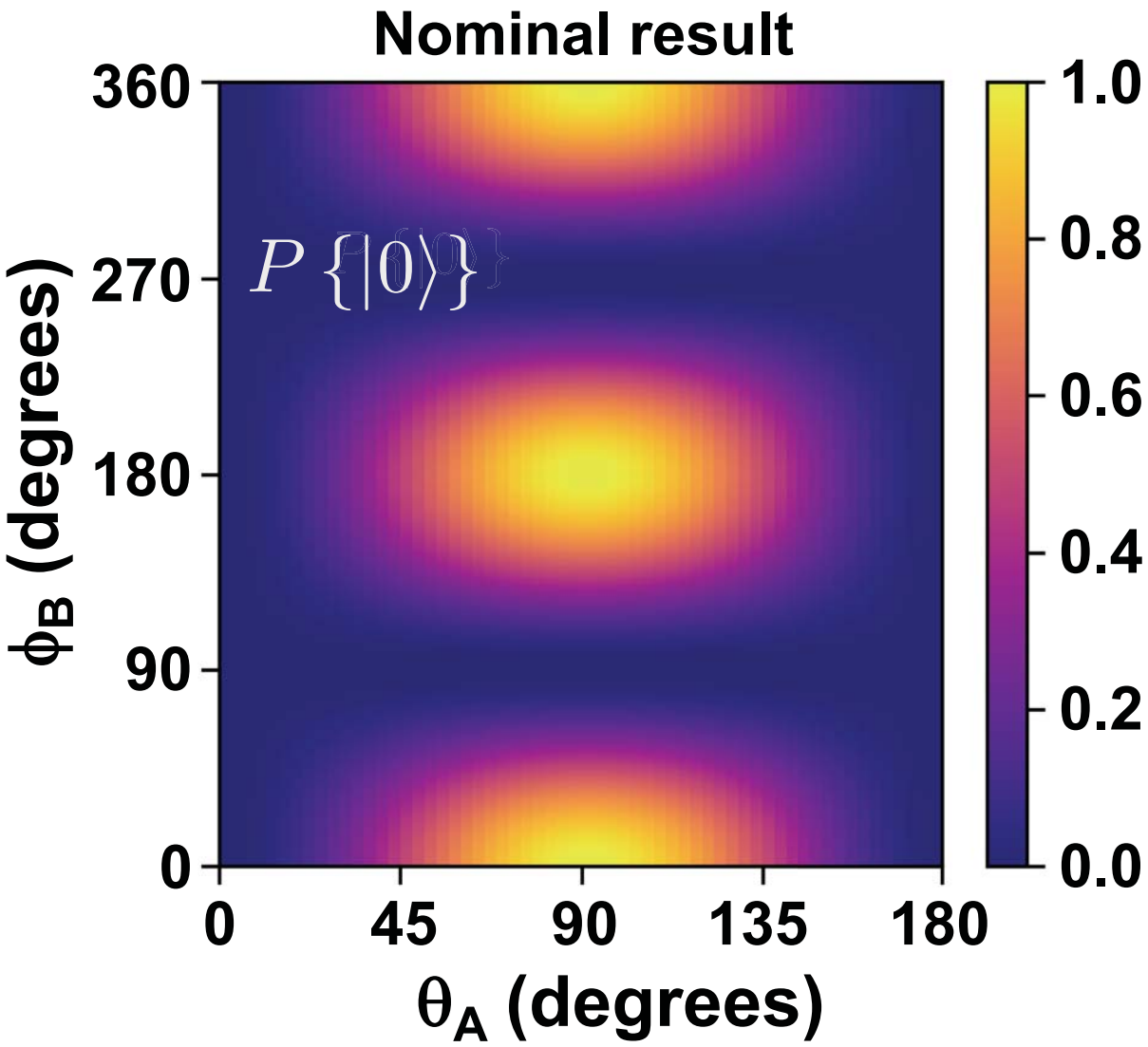
Rabi Experiment (22ns Pulse)



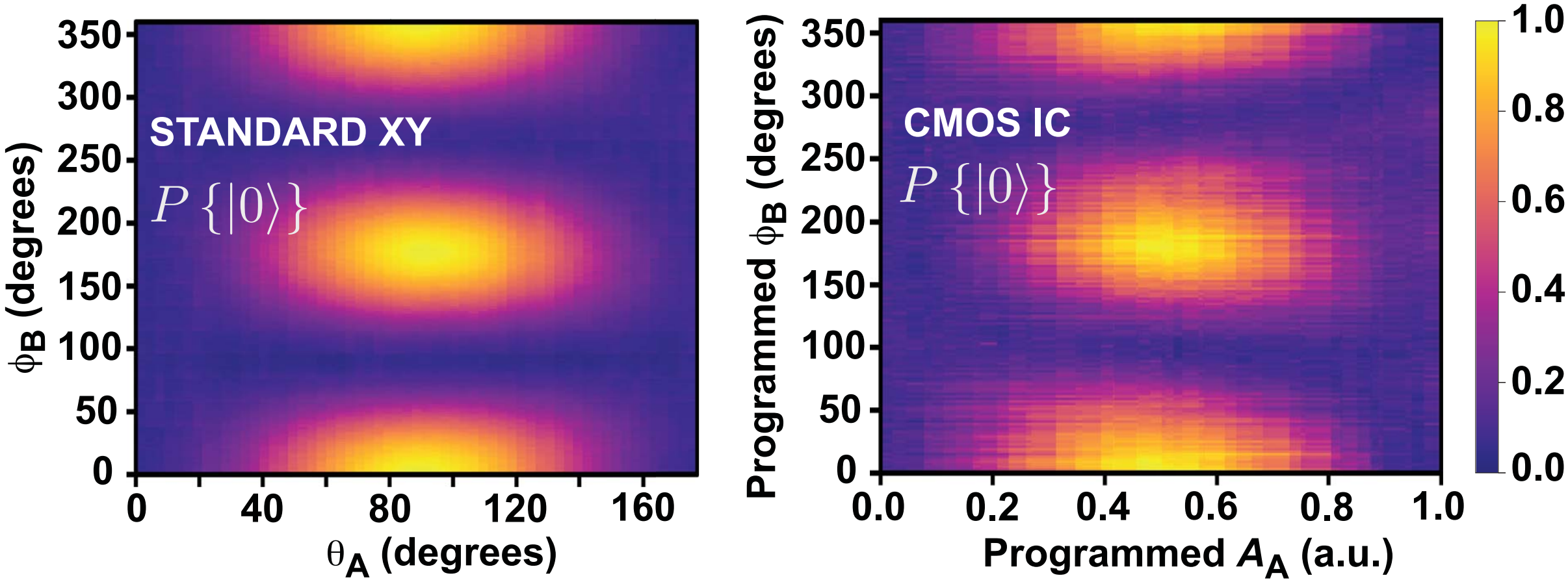


Three-Pulse Experiment





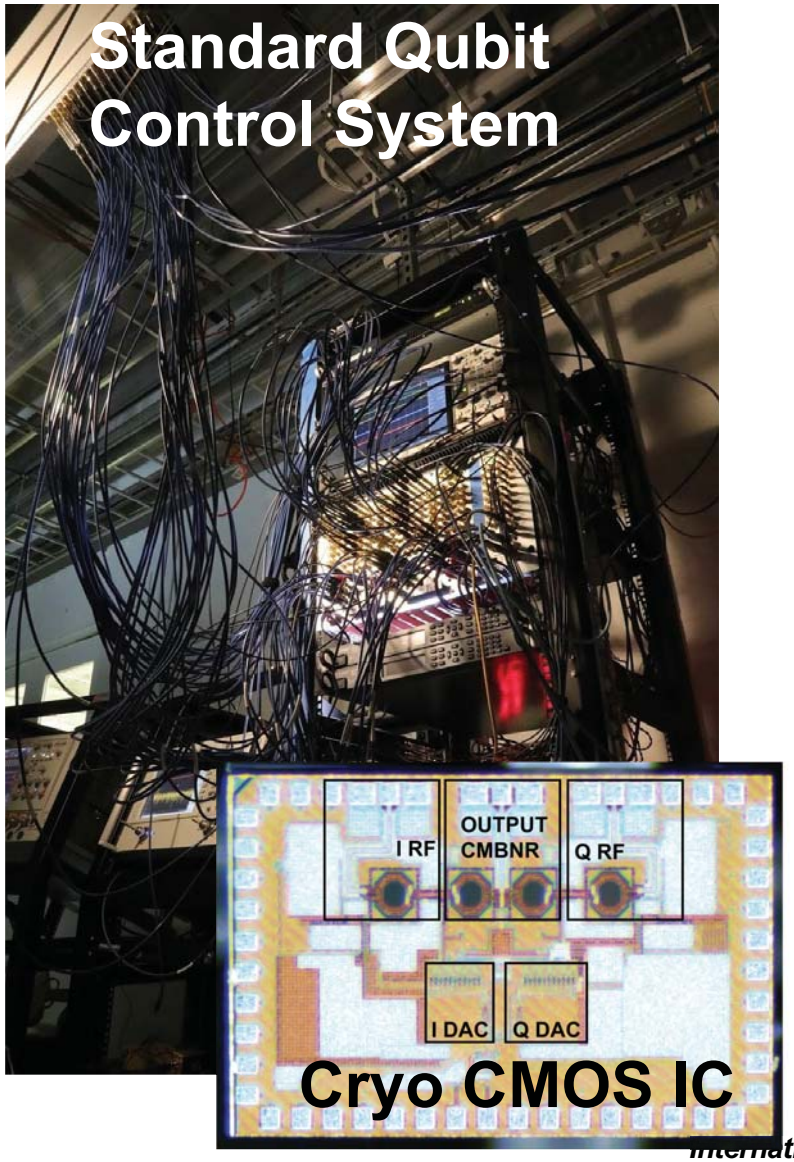
Three-Pulse Experiment Results



22ns Pulses

X & Y axis for CMOS IC have not been calibrated

Comparison w/state of the art



	Standard	Cryo CMOS
Form Factor	Rack Mount	IC
Physical Temp	300 K	**3 K**
Update Rate	1 Gsps	1 Gsps
Instruction Set	N/A	**4-bit**
Dig. Data Rate	28 Gbps	**< 0.5 Gbps**
Measured T_1	18.3 μs	17.8 μs
$\|2\rangle$ population	Negligible	Negligible (T_G>15ns)
π-Rabi P{$\|1\rangle$}	~95%	~95%
3 Gate RMS Err	2.5%	11.7% (uncalibrated)
Total AC+DC PWR	> 1W	**< 2mW**

Conclusions

- Integrated cryo electronics required for useful fault tolerance QC

- Gen 1 cryo-CMOS XY controller:
  - 4-bit instruction set
  - < 2 mW power consumption
  - Tested with qubit
  - Important step towards future cryo quantum controller

- Future steps:
  - Randomized benchmarking, on-chip leakage cancellation, DRAG, Z control, etc.

Acknowledgement

- This work was partially carried out during a sabbatical with support of the **Google Visiting Faculty Program**.
- We thank NSF CCCS-1809114, CCCS 1351744 for further support

- **Current postdoc opening at UMass**