Low-Power Cryo-CMOS Circuits and Systems

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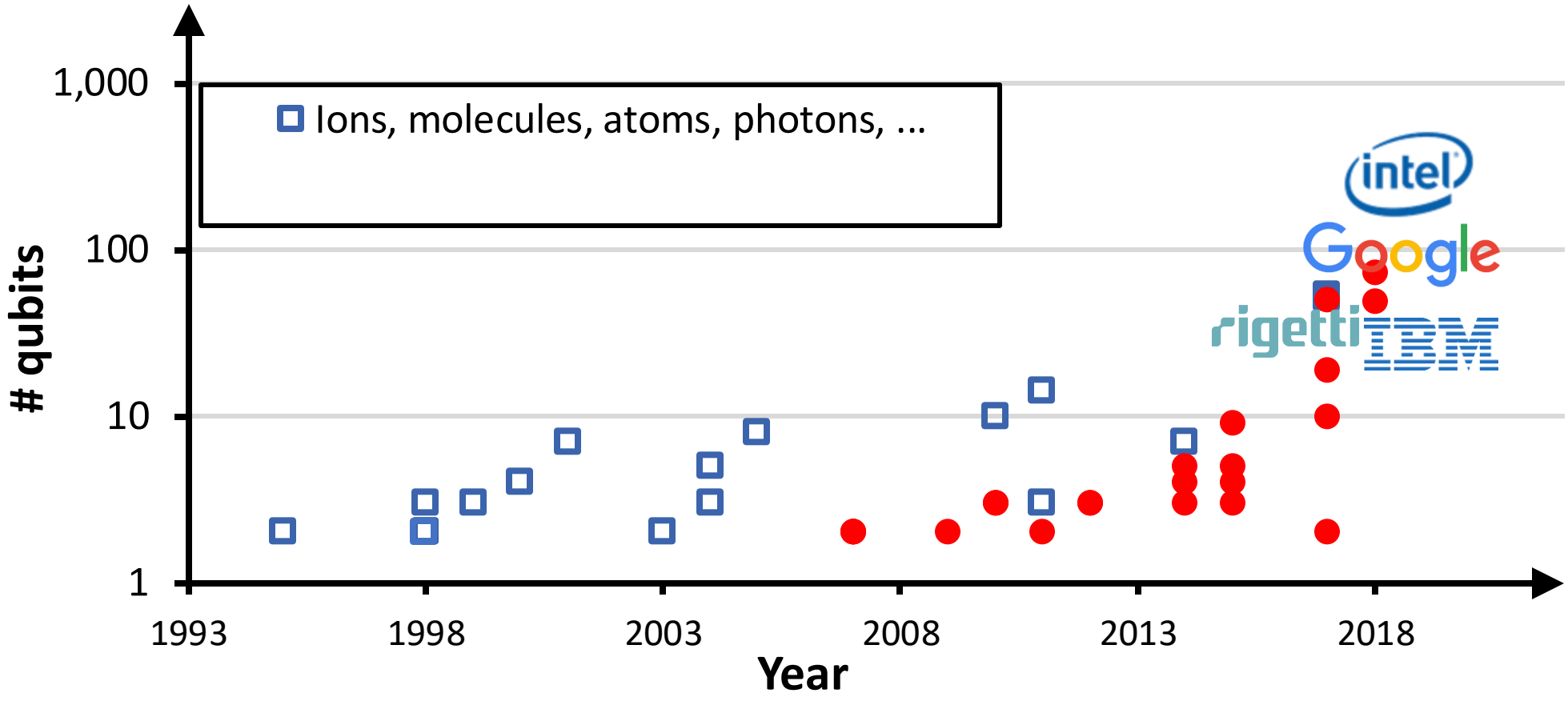
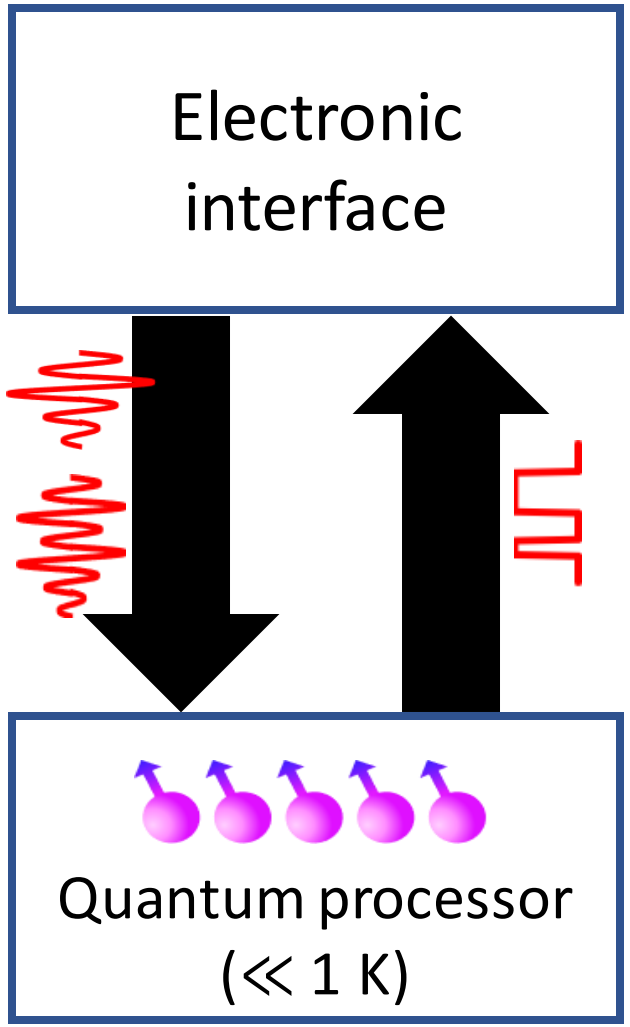
Outline

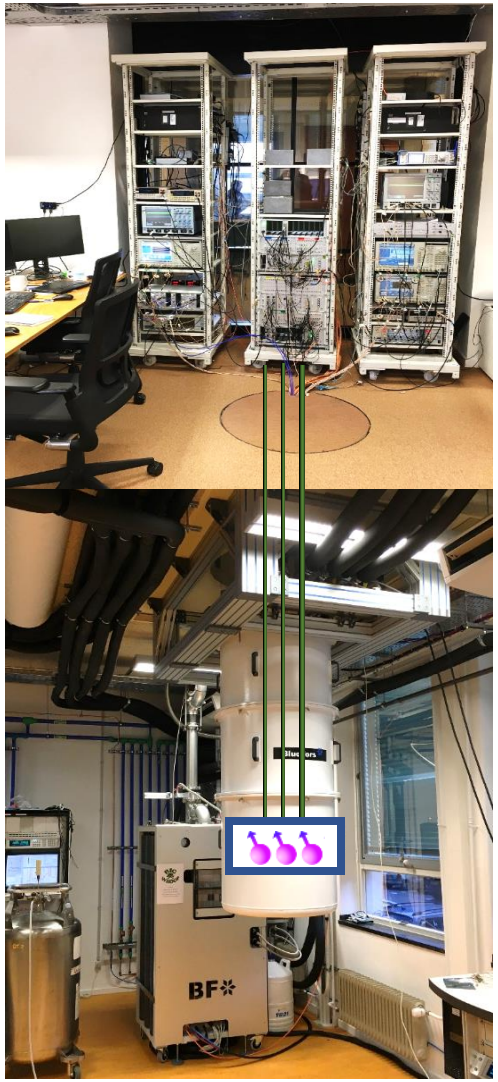
- Scalability of the Control Electronics
- A Cryo-CMOS Controller
- Device & System Modeling
- Cryo-CMOS Circuits
- Conclusion

State-of-the-Art



A real-life quantum computer





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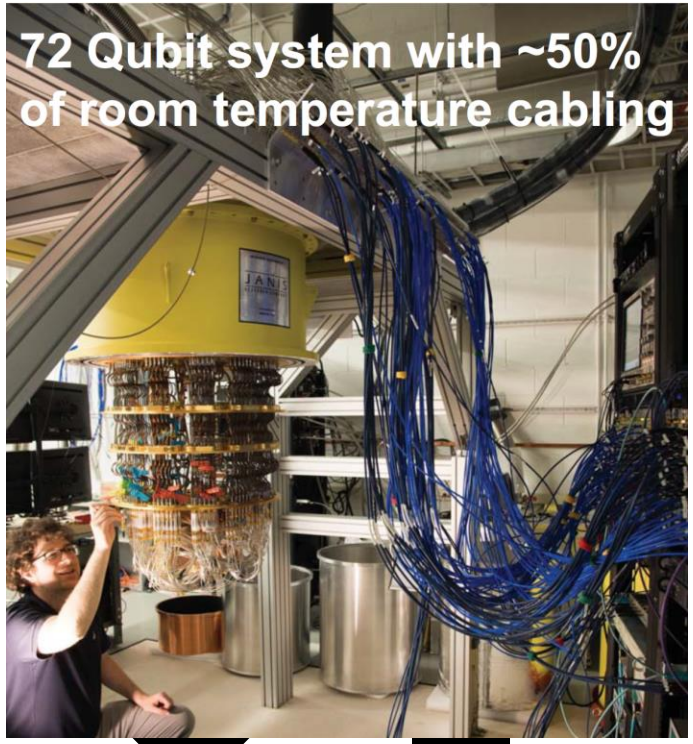
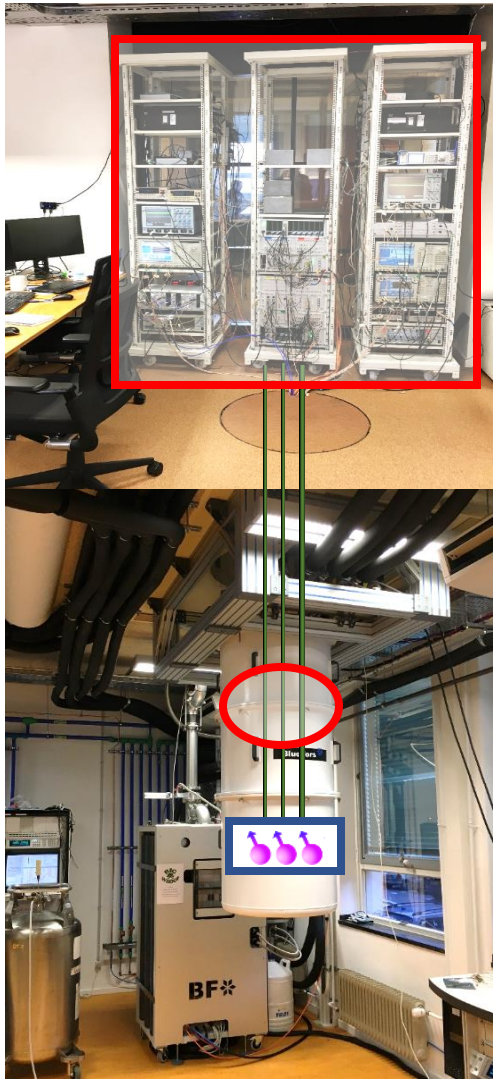


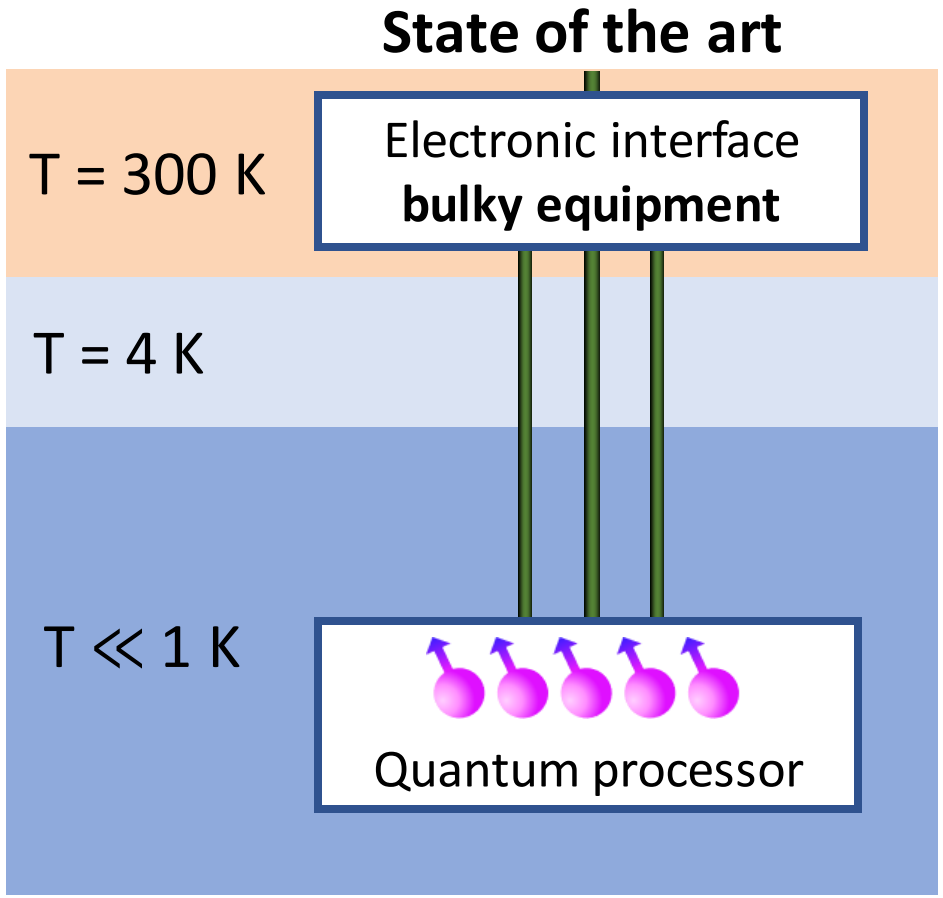
Image: Google Bristlecone. Taken from: J.C. Bardin et al., *"An Introduction to Quantum Computing for RFIC Engineers"*, RFIC Symposium 2019

How to scale up?

Quantum processor
(≪ 1 K)



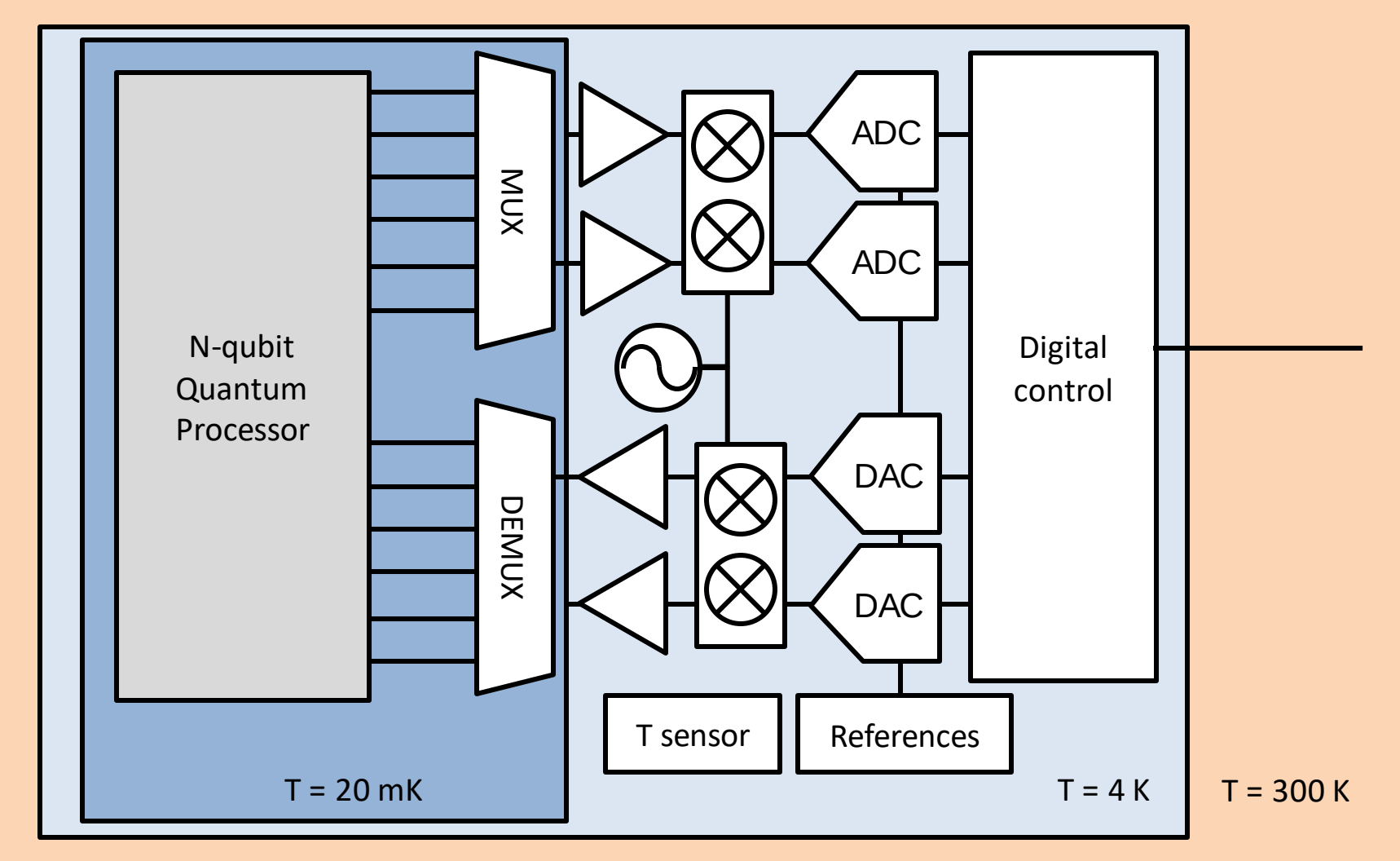
Our Vision



Cryogenic and **integrated** electronic interface

for **large-scale** quantum computers

A Scalable Quantum Computer

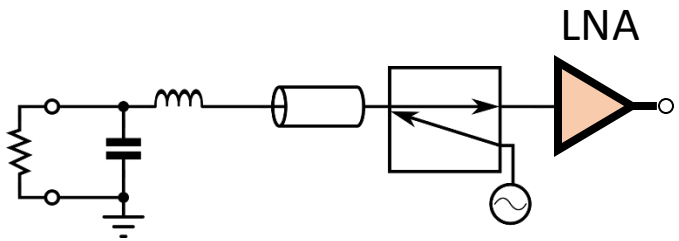


Challenges

- Performance

Constant voltages
- Stability < 1 μV

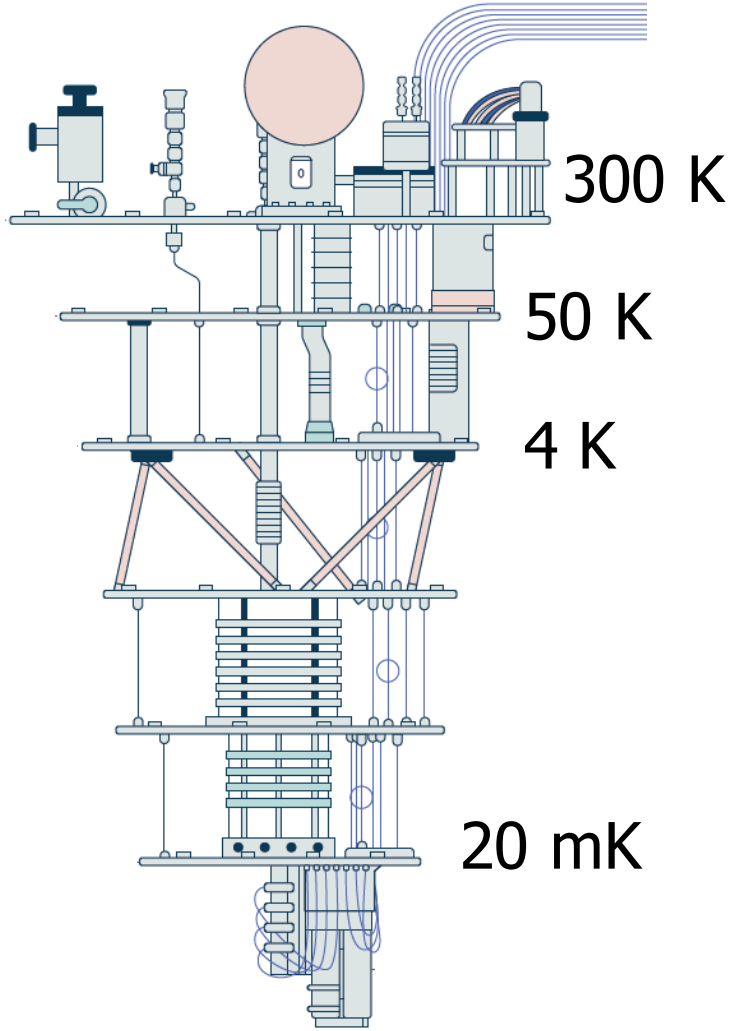
Microwave pulses
- Frequency > 5 GHz
- Resolution > 10 bit
- Timing accuracy < 1 ns



Read-out
- Noise < 100 pV/√Hz
- Kick-back < 100 μV

Challenges

- Performance
- Power dissipation
  - < 1 mW @ 20 mK
  - ~ 1 W @ 4 K
  - 1 W for 1000 qubits?
    ⇒ 1 mW/qubit



Challenges

- Performance
- Power dissipation
- Cryogenic technology
  - Operate @ 4 K, 20 mK, …
  - Superconducting devices (RSFQ, RQL, SQUID, …)

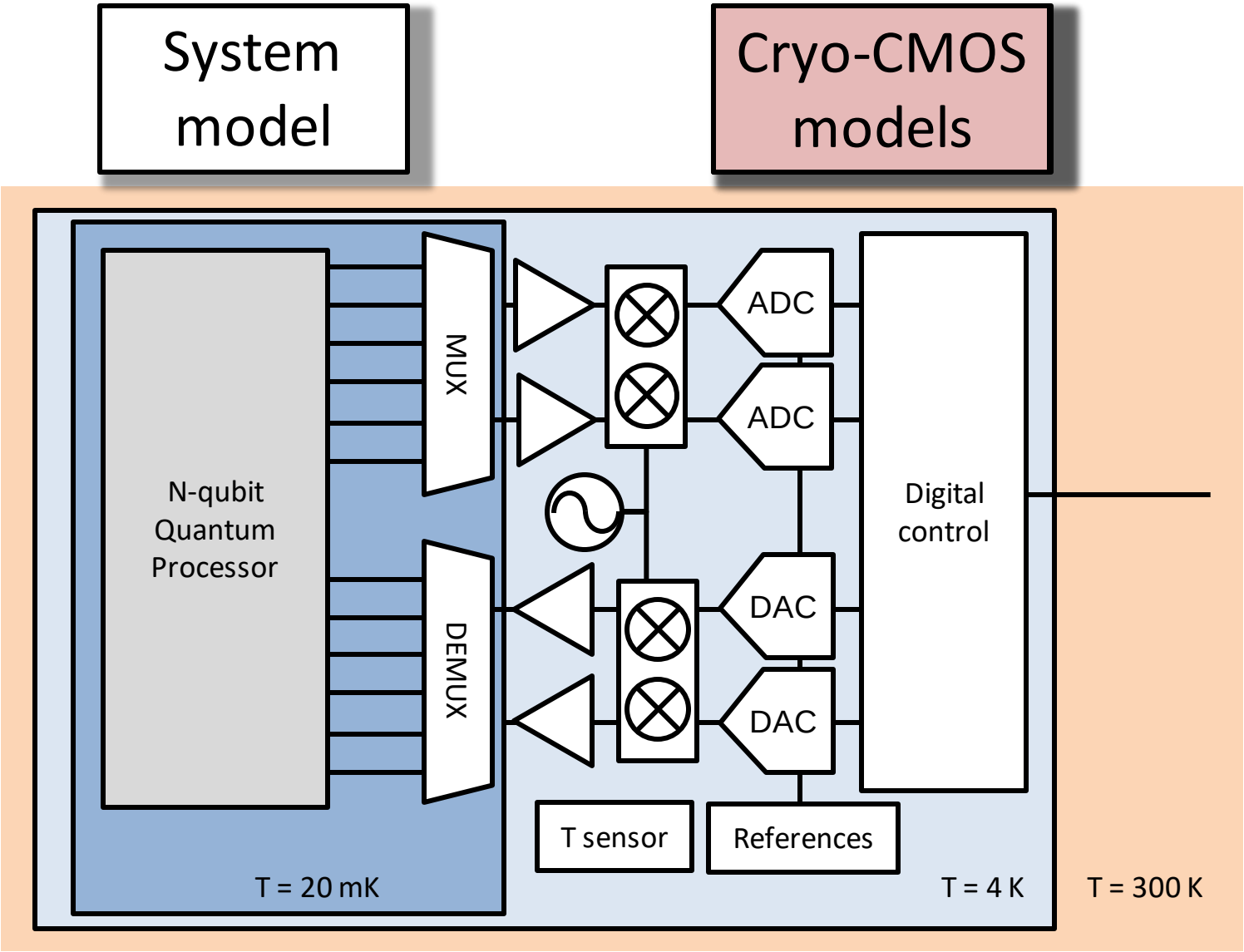
Semiconductors	**Minimum temp.**
Si BJT	100 K
Ge BJT	20 K
SiGe HBT	< 1 K
GaAs MESFET	< 4 K
CMOS	30 mK or below?

Most used today

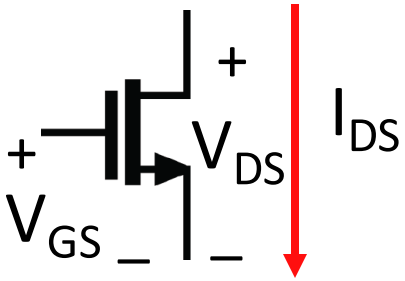
Very Large Scale Integration

Challenges

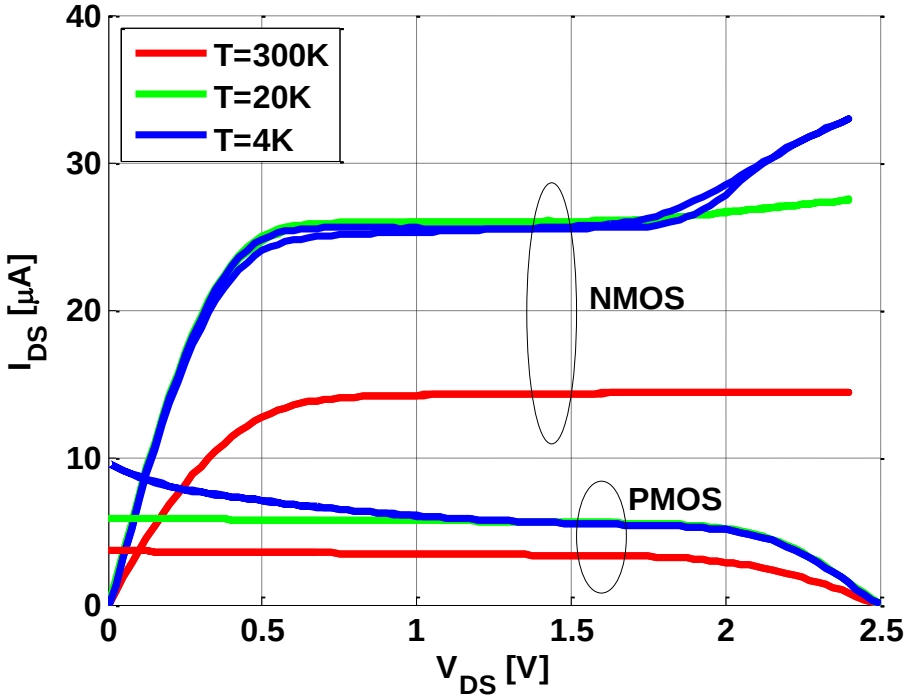
- Performance
- Power dissipation
- Cryogenic technology

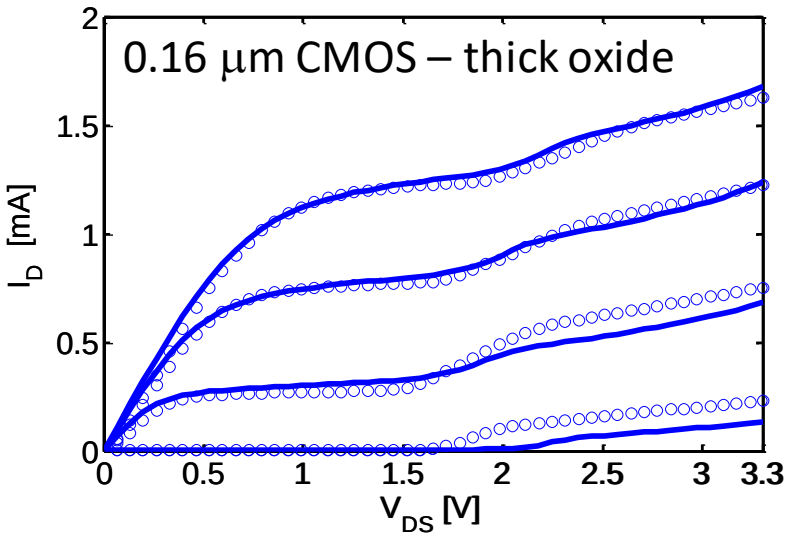


Cryo-CMOS Characteristic



W/L=0.4/1.61
0.322-µm CMOS
V_{GS} = 1.5 V





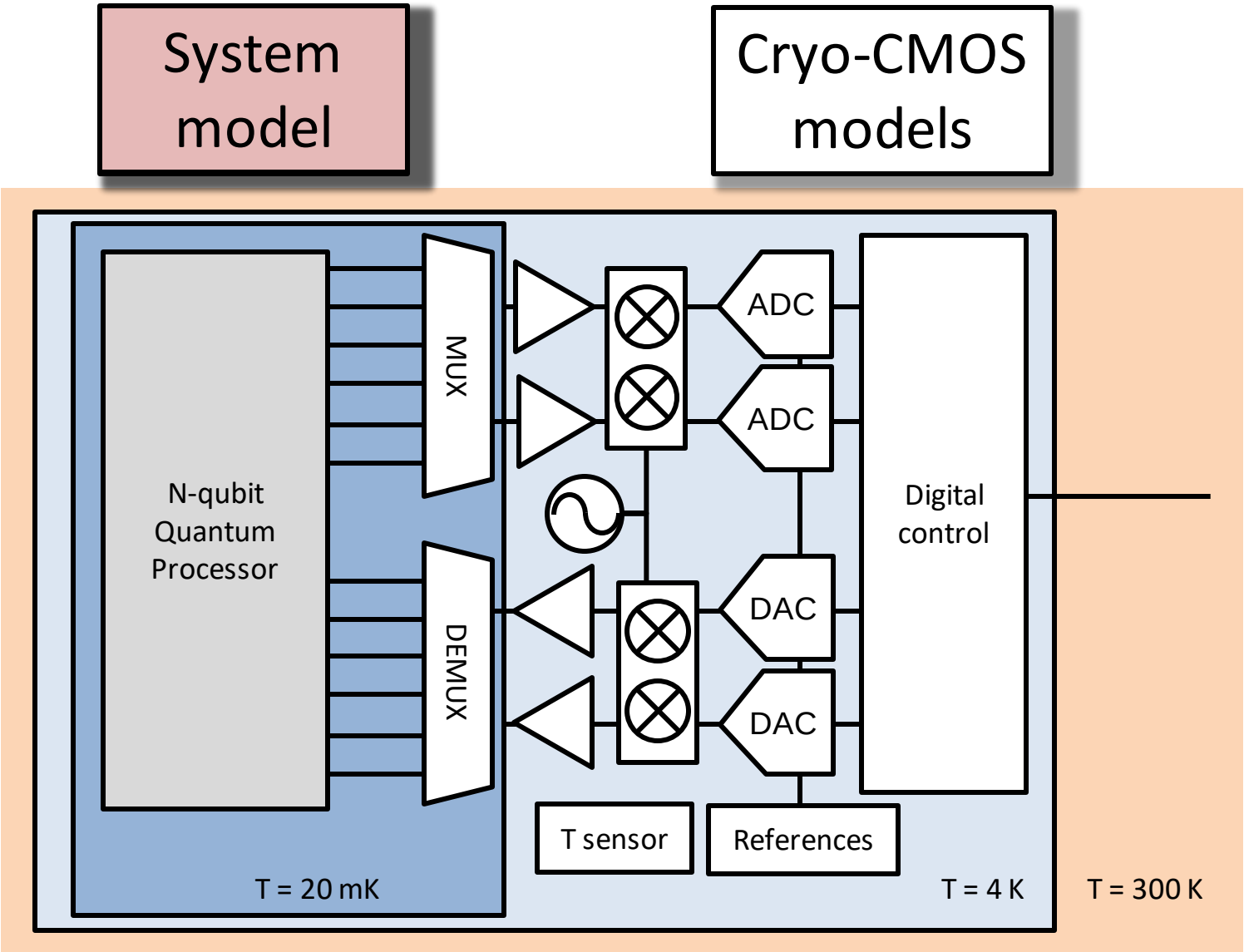
Compact Spice model

→ *More by P.A. 't Hart*

[ESSDERC 2017, JEDS 2018]

Challenges

- Performance
- Power dissipation
- Cryogenic technology



Objective

1-qubit gate:
Oscillator phase noise
Timing accuracy
…

Fidelity
Quantum Processor

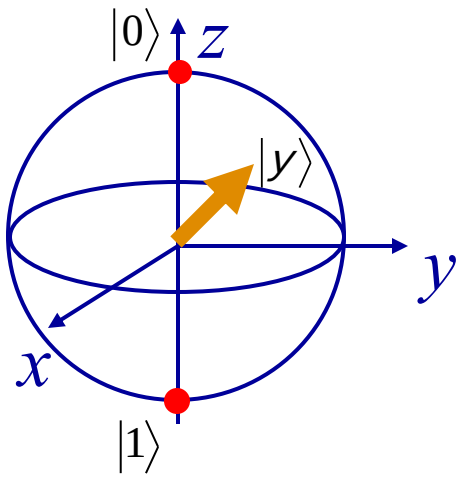
2-qubit gate:
Voltage drift
Timing jitter
…

Qubit read-out:
Amplitude noise
…

Power
Electronic Interface

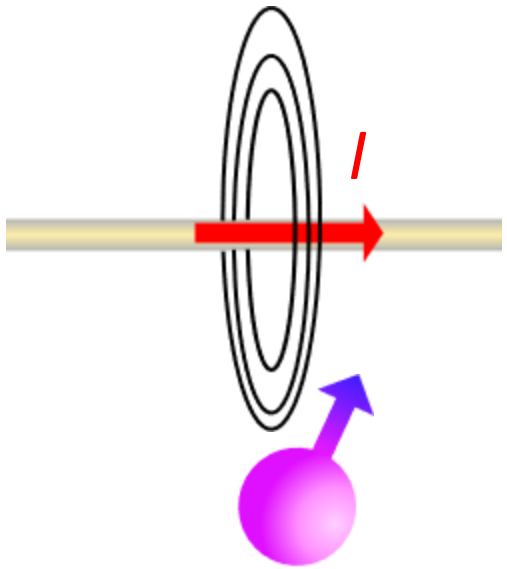
Rotating a Single-Electron Spin Qubit

- Single electron in magnetic field rotates around Z-axis
  - Typical Larmor ('qubit') frequency: 5…20 GHz
- By applying a varying magnetic field rotates around X/Y-axis
  - Drive at qubit frequency
  - Drive coherent to the qubit

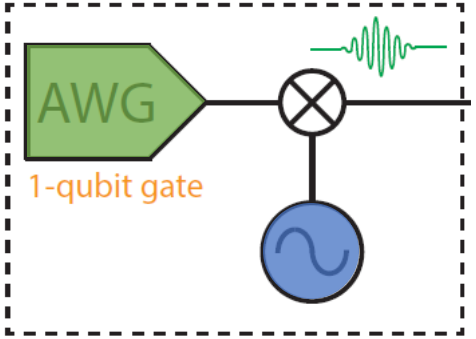


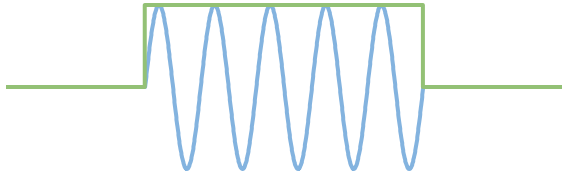
Microwave pulse

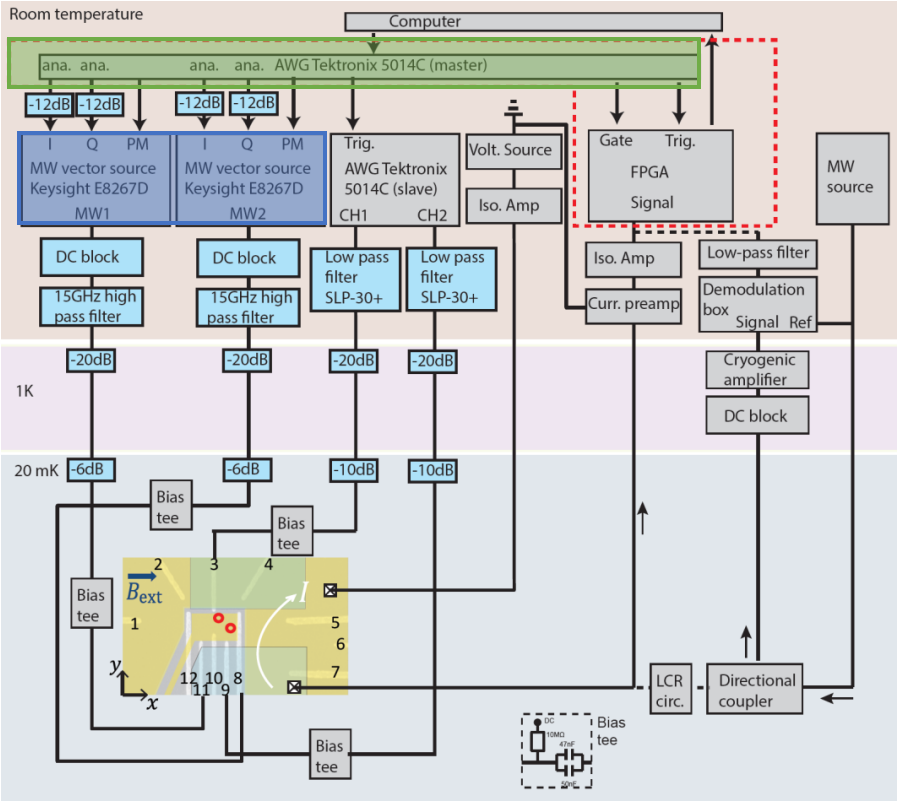
f ~ 5 GHz – 20 GHz



Example – Microwave generation





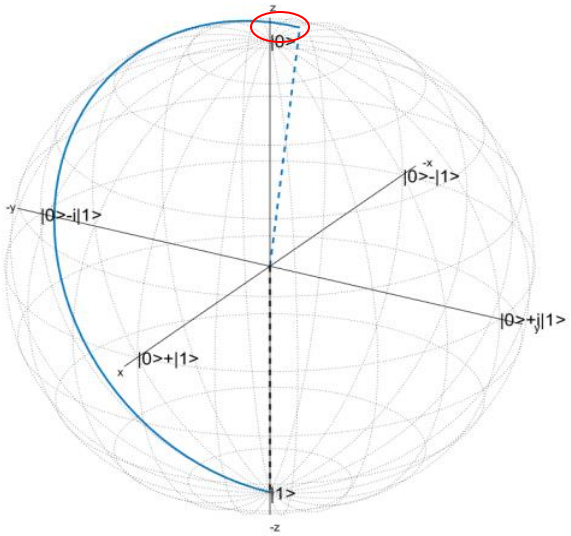


Courtesy of T. Watson (Vandersypen Lab)

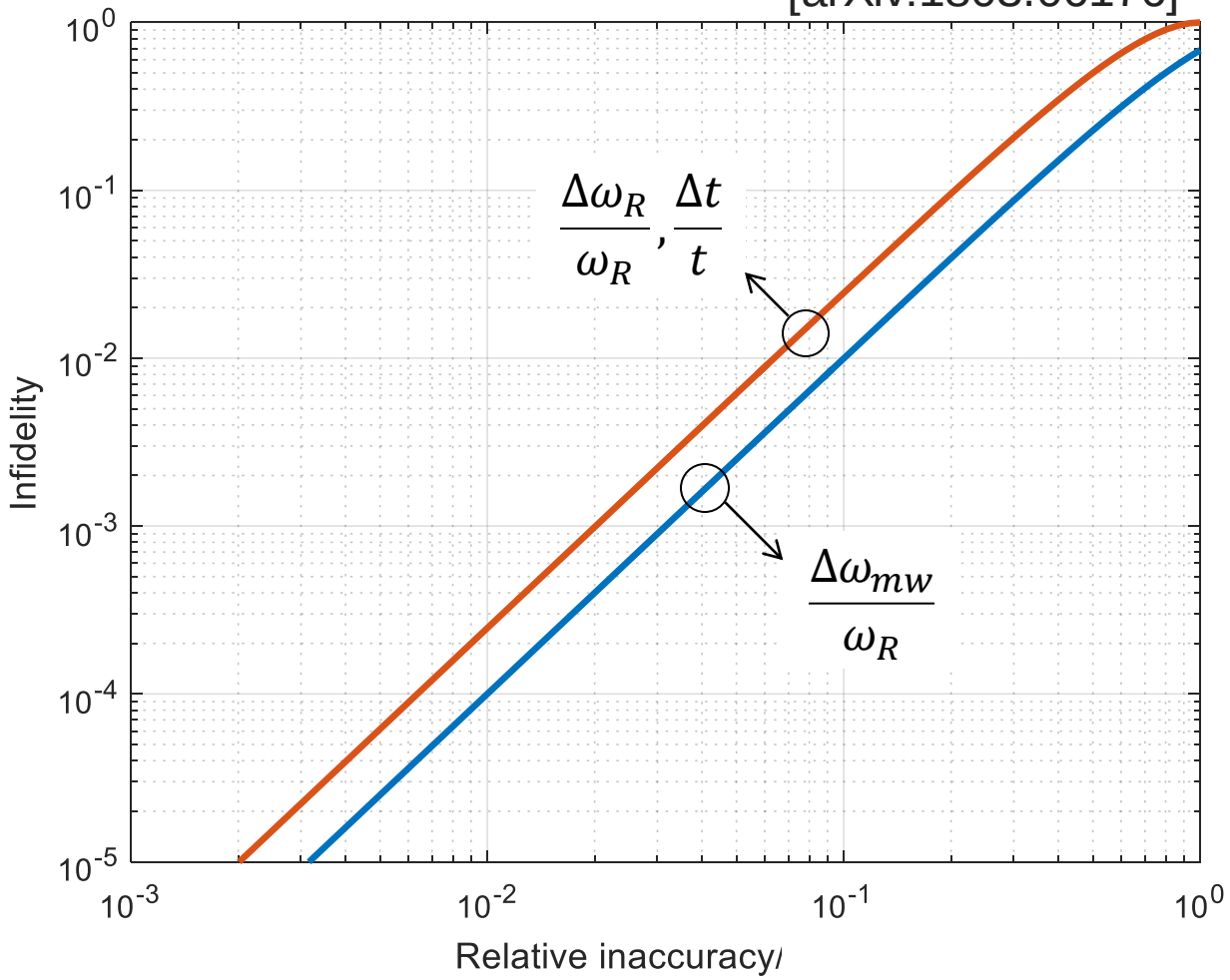
- **System modelling:** how electronics affect qubits
- Errors in single-qubit gate
  - Microwave envelope: amplitude / duration
  - Microwave carrier: frequency / phase

Specifications for the Inaccuracy

Example:



[arXiv:1803.06176]

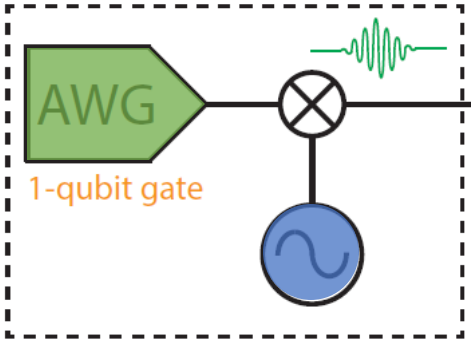


1-Qubit Gate Specifications

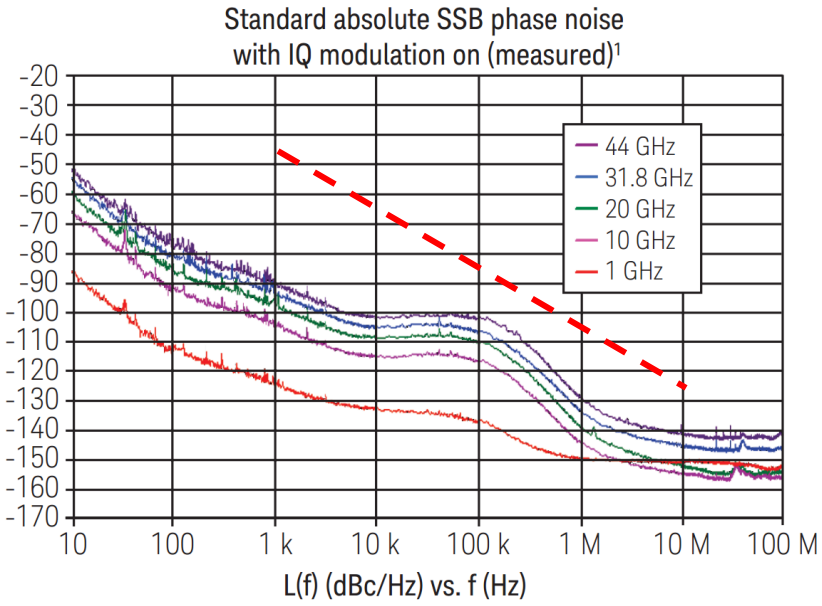
- Example specifications for F = 99.9% (π-rotation in 500 ns)

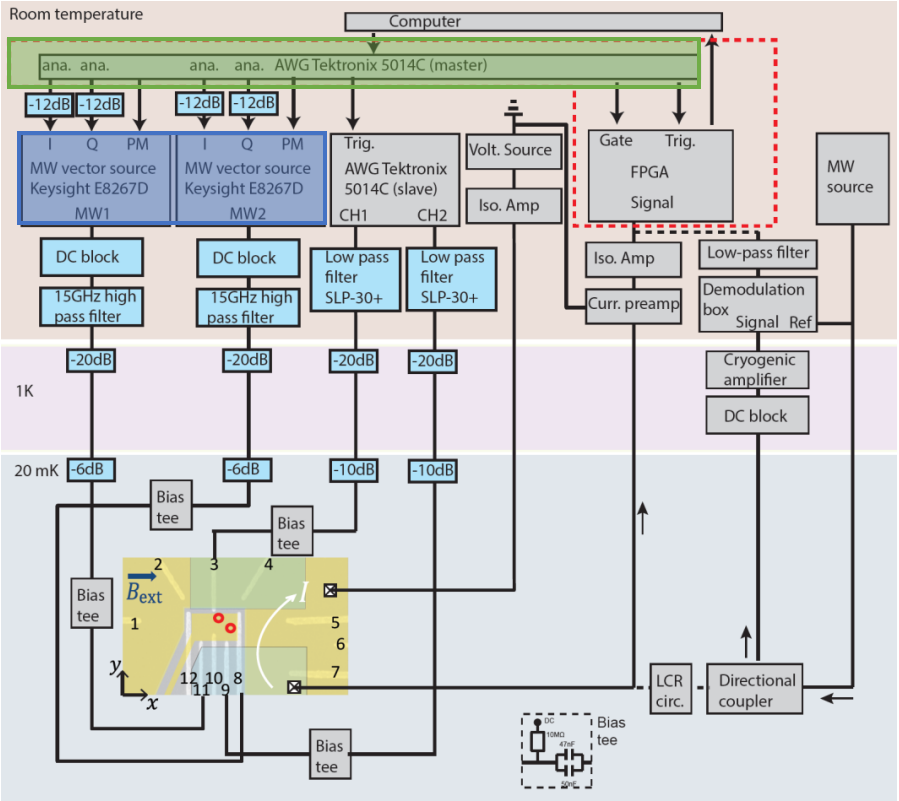
	Contribution	Value	
Frequency			
Inaccuracy	125 ppm	11.2 kHz	
Oscillator noise	125 ppm	11.2 kHz_{rms}	ENBW = 2.47 MHz, $\mathcal{L}$ (1 MHz) = -106 dBc/Hz
Nuclear spin noise	3.6 ppm	1.9 kHz_{rms}	(T_2^* = 120 µs)
Wideband noise	125 ppm	12 μV_{rms}	ENBW = 2.85 MHz, S_n = 7.12 nV/√Hz
Phase			
Inaccuracy	125 ppm	0.64°	
Amplitude		2 mV	
Inaccuracy	125 ppm	14.2 µV	8-bit resolution
Noise	125 ppm	14.2 μV_{rms}	ENBW = 1 MHz, PSD = 14.2 nV/√Hz, SNR = -40 dB
Duration		500 ns	
Inaccuracy	125 ppm	3.56 ns	f_s = 140 MS/s
Noise	125 ppm	3.56 ns_{rms}	
FIDELITY	99.9 %		

Existing Setup



- Microwave Carrier: **Keysight E8267D**
  - 22.4 kHz resolution — 1 mHz
  - $\mathcal{L}$ (1 MHz) = -106 dBc/Hz — >15 dB better
  - S_n = 7.12 nV/√Hz — 63 nV/√Hz
    → > 20 dB attenuation





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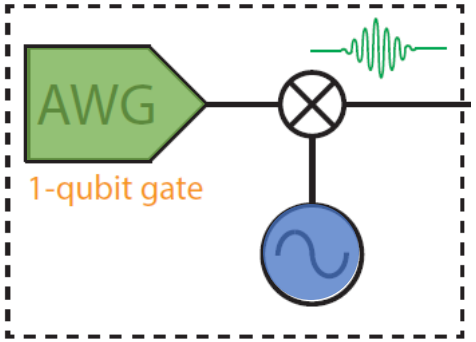

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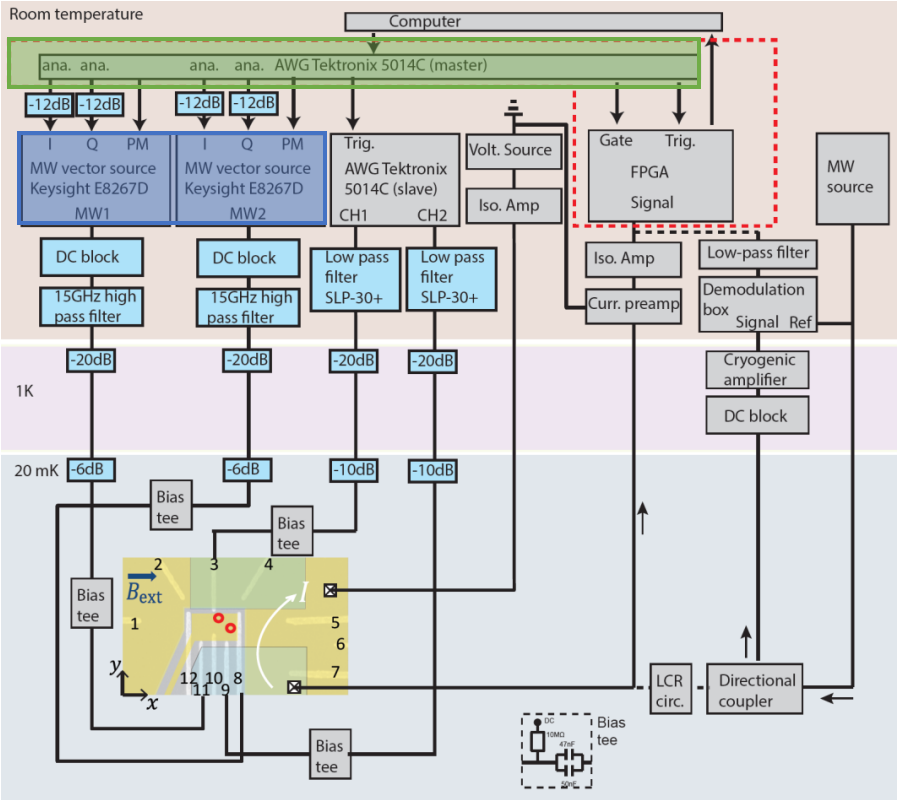
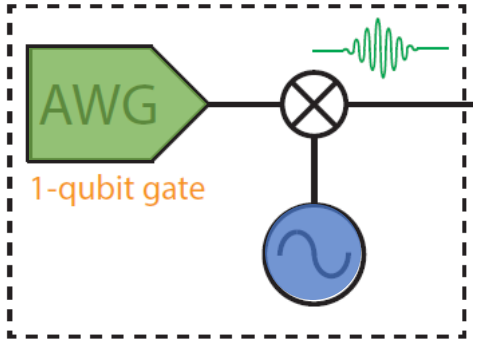
  - S_n = 7.12 nV/√Hz — 63 nV/√Hz
    → > 20 dB attenuation

- Microwave Envelope: **Tektronix 5014C**
  - 8-bit resolution — 14-bit
  - 140 MS/s — 1.2 GS/s
  - 3.56 ns_{rms} — 5.0 ps_{rms}
  - 40 dB SNR — better



Courtesy of T. Watson (Vandersypen Lab)

CMOS Integrated Circuits

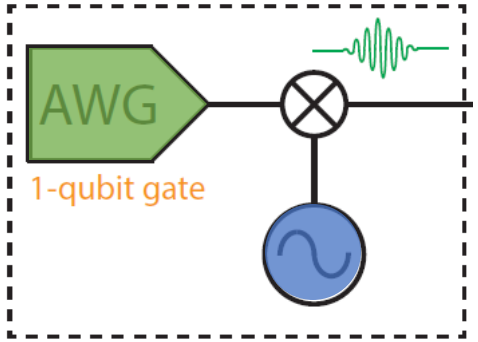


- **Direct implementation:**
  - Digital-to-analog converter (10-bit 500 MS/s)[1] P = 24 mW
  - Phase-locked loop (9.2 - 12.7 GHz)[2] P = 13 mW

P_{tot} = 37 mW/qubit

[1] W. T. Lin *et al.*, IEEE JSSC 2012
[2] K. Raczkowski *et al.*, IEEE JSSC 2015
[3] W. T. Lin *et al.*, IEEE JSSC 2014

CMOS Integrated Circuits



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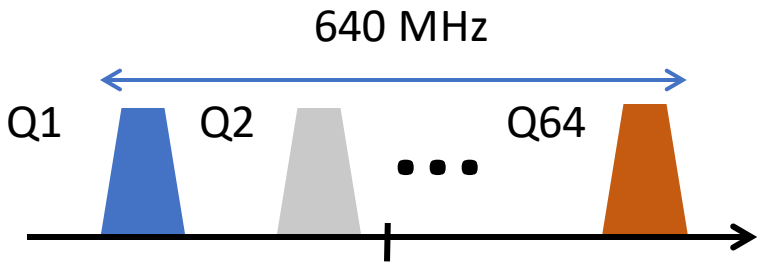
  P_{tot} = 37 mW/qubit

- **Implementation with frequency multiplexing:**
  - Digital-to-analog converter (12-bit 1.6 GS/s)[3] — P = 40 mW
  - Phase-locked loop (9.2 - 12.7 GHz) [2] — P = 13 mW

  P_{tot} < 1 mW/qubit

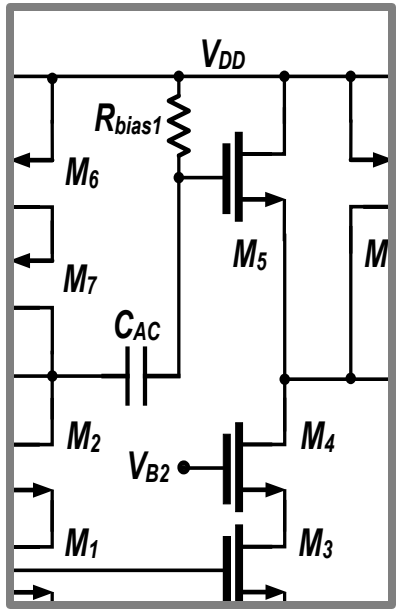


[1] W. T. Lin *et al.*, IEEE JSSC 2012
[2] K. Raczkowski *et al.*, IEEE JSSC 2015
[3] W. T. Lin *et al.*, IEEE JSSC 2014

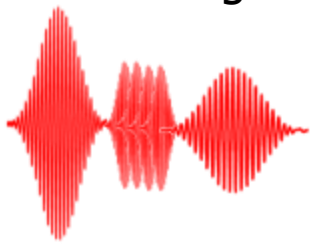
Co-Design Electronics/Quantum

- General procedure to derive specs/verify performance:

Circuit simulator



Electrical signals



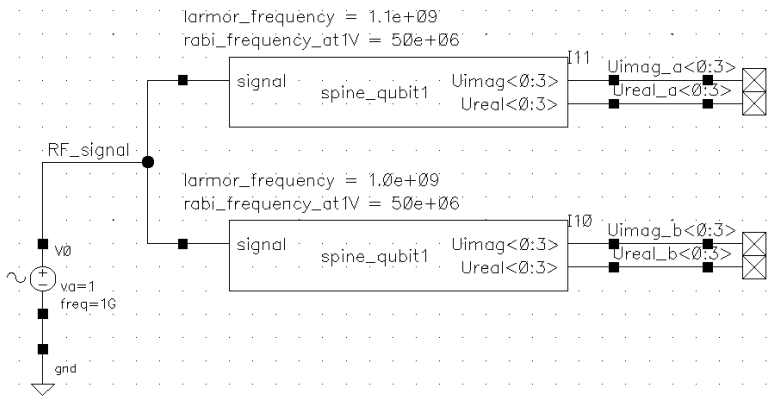
Qubit simulator (Hamiltonian)

Fidelity (control)

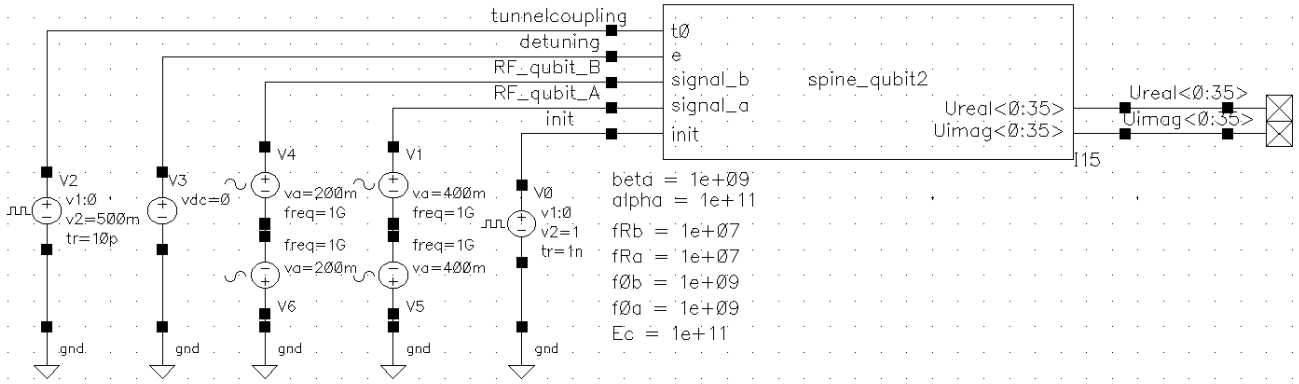
→ Co-simulation for design automation

SPINE = Spin Emulator in Cadence

- Model of a single spin qubit:



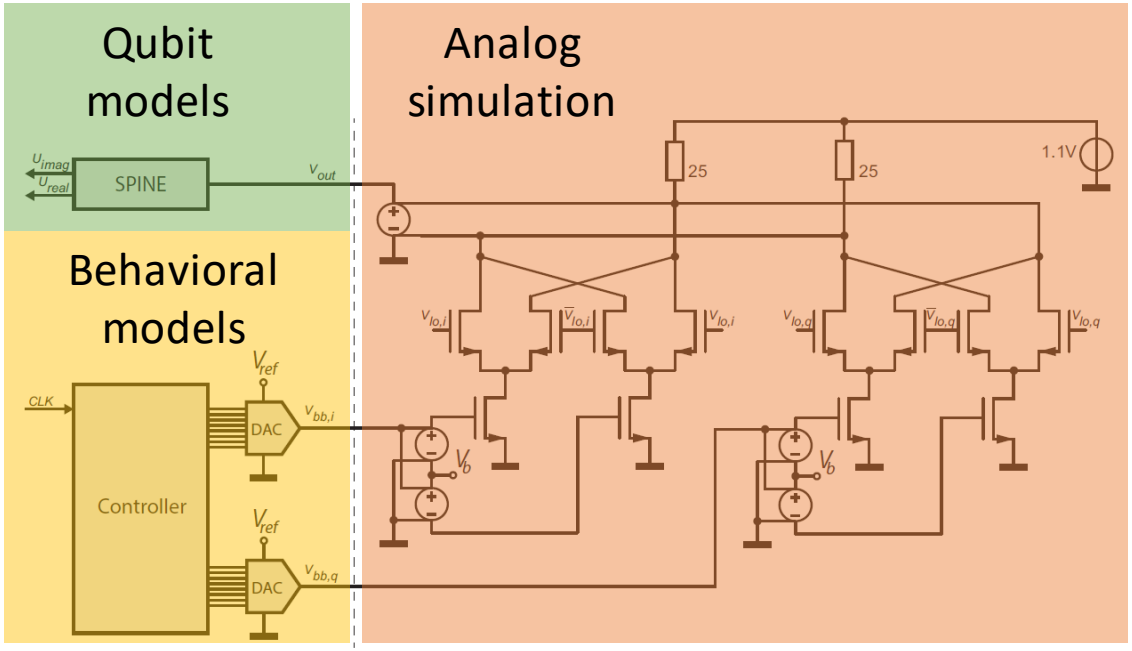
- Model of two coupled spin qubits:

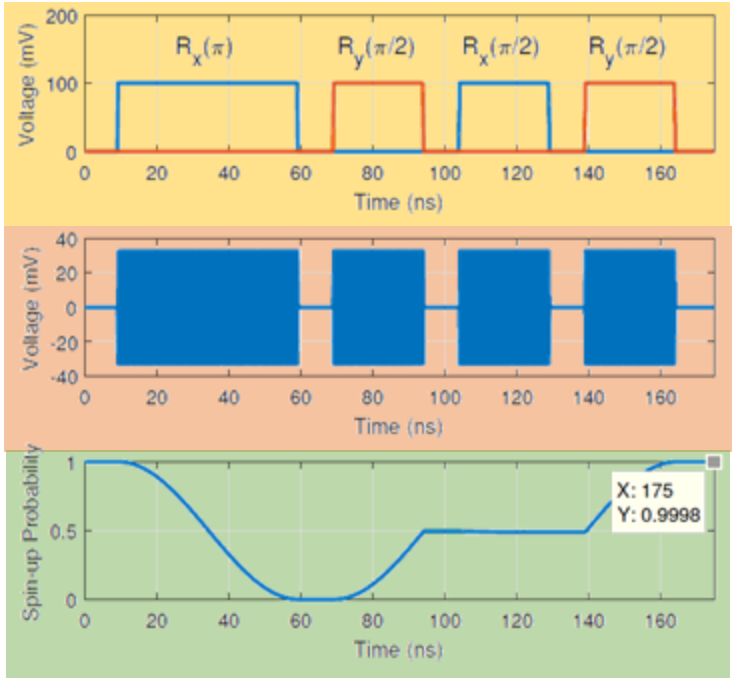


[Best IP award at DATE 2018]

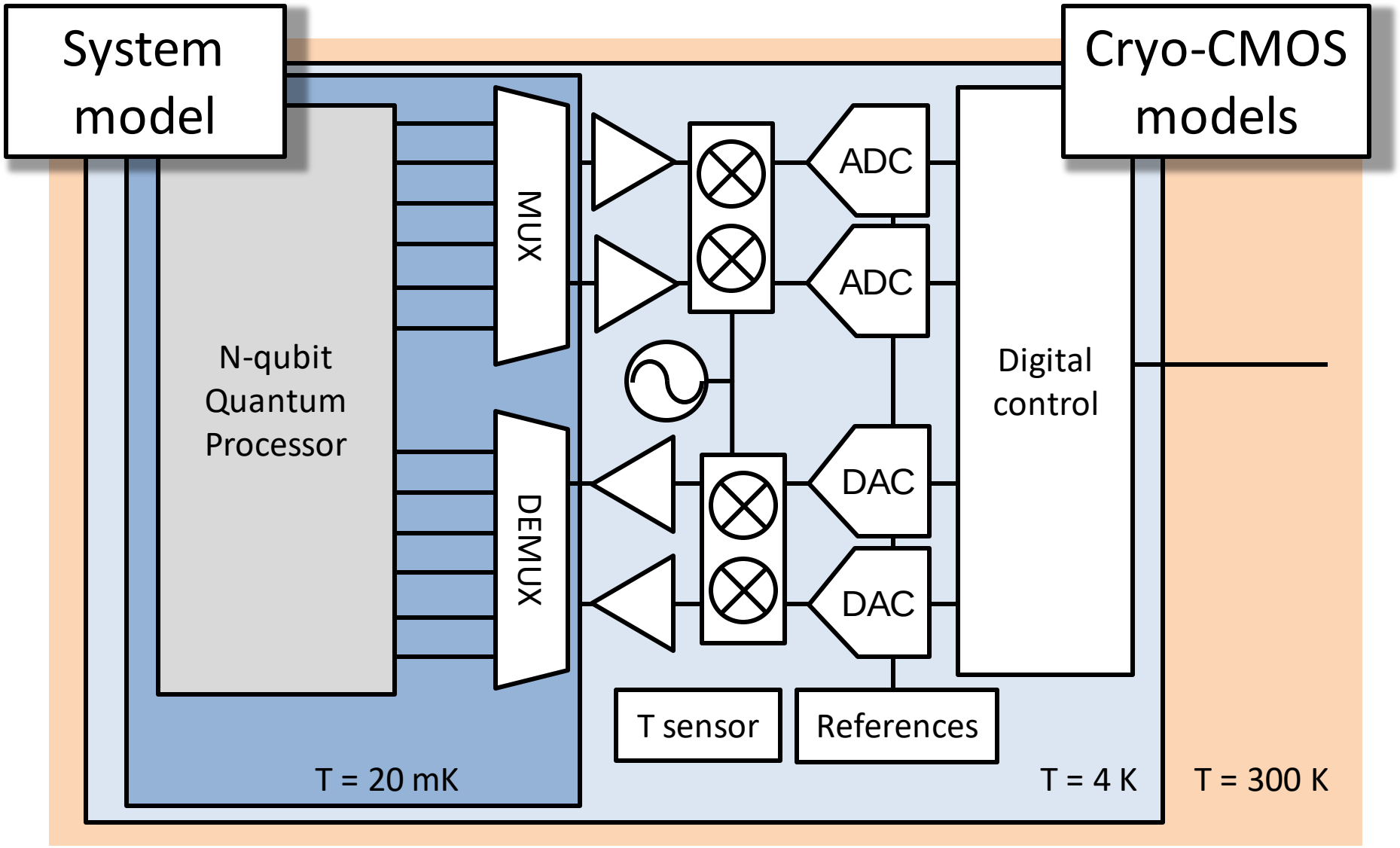
A Co-Simulation Example

- Co-design quantum processors ***and*** electronic interfaces
- System-level verification





Circuit Blocks



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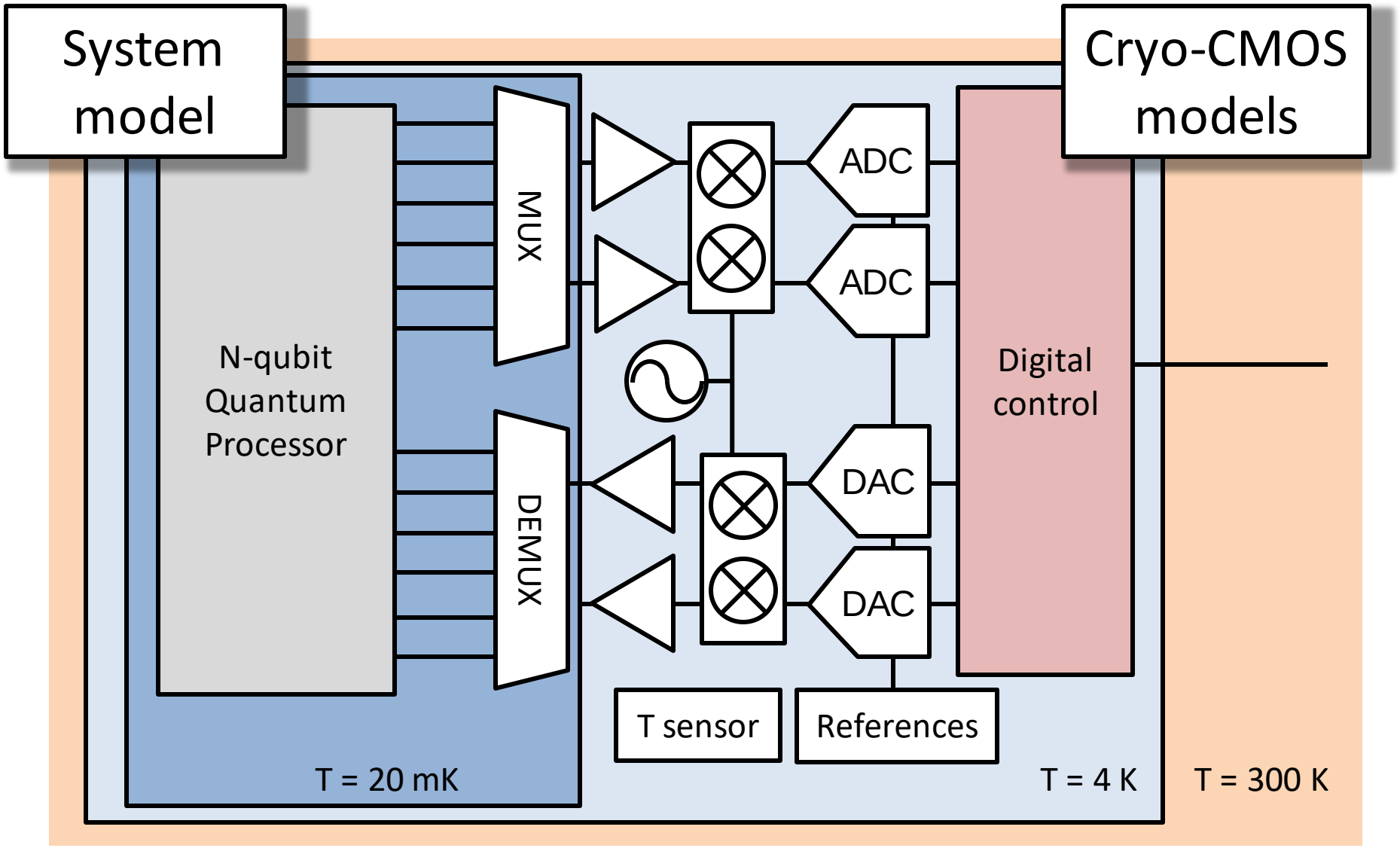
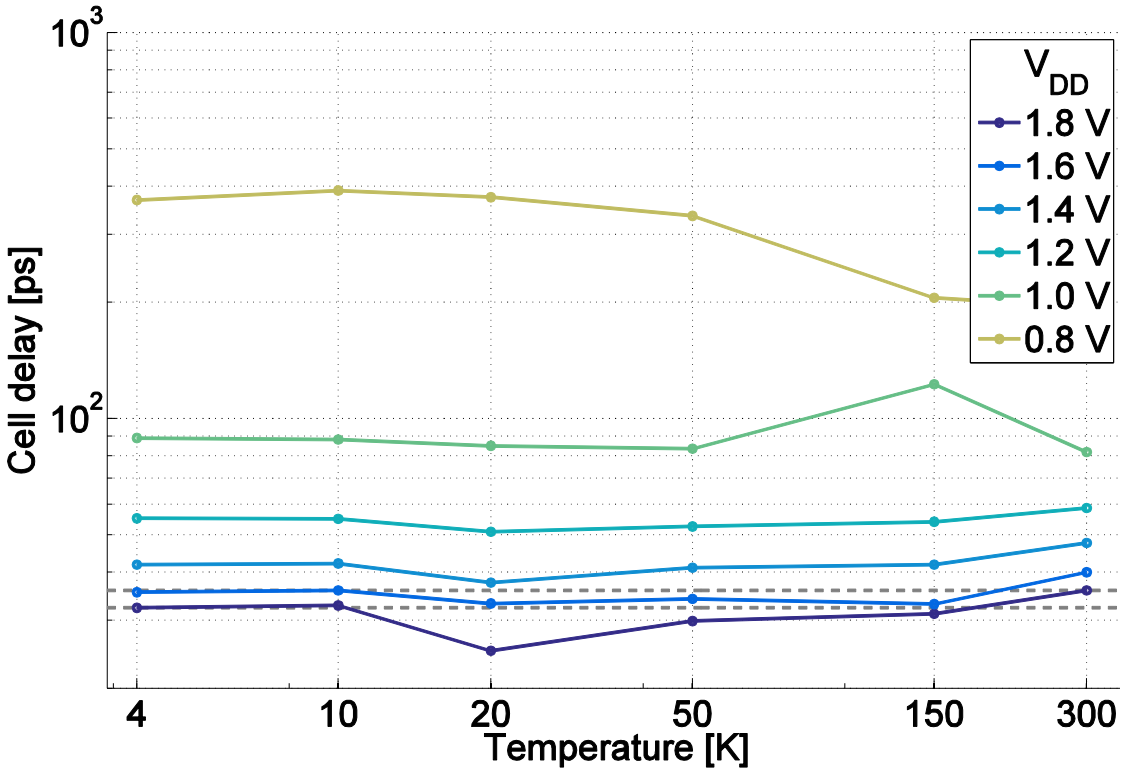


Digital design @ 4 K

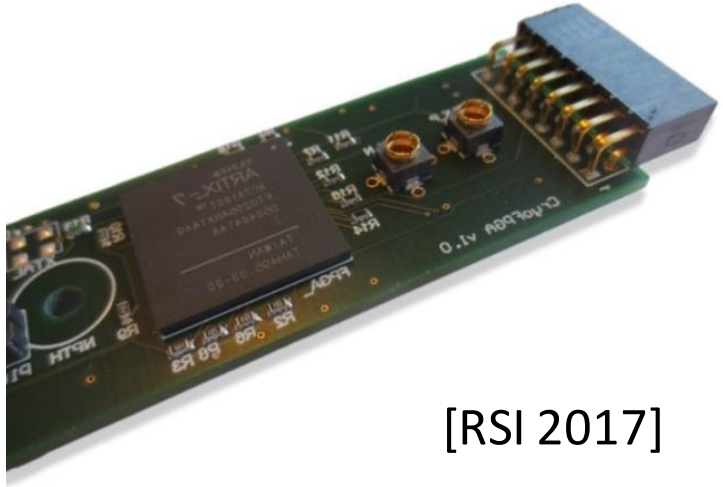
Application-specific IC (ASIC)

160-nm inverter delay

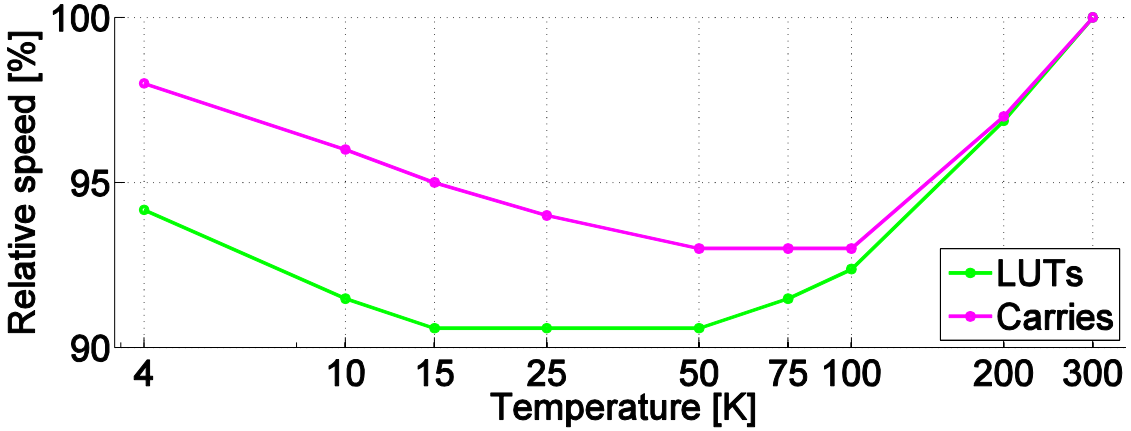


Off-the-shelf standard FPGA

Logic speed change < 10%



[RSI 2017]



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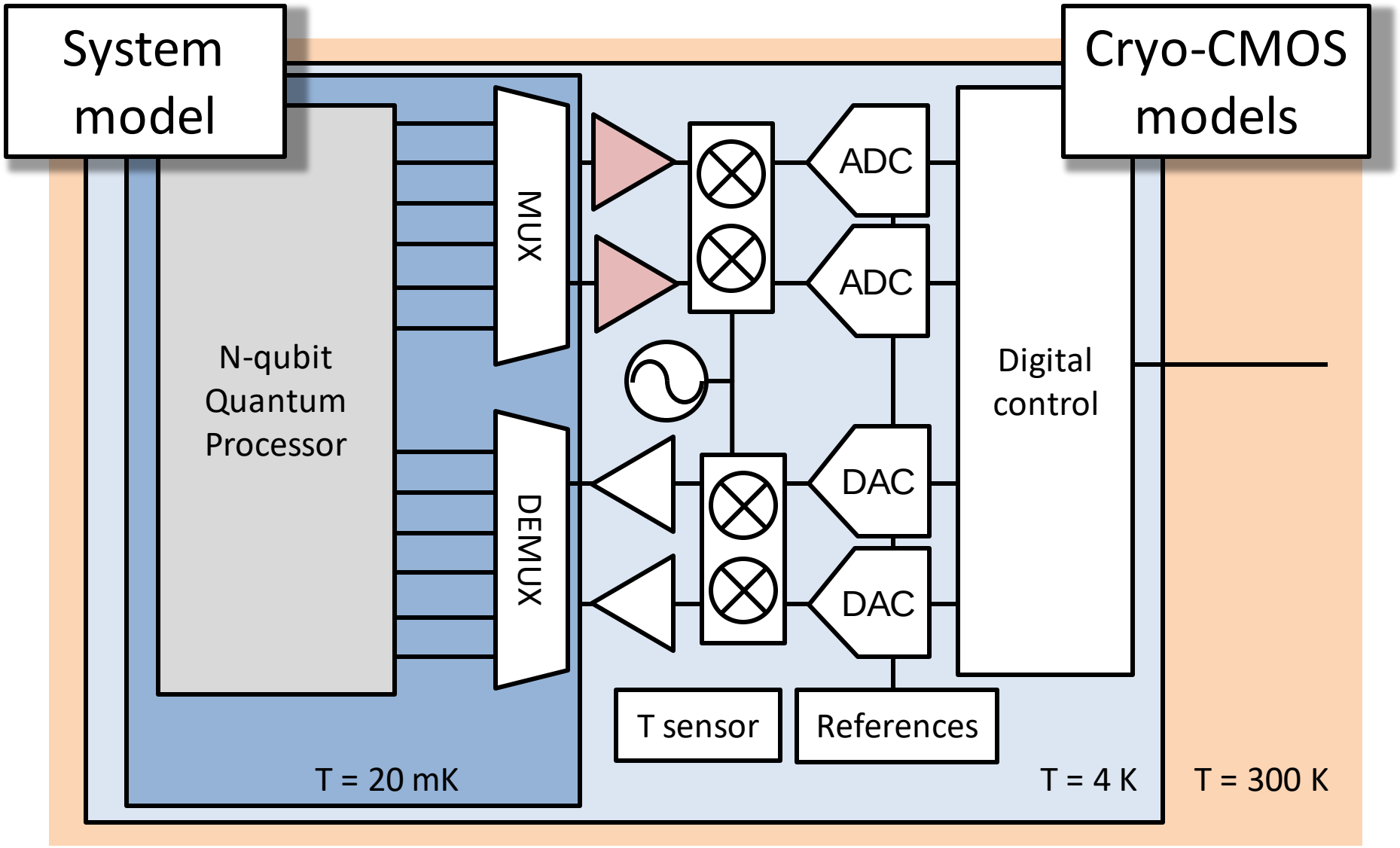
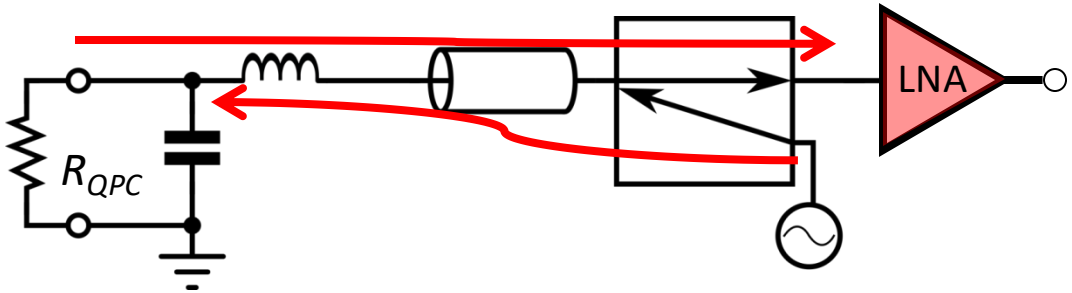
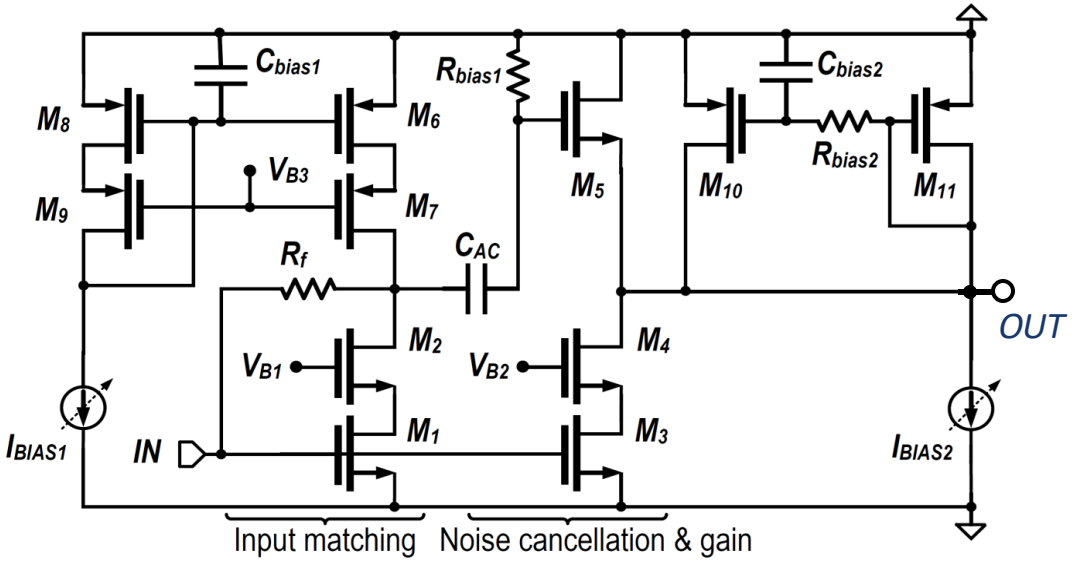


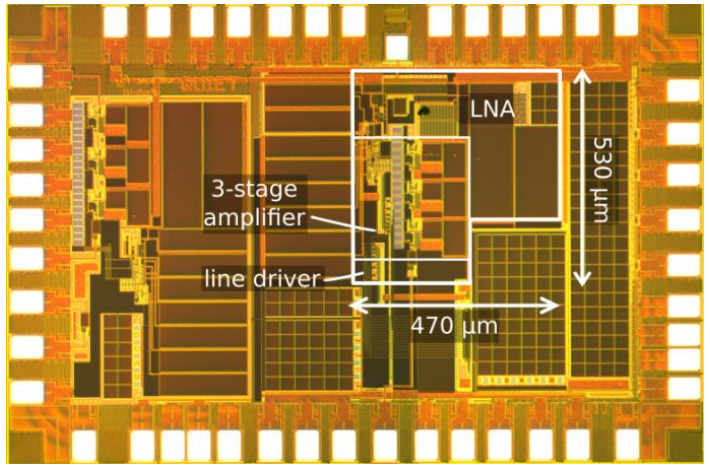
Cryo-CMOS LNA

- LNA for reflectometry
  - 50-Ω input matching
  - Minimum noise





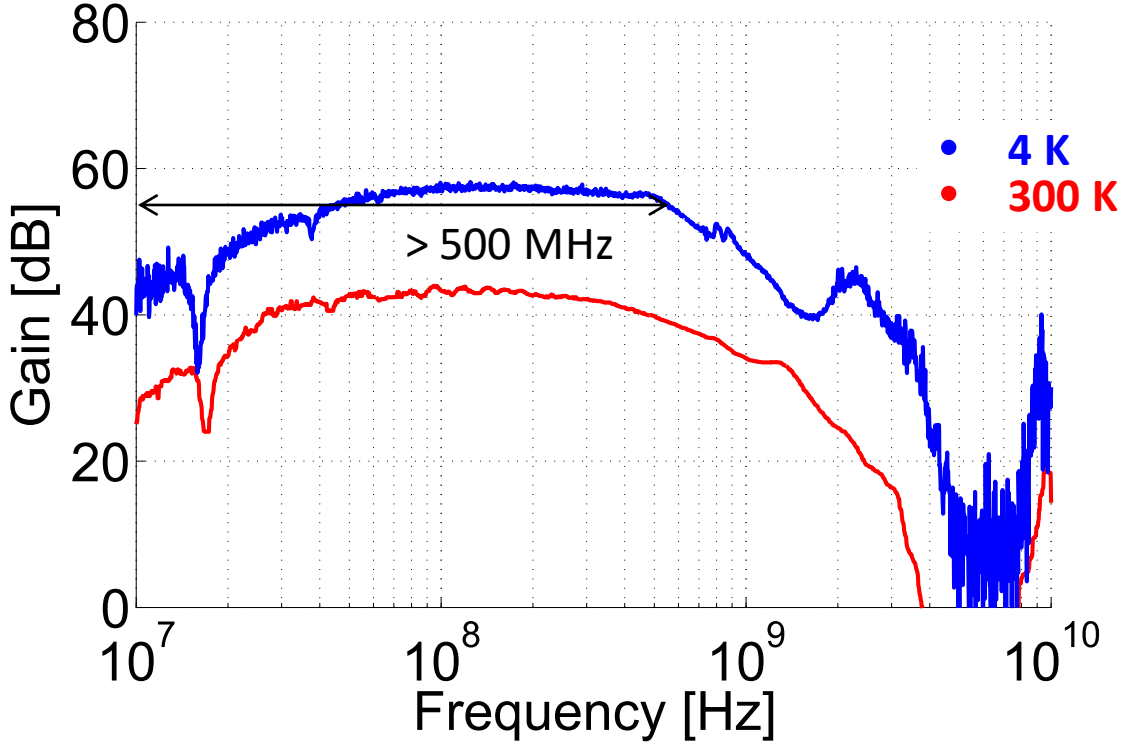
0.16 µm CMOS



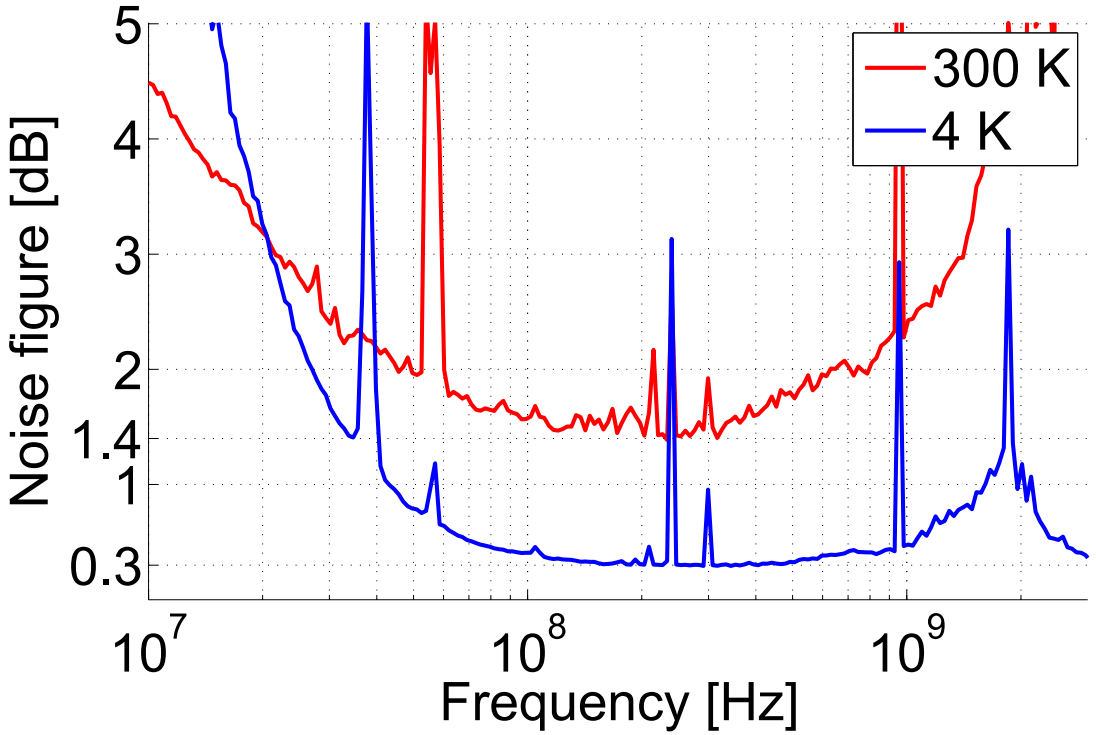
[ISSCC 2017, JSSC 2018]

Cryo-CMOS LNA – Performance

Gain



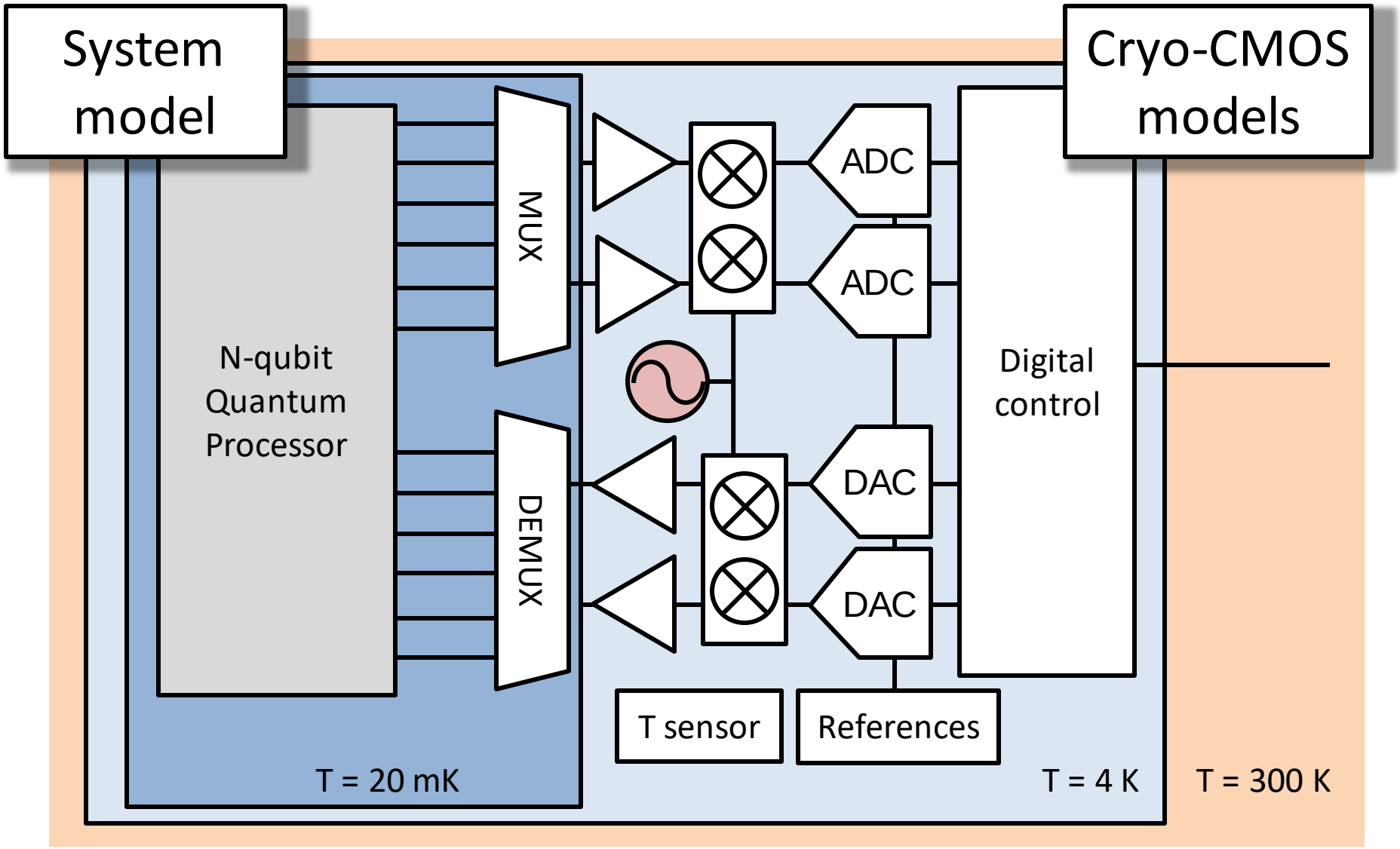
Noise



Power consumption = 91 mW
With FDMA (150x 1-MHz qubits) ⇒ 0,61 mW/qubit

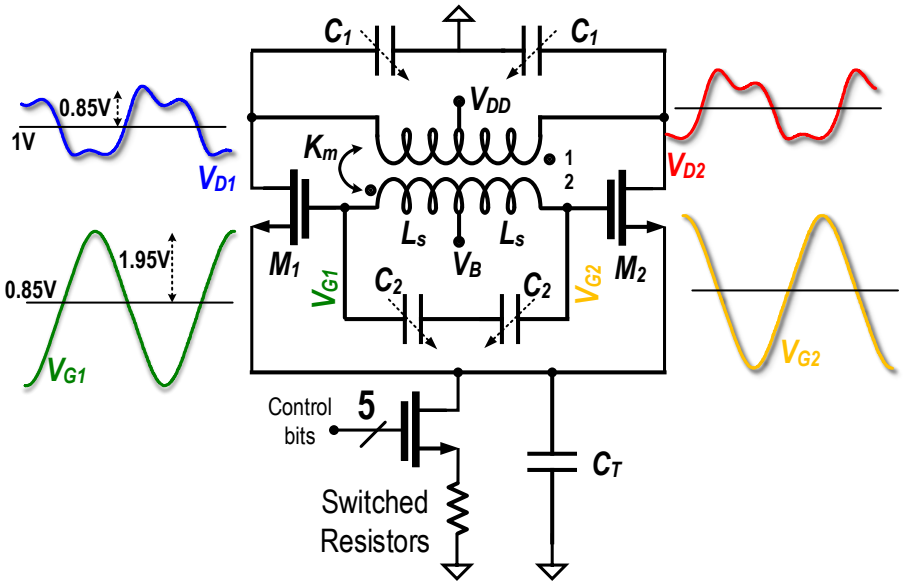
→ *More by H.A.R. Homulle*

Circuit Blocks

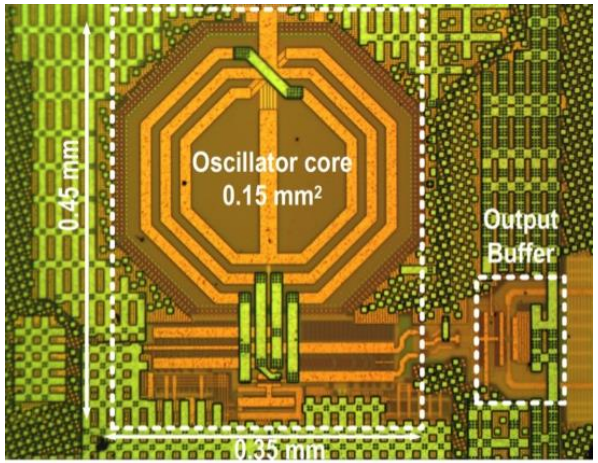


Cryo-CMOS LC Oscillator

- Designed for low flicker noise
- Digitally tunable frequency



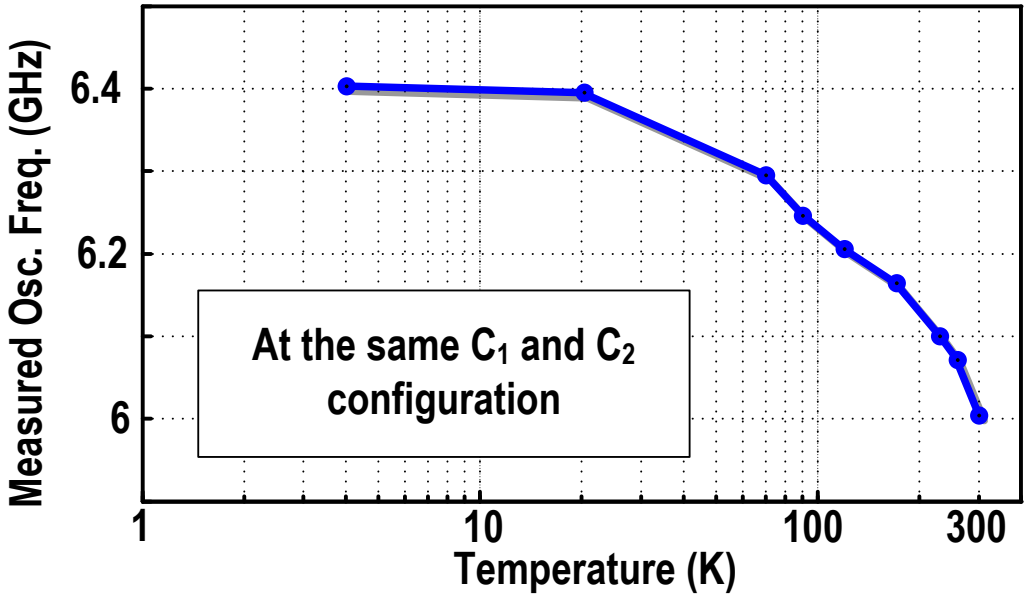
40-nm CMOS



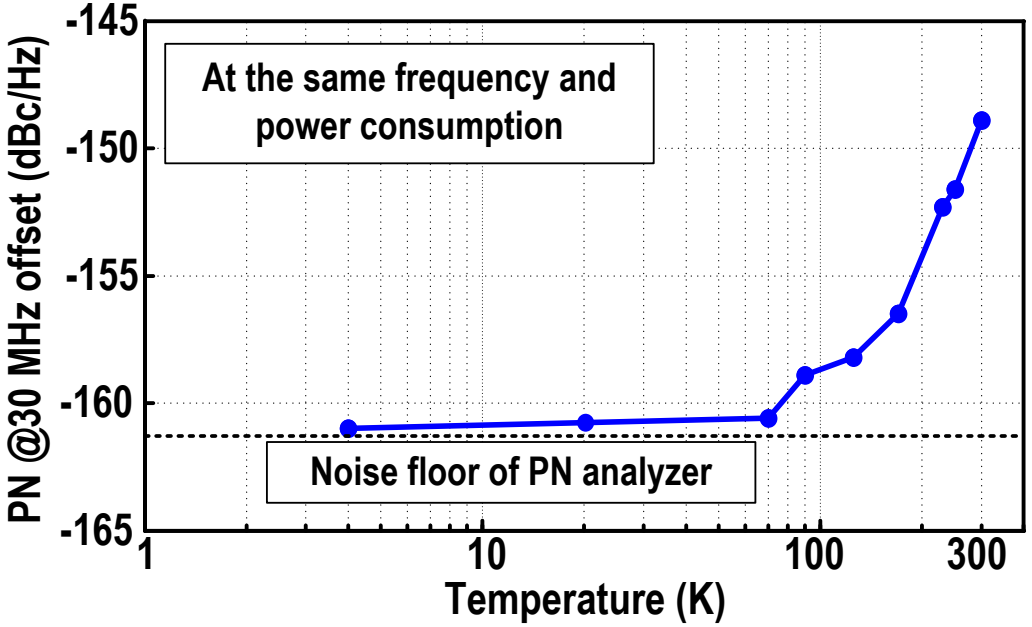
[ISSCC 2017, JSSC 2018]

Cryo-CMOS LC Oscillator - Performance

Oscillation frequency

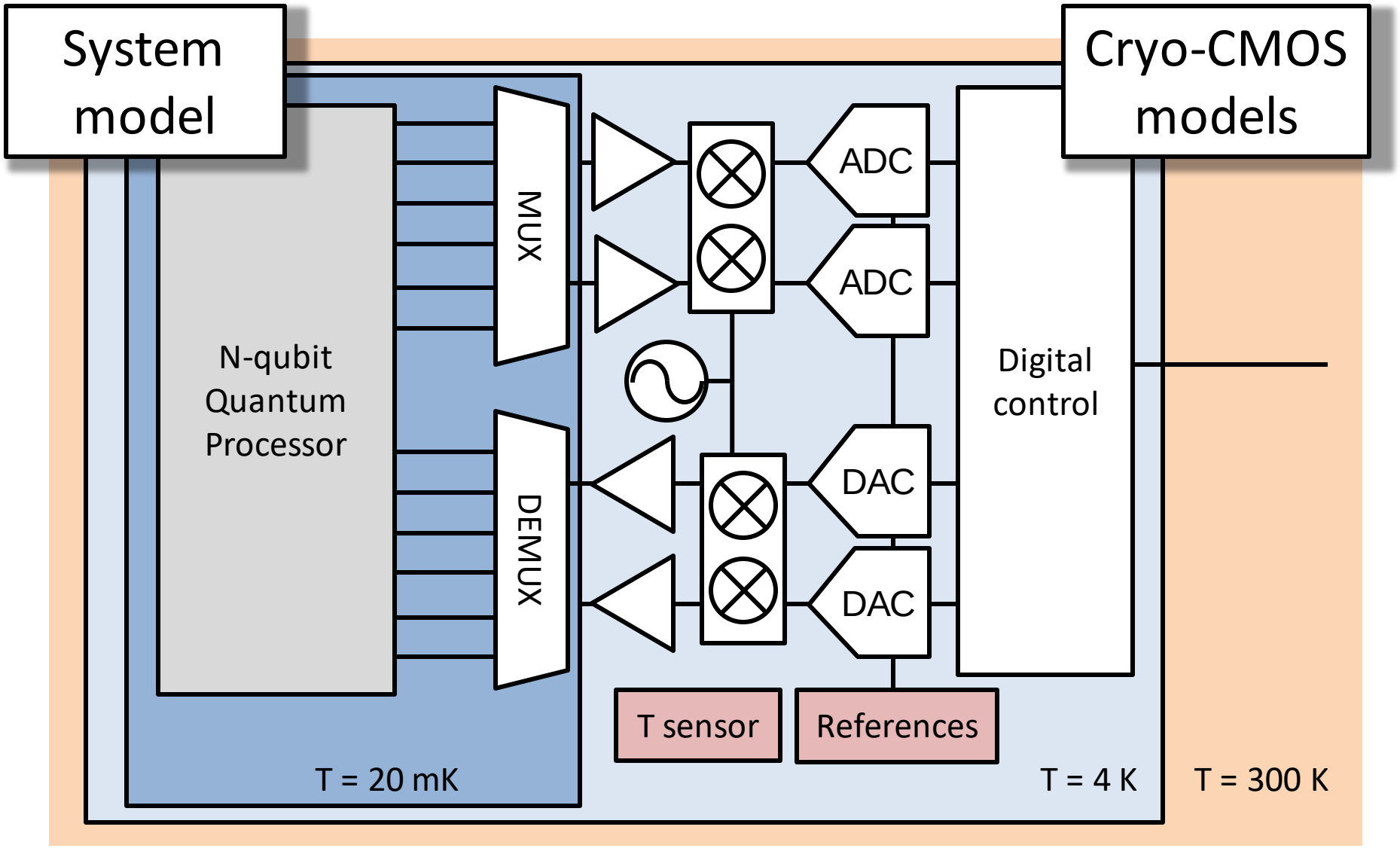


Phase noise



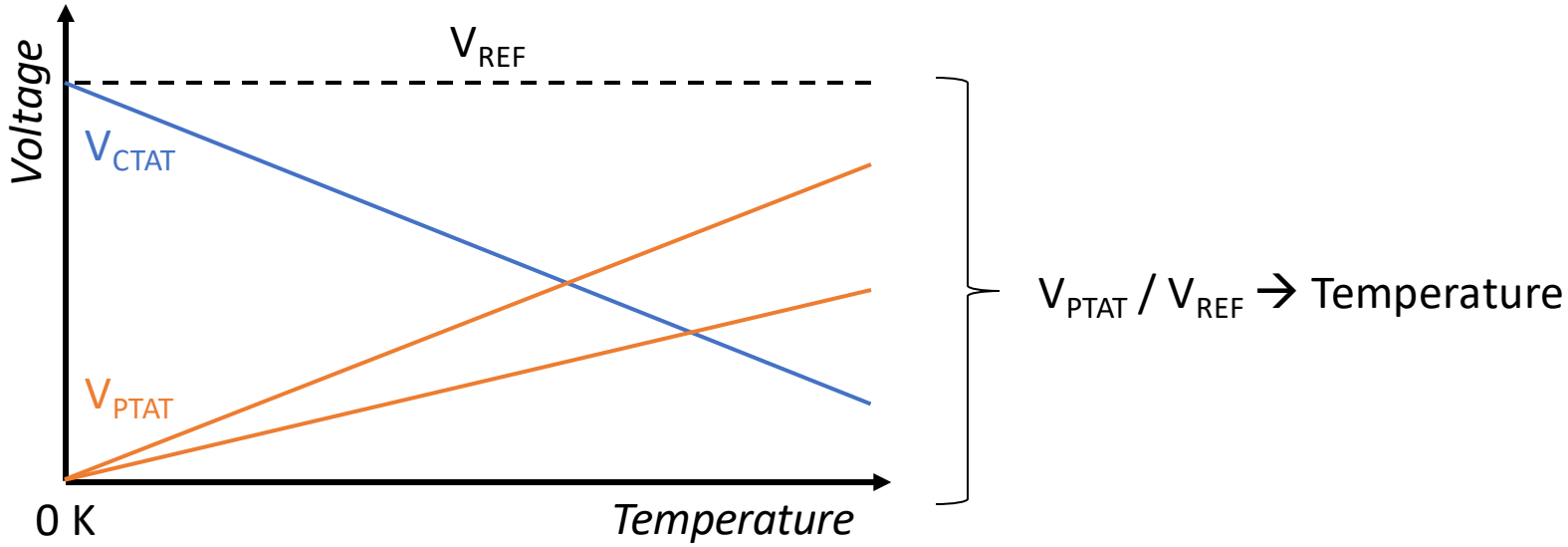
[ISSCC 2017, JSSC 2018]

Circuit Blocks



Cryo-CMOS Voltage References

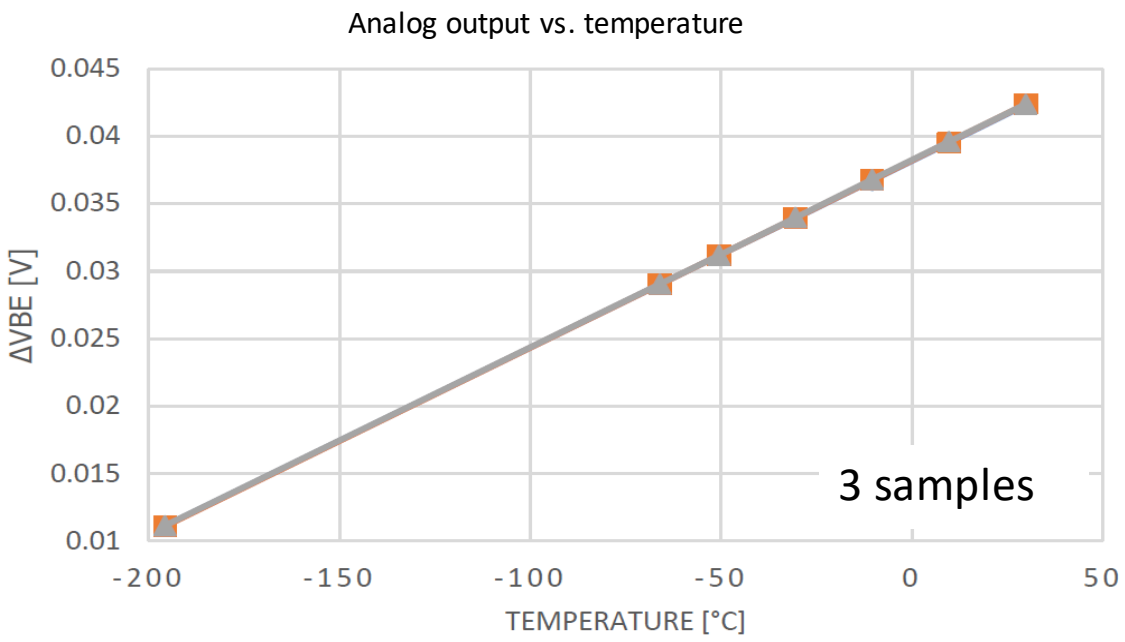
- Principle: Combine two voltages with complementary T-dependence



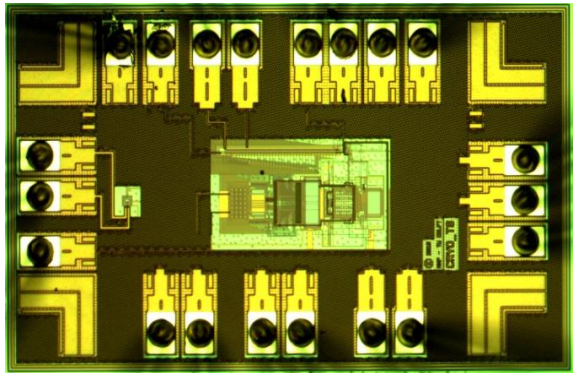
- CTAT: Complementary to absolute temperature
- PTAT: Proportional to absolute temperature

Cryo-CMOS Voltage References

- Principle: Combine two voltages with complementary T-dependence



160-nm CMOS

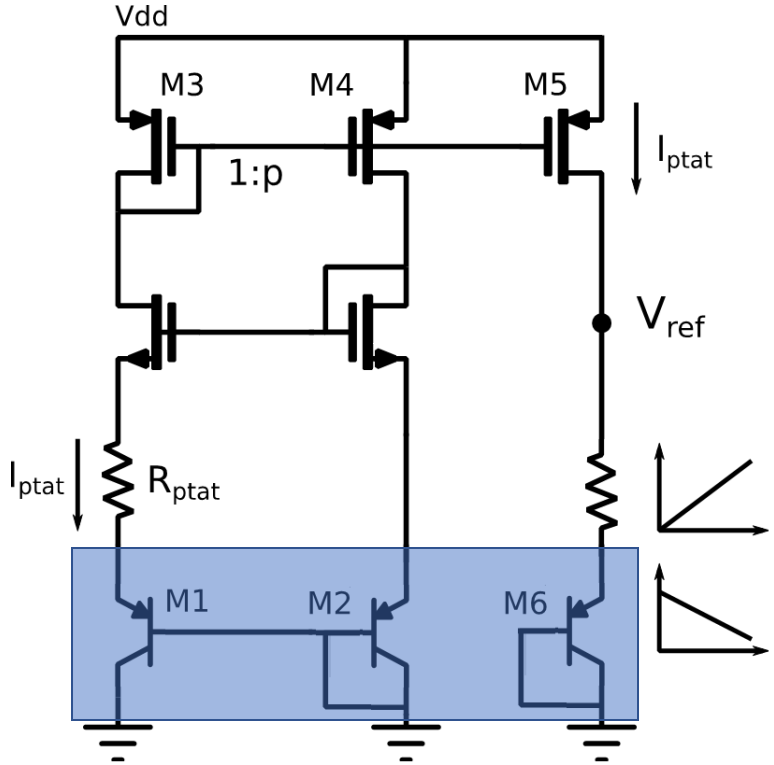


[O. Eniola]

- CTAT: Complementary to absolute temperature
- **PTAT: Proportional to absolute temperature**

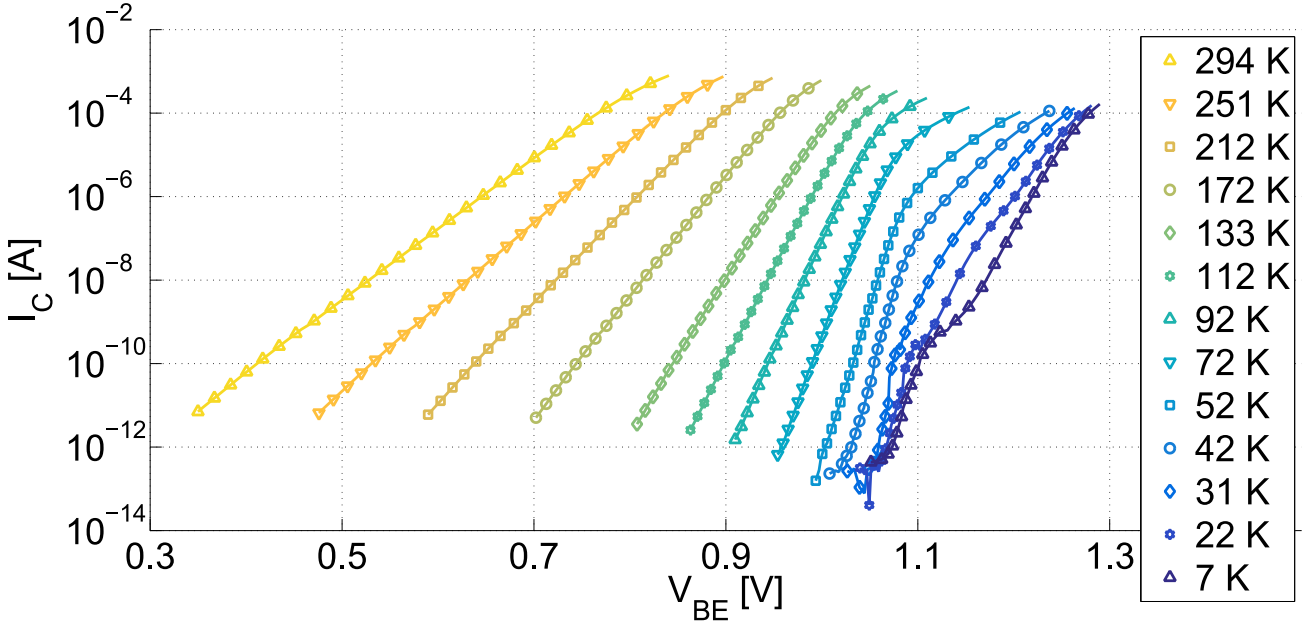
Cryo-CMOS Voltage Reference

- Typical structure:



Bipolar Transistors stop working below ~ 70 K

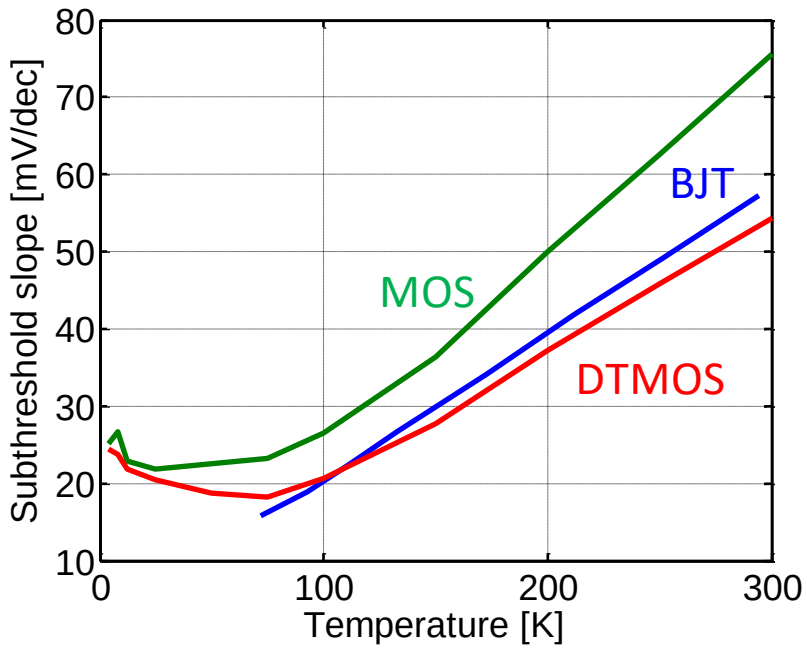
300 K → 7 K

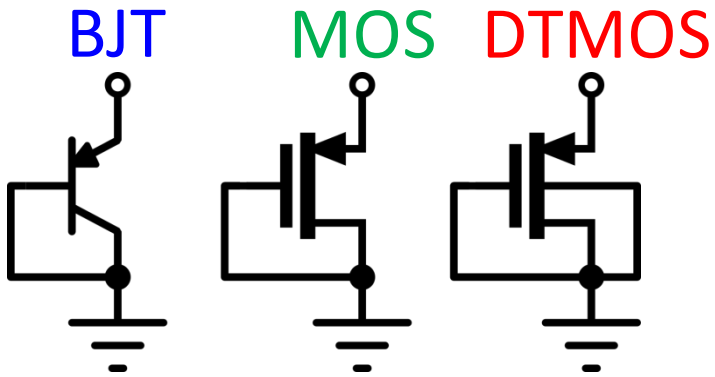


[IEEE Sensors 2016]

Cryo-CMOS references & temp. sensors

- On-going research: which device gives higher accuracy?

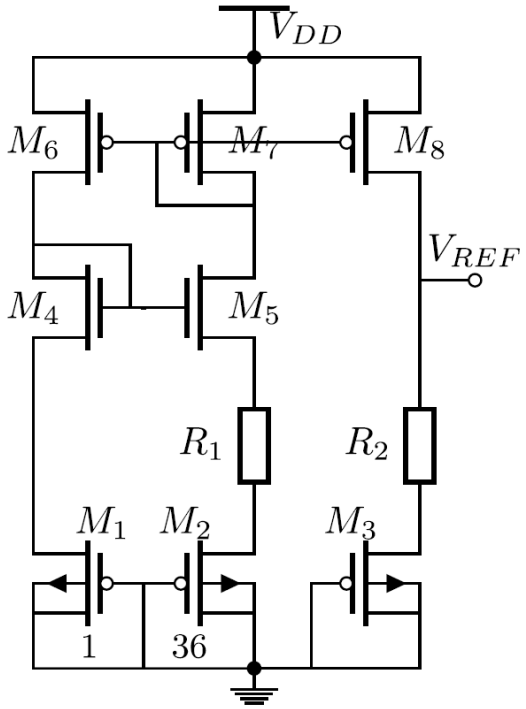


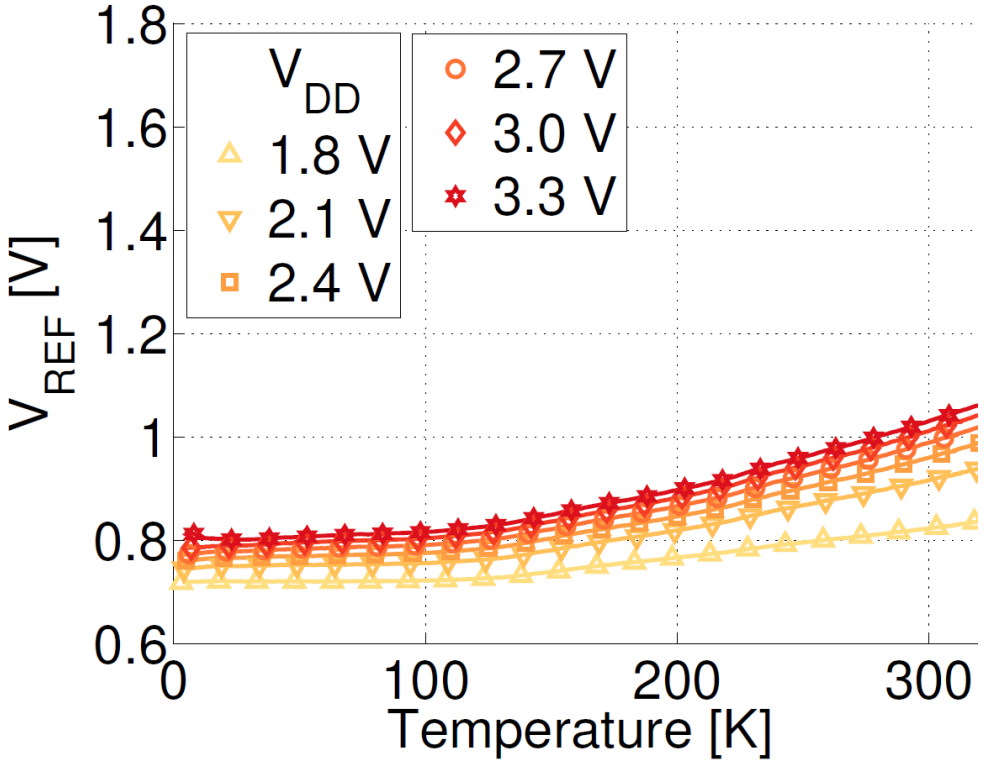


[IEEE JEDS 2018]

A first reference prototype

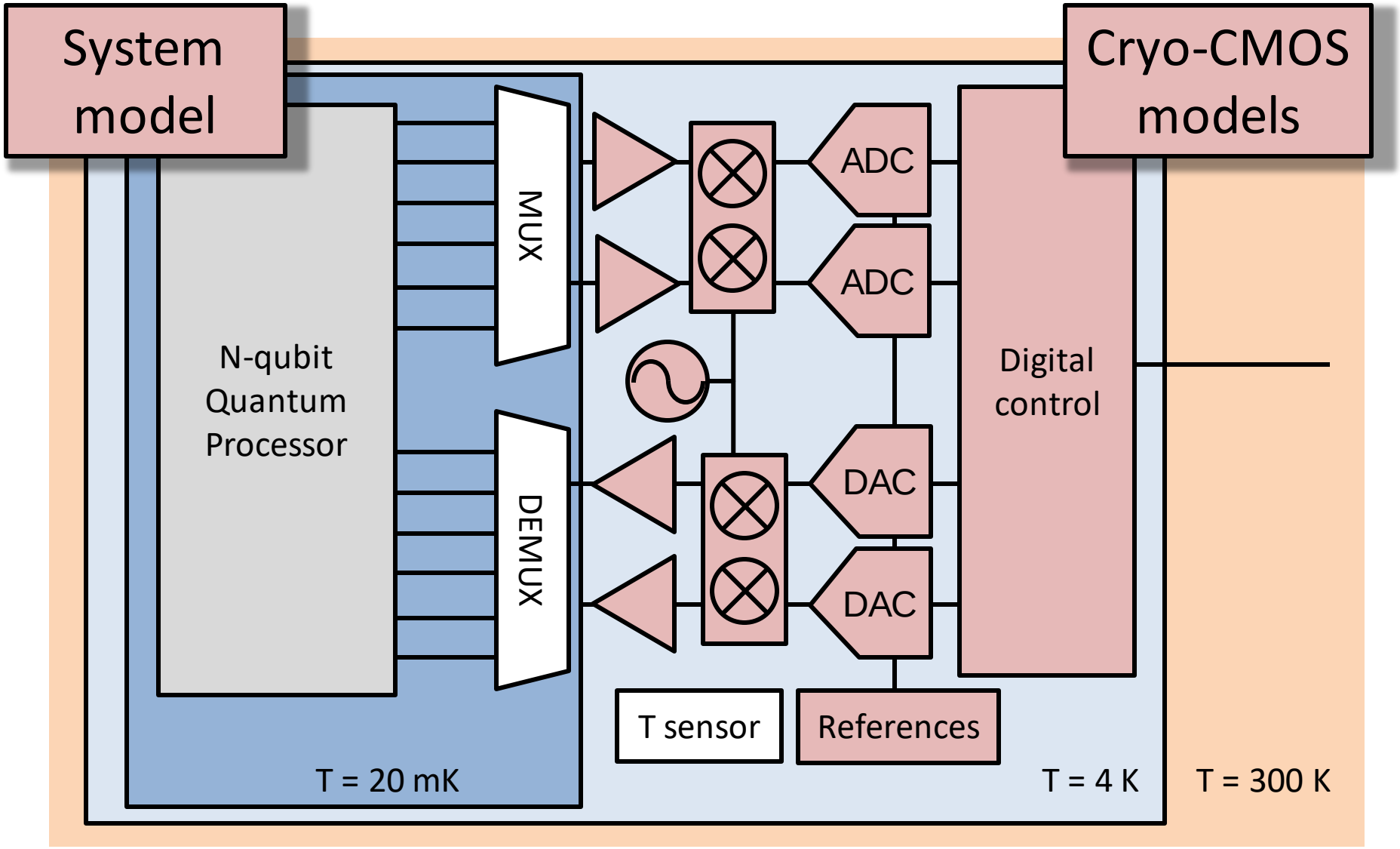
- DTMOS in a classical architecture
- Better than 0.1 %/K from 4 K to 320 K



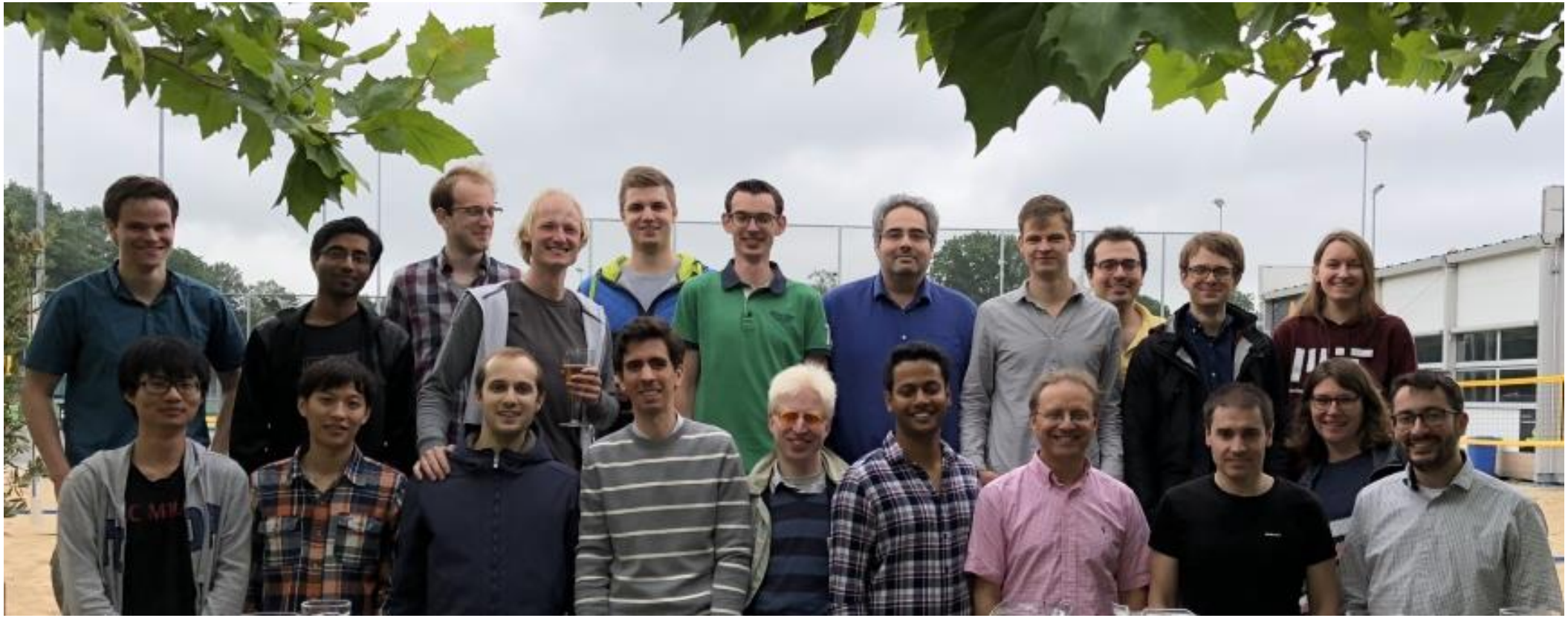


[IEEE SSCL 2018]

On-going Research



Conclusions

- Cryo-CMOS devices operates at 4 K
- Models and analog/RF circuits ⇒ Cryo-CMOS works!
- Circuits can be optimized for QC applications
- VLSI with Cryo-CMOS ⇒ enabler of scalable QC

Acknowledgments