Towards 2-4 K Monolithic Quantum Processors with Control and Readout Electronics in Production 22nm FDSOI CMOS Technology

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FermiLab, June 19, 2019

Outline

- **Proposed monolithic approach**
- Cryogenic characterization of 22nm FDSOI CMOS Technology
- Impact of process variation
- Scaling to higher temperature
- Conclusions

Our approach and goals

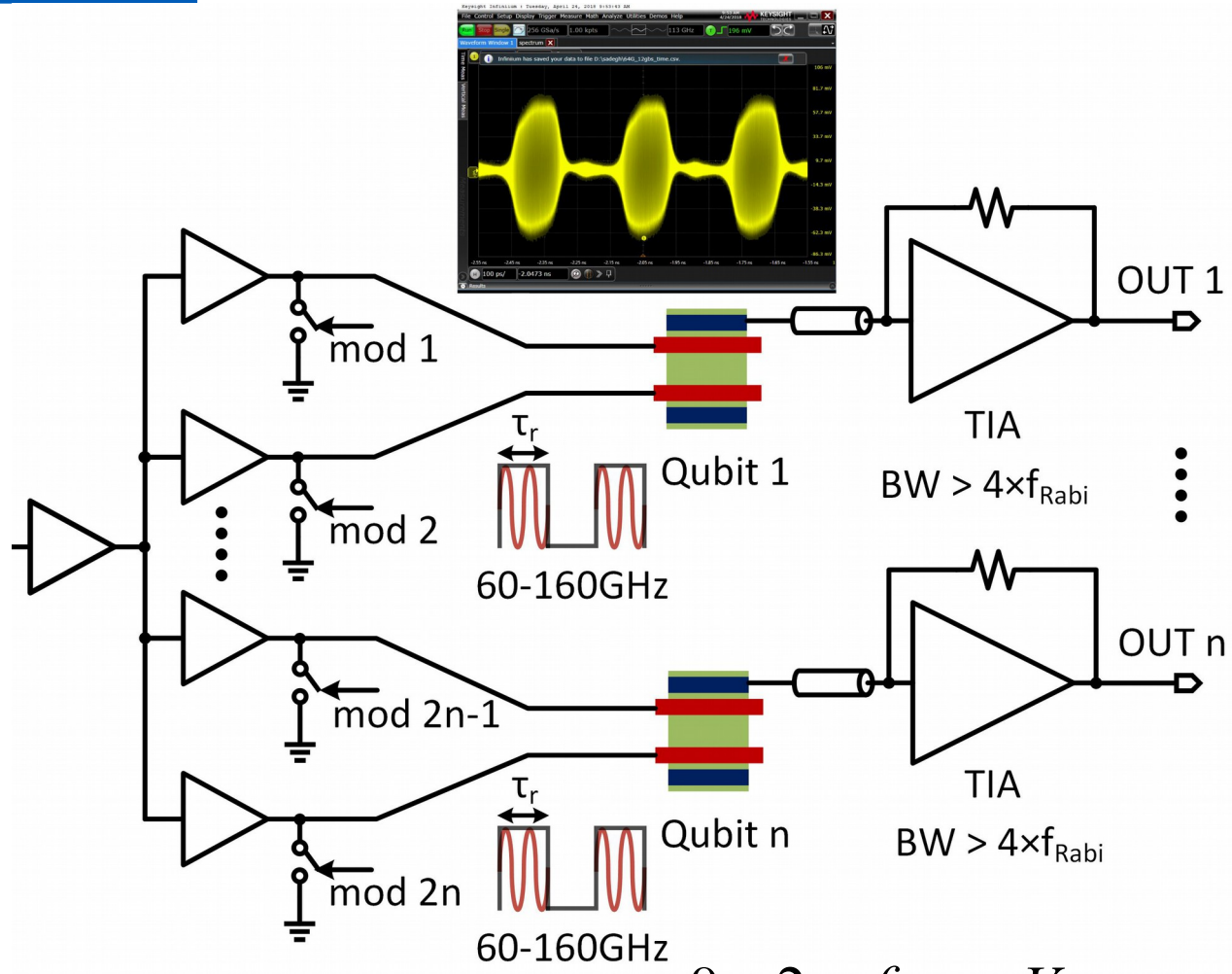
- ***Foundry FDSOI*** CMOS-based QD qubits
  - **SiGe p-MOSFET** with channel/S-D heterojunction for hole spin qubit
- Investigate same and new spin control and readout techniques as SC qubits
- ***mm-wave AMS circuits*** for spin manipulation and readout ***on the same die with the qubits***
- **2-4 *K*** operation now, ***(maybe) 77 K*** in 15 years

Low power monolithic quantum processor

- External low phase noise mm-wave signal
- Broadband mm-wave (FDM) signal distribution
  - 60-100 GHz for 4-6 K operation
  - 140-220 GHz for 8-12 K operation
- n-MOS switch pulse modulators >40dB isolation
- Current or dispersive readout < 5 mW per qubit
- 50Ω chip inputs and outputs
- SRAM to store the pulse sequences

Example:

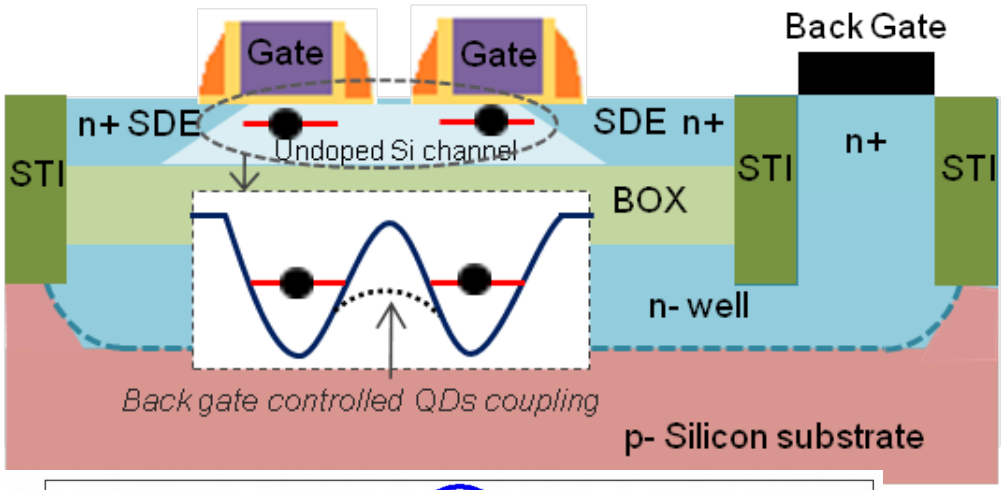
- 200 qubits with individual readout: 1 W
- mm-wave ESR signal distribution: 200 mW
- Switches do not consume power

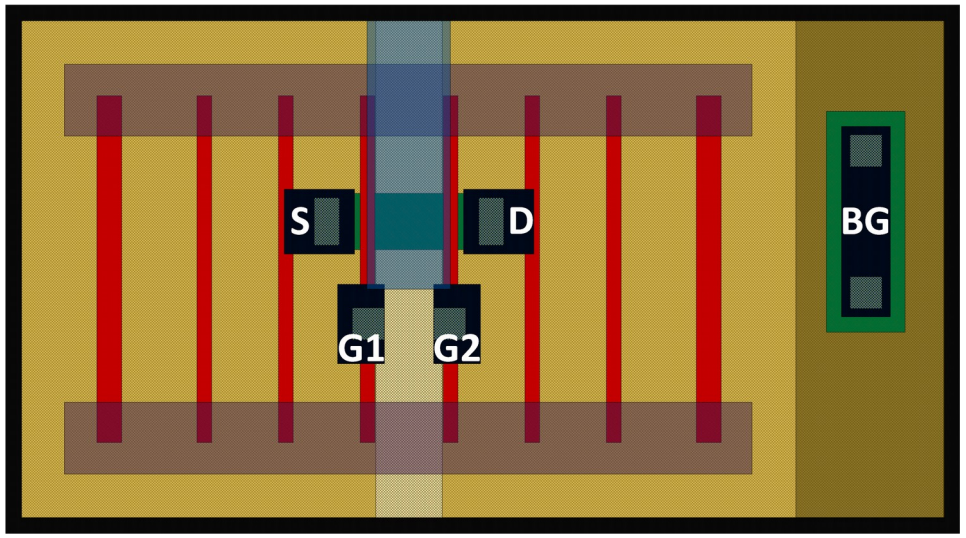


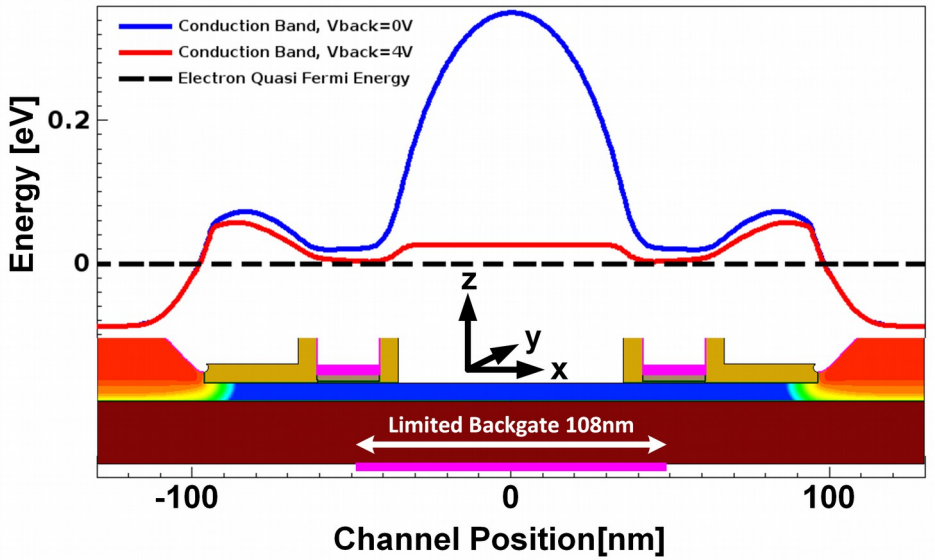
[S.Bonen et al. EDL 2018]

$$\theta = 2\pi f_R \tau \propto V_{mmw} \tau$$

Electron- and hole-spin DQD concept in FDSOI

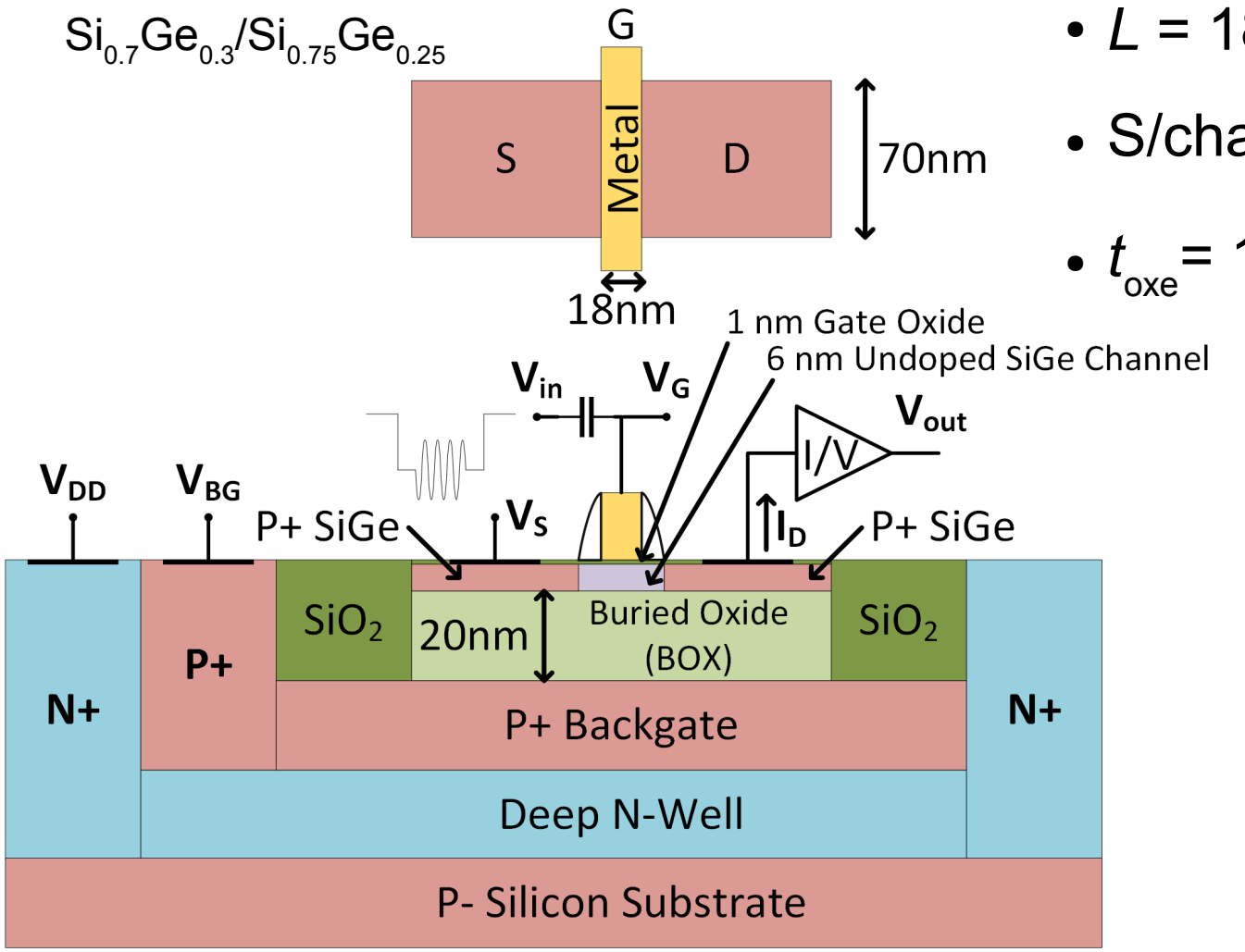




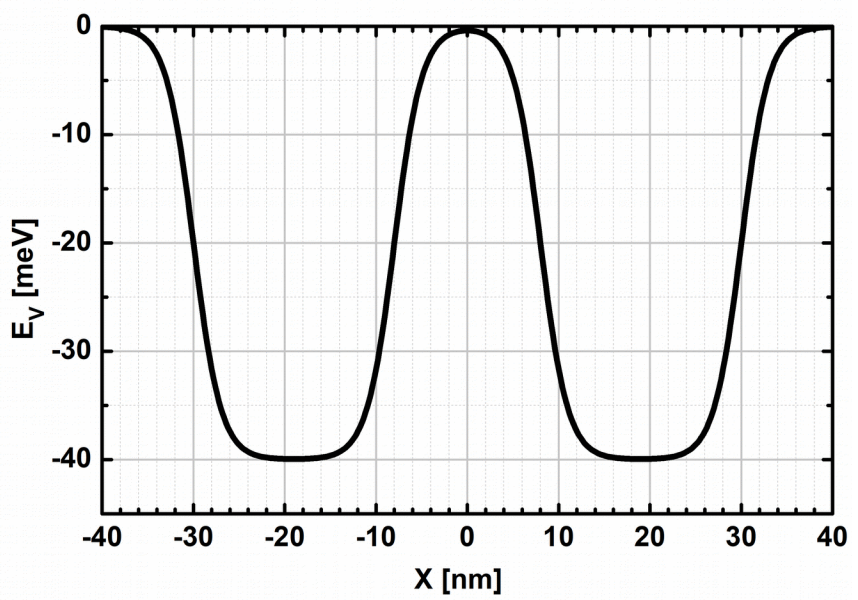


- Double-dot qubit (C-NOT) = 2-gate MOSFET cascode
- Quantum dot (QD) under each top gate
- Individual gate control of each QD
- Potential barrier between dots
- Back gate for entanglement control **(needs special mask)**
- mm-wave E-field applied on gate and *z*-axis dc magnetic field

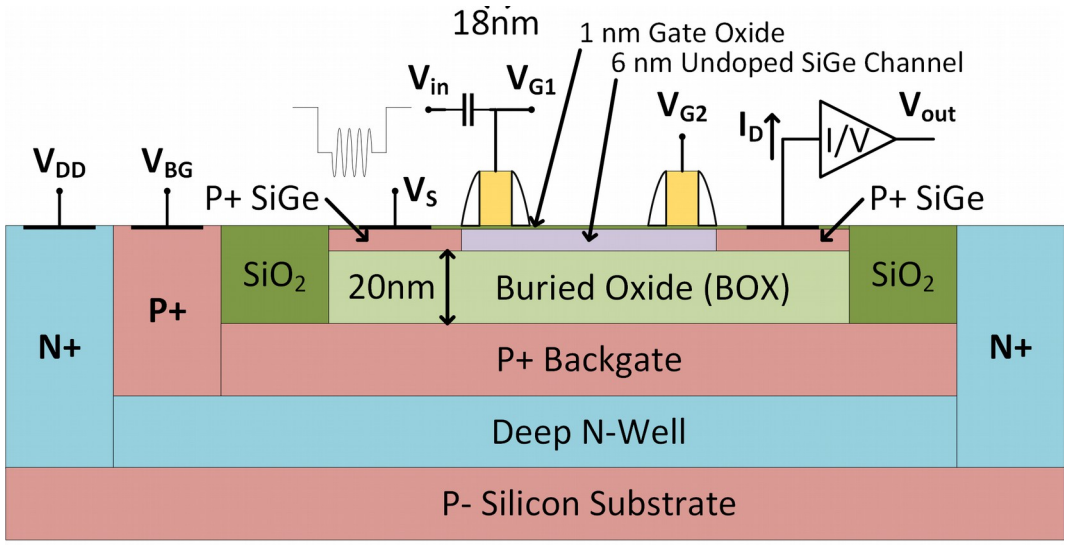
The SiGe p-MOSFET is the SiGe hole-spin qubit

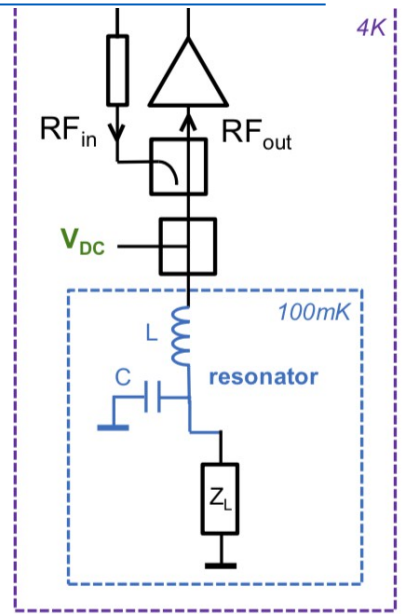


- L = 18 nm; W = 70 nm
- S/channel heterojunction: ΔE_V = 35-40 meV
- t_{oxe} = 1 nm => larger EDSR, f_R

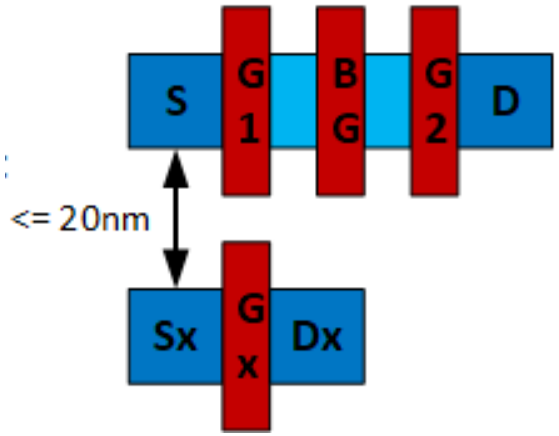


Spin readout approaches need ultra low noise amp.





L. Hutin
IMS 2019



- Spin blockade filter with TIA current readout: destructive, good for Rabi frequency characterization
- Capacitive charge sensor with SET and TIA current readout
- mm-wave off-resonance reflection with (SET) resonator, coupler and mm-wave tuned LNA: large area, Q?

Comparison to other qubit families

- >20x f_L, f_R compared to SC qubits:
  - > 20^2x smaller readout resonators, > 20x higher operation temp.
- Larger $\boldsymbol{g}$, f_R than vertically stacked SiGe/Si/SiGe FinFET qubit
- Backgate control for circuit V_T adjustment at low temperature
- Potential selective fast backgate for CNOT gate
- All spin control/readout schemes from SC qubits can be used

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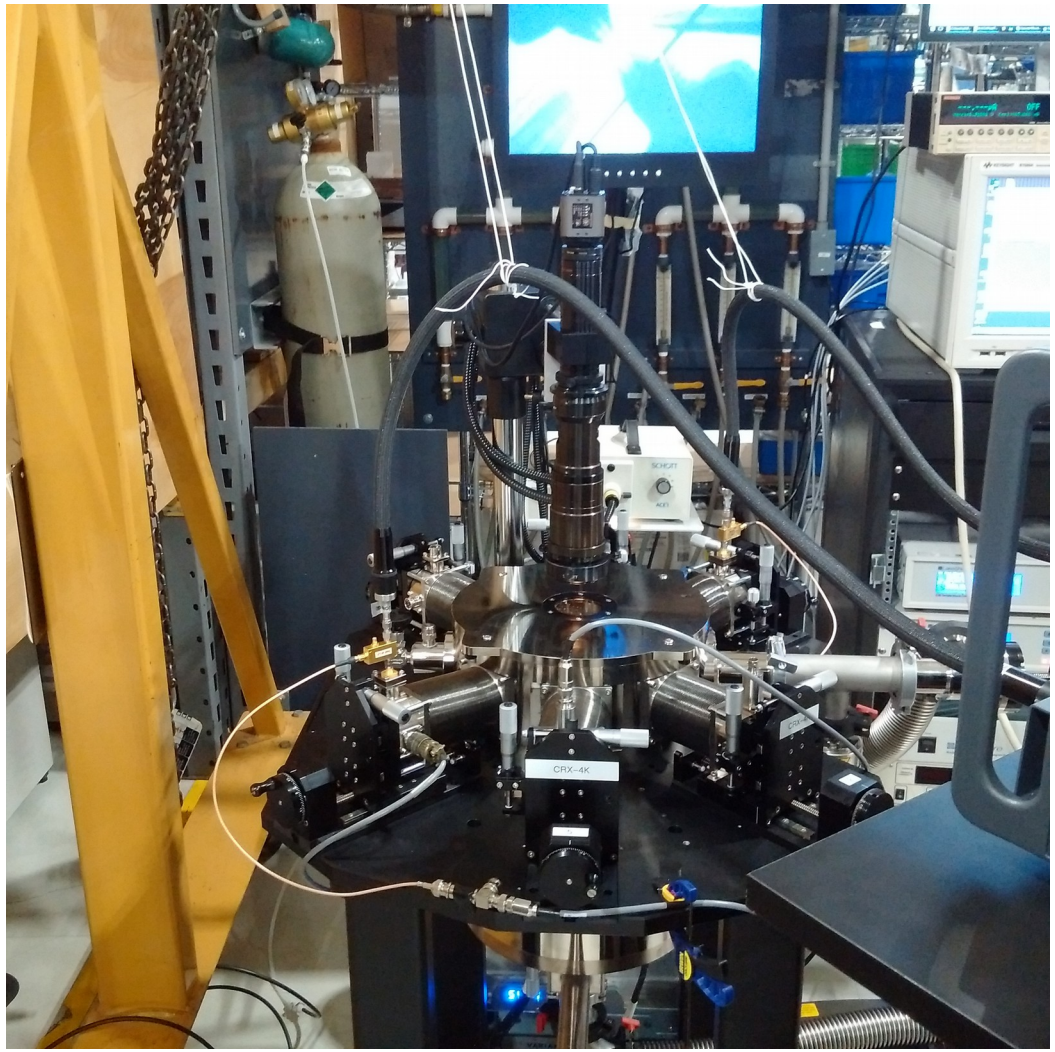
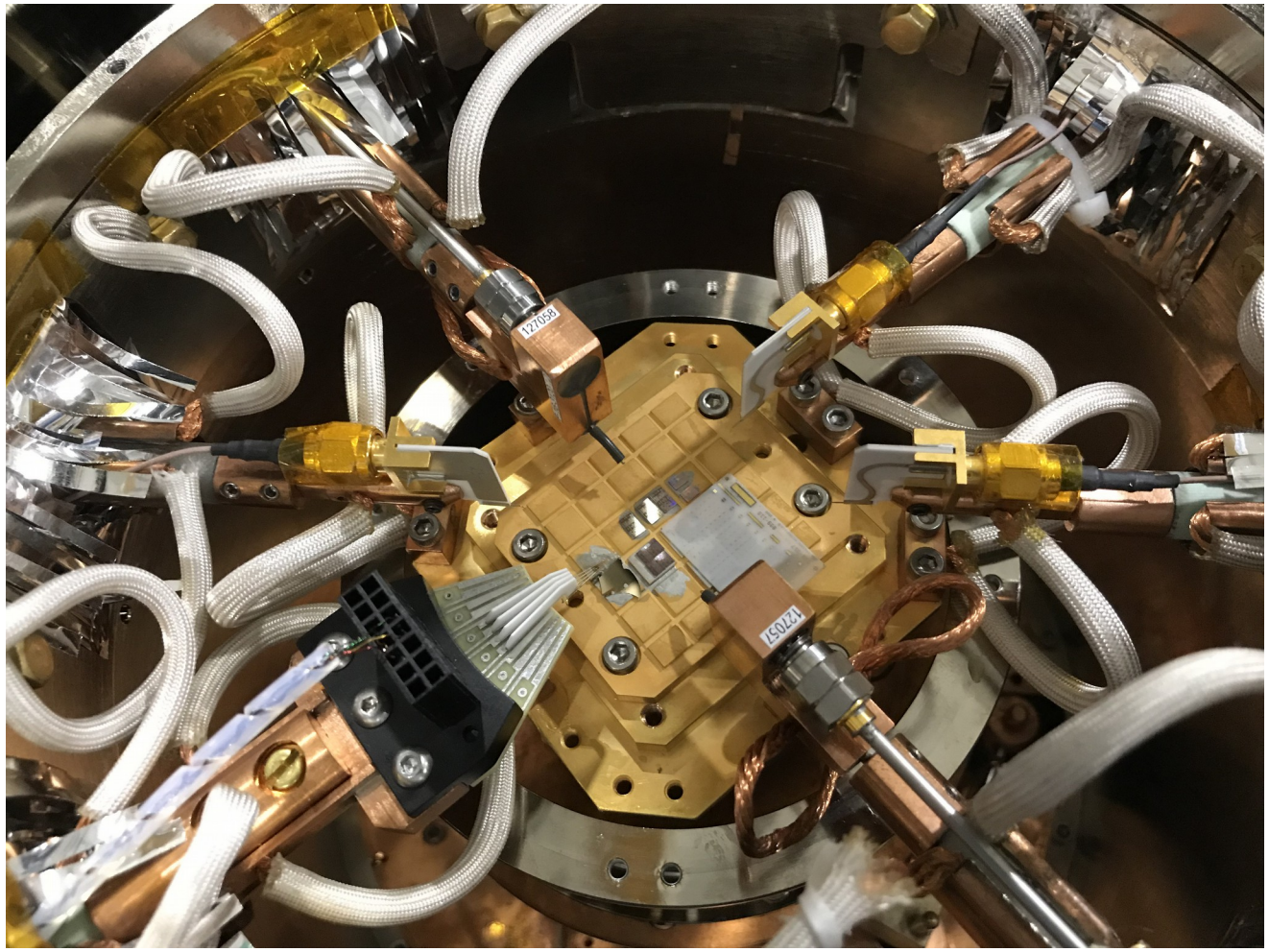
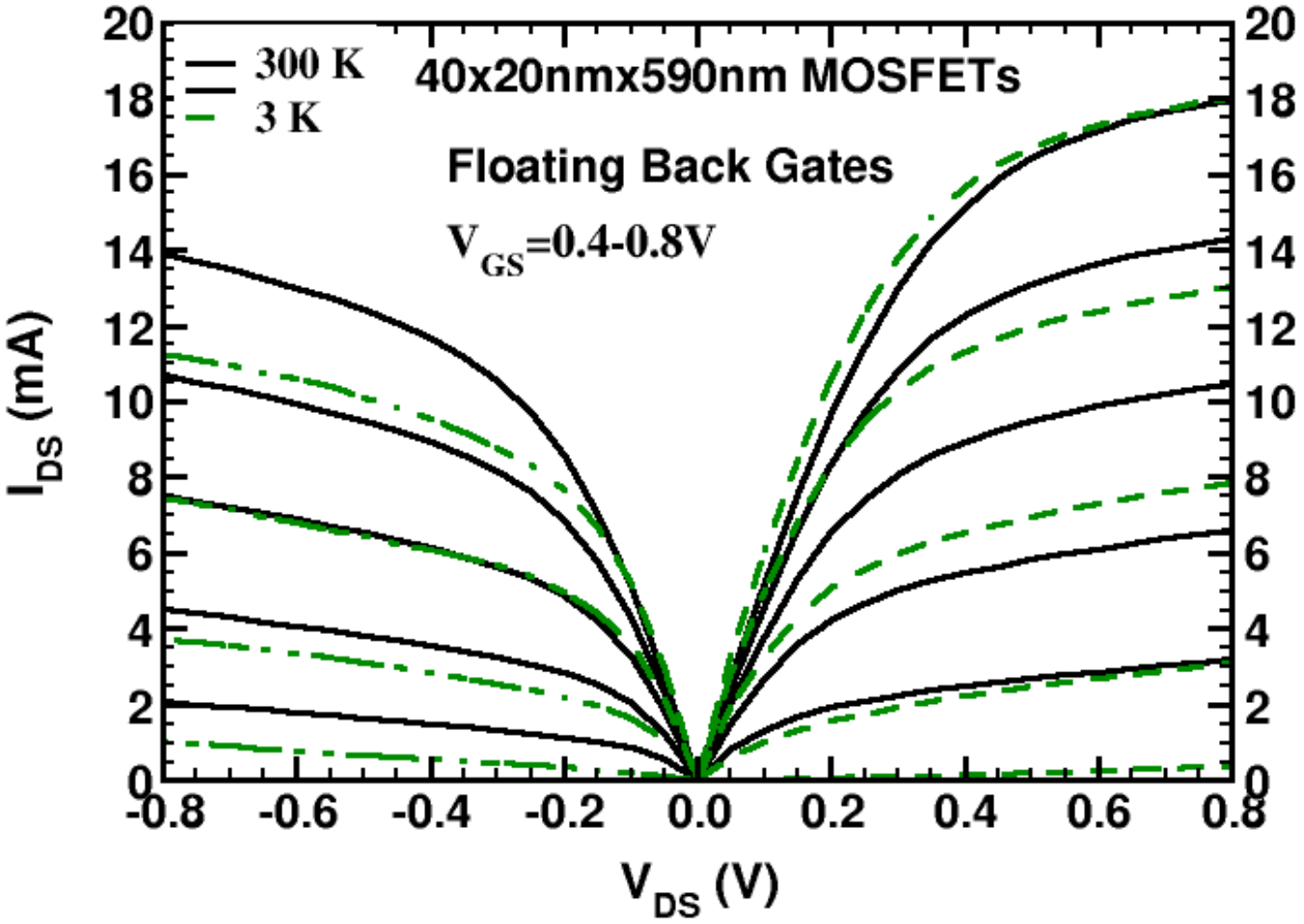
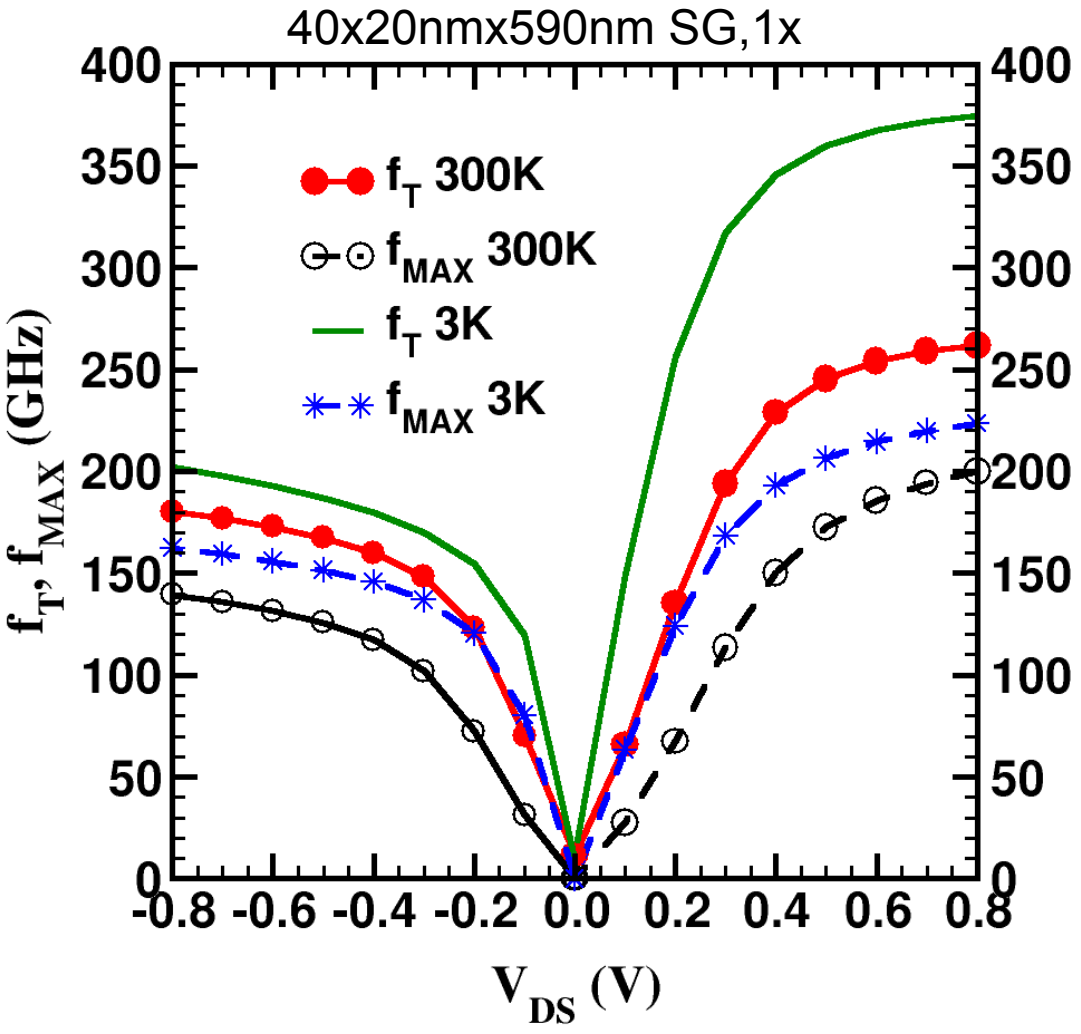
Measurement set-up at 2 K



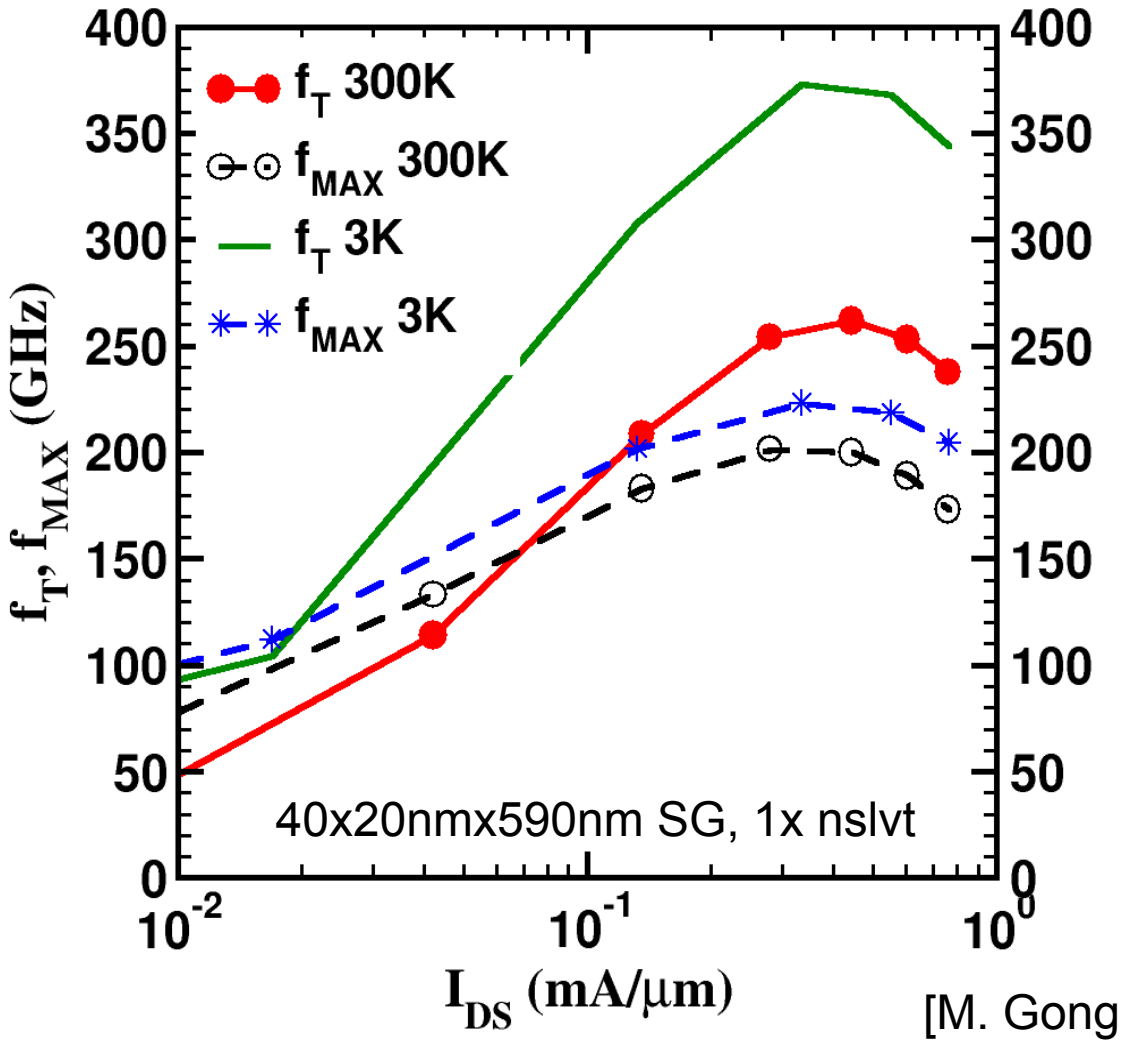


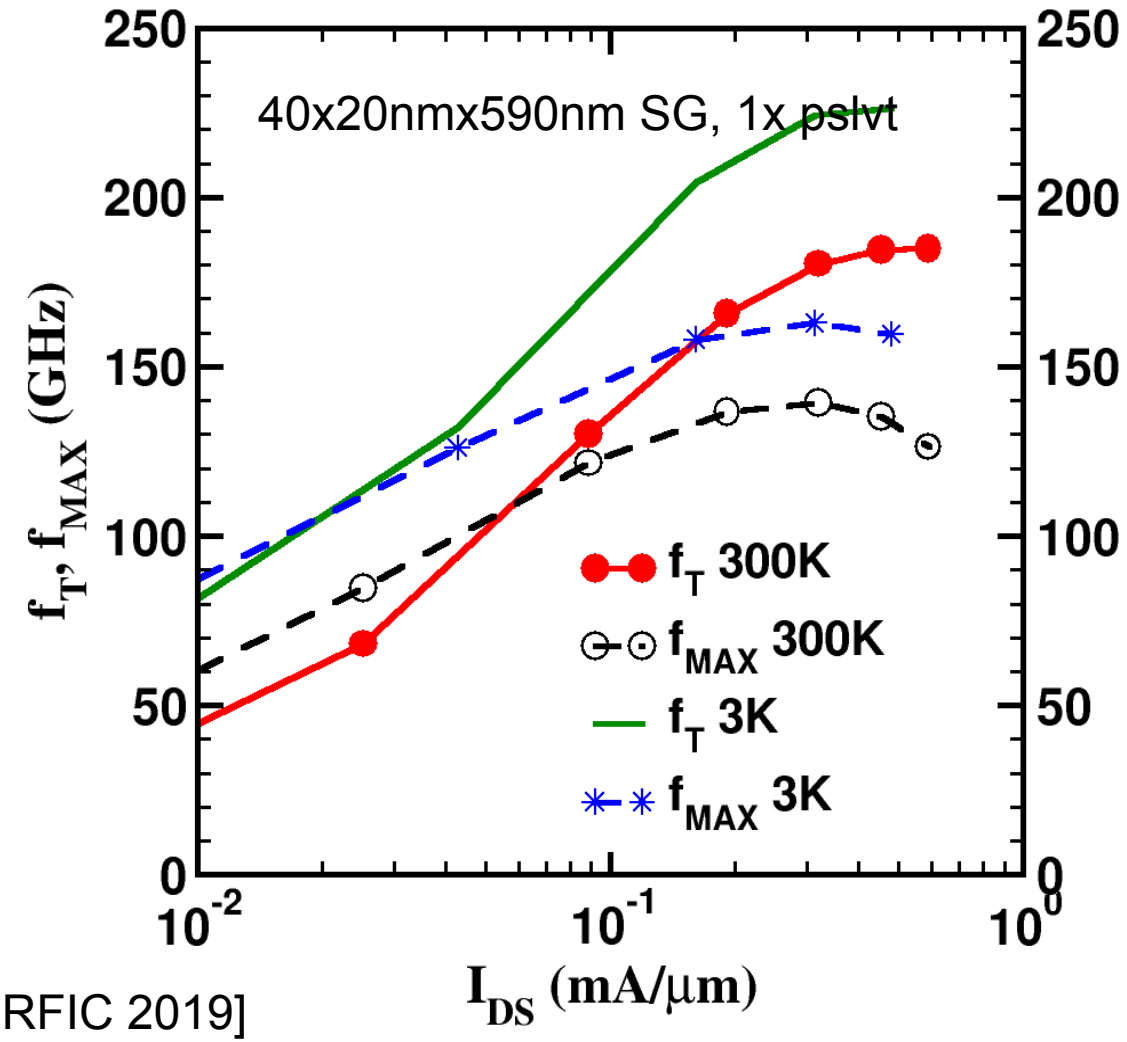
“Classical” MOSFET behaviour in saturation





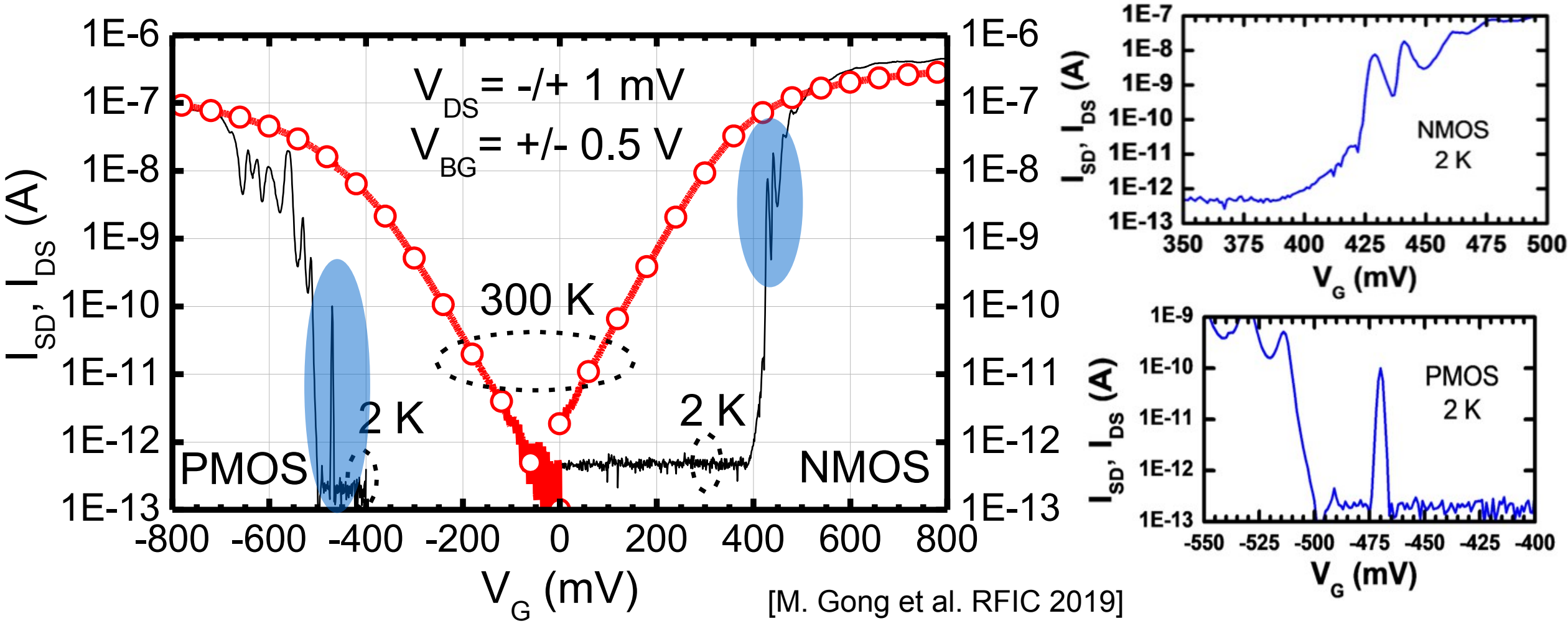
Peak f_T, f_{MAX} current densities invariant with temp.





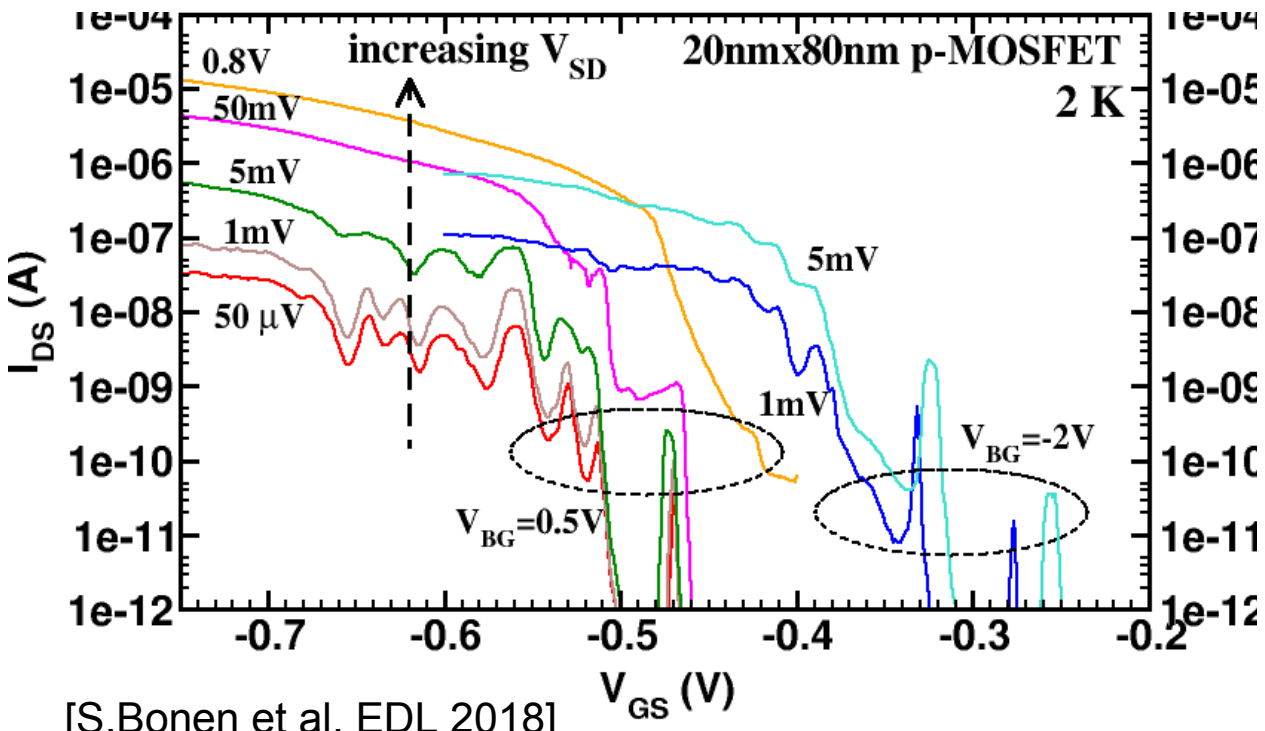
[M. Gong et al. RFIC 2019]

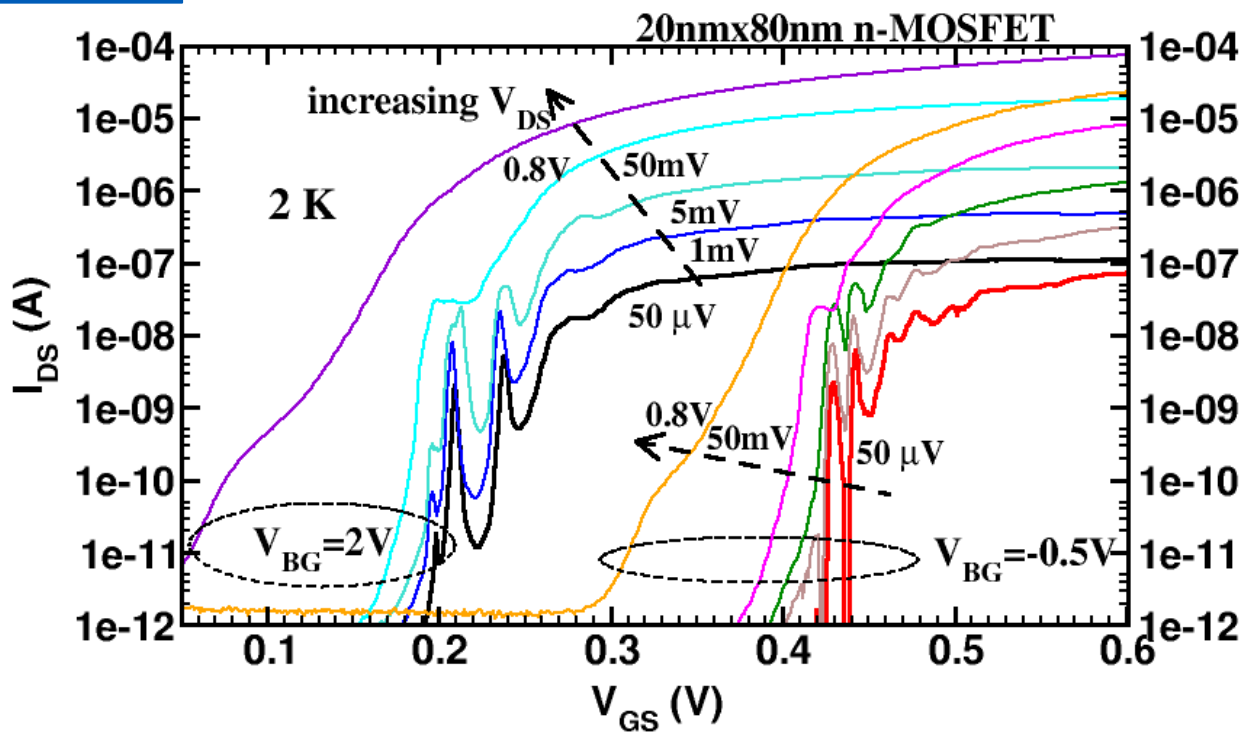
Quantum behavior at low V_{DS} and 2 K



[M. Gong et al. RFIC 2019]

Energy level spacing tuneable from backgate

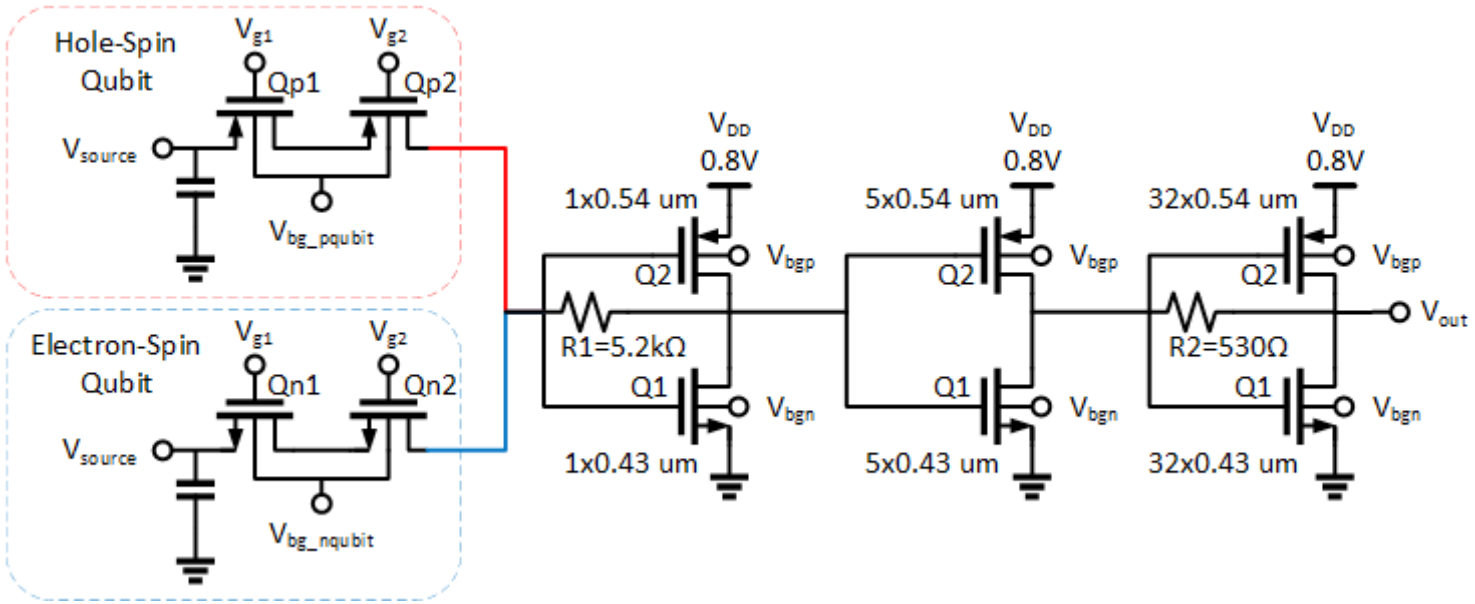


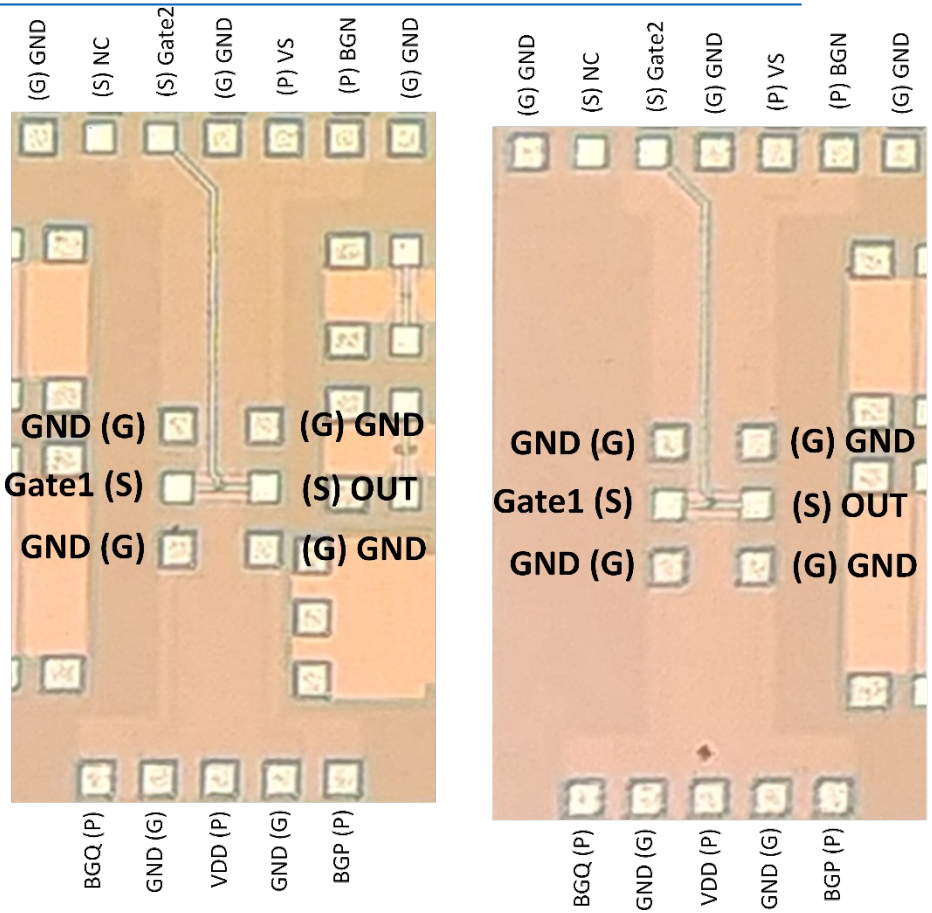


[S.Bonen et al. EDL 2018]

ΔV_{GS} increases (doubles) at +/-2V back gate voltage as C_{gs} decreases

Monolithic integration of qubits and readout TIA

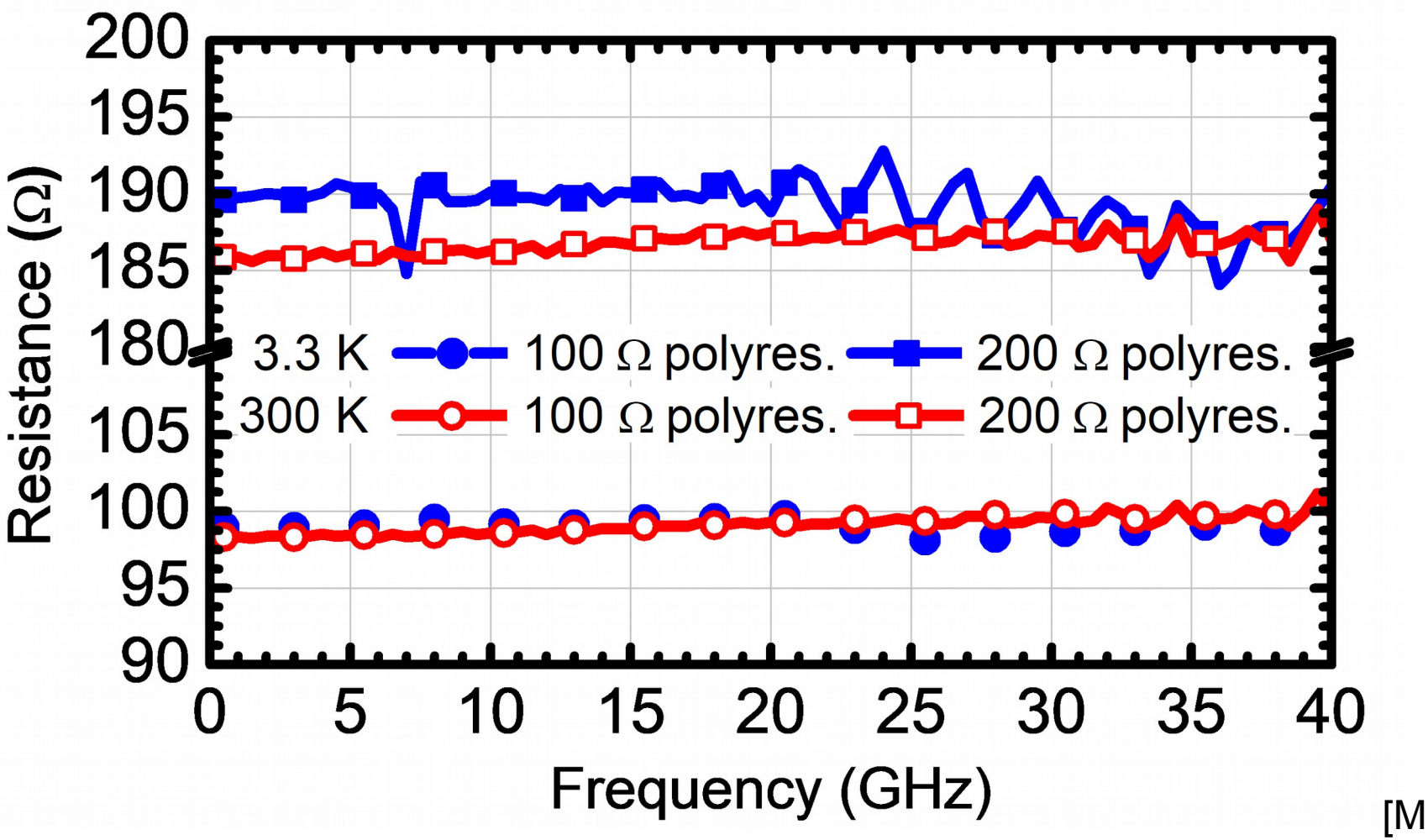




Challenges:

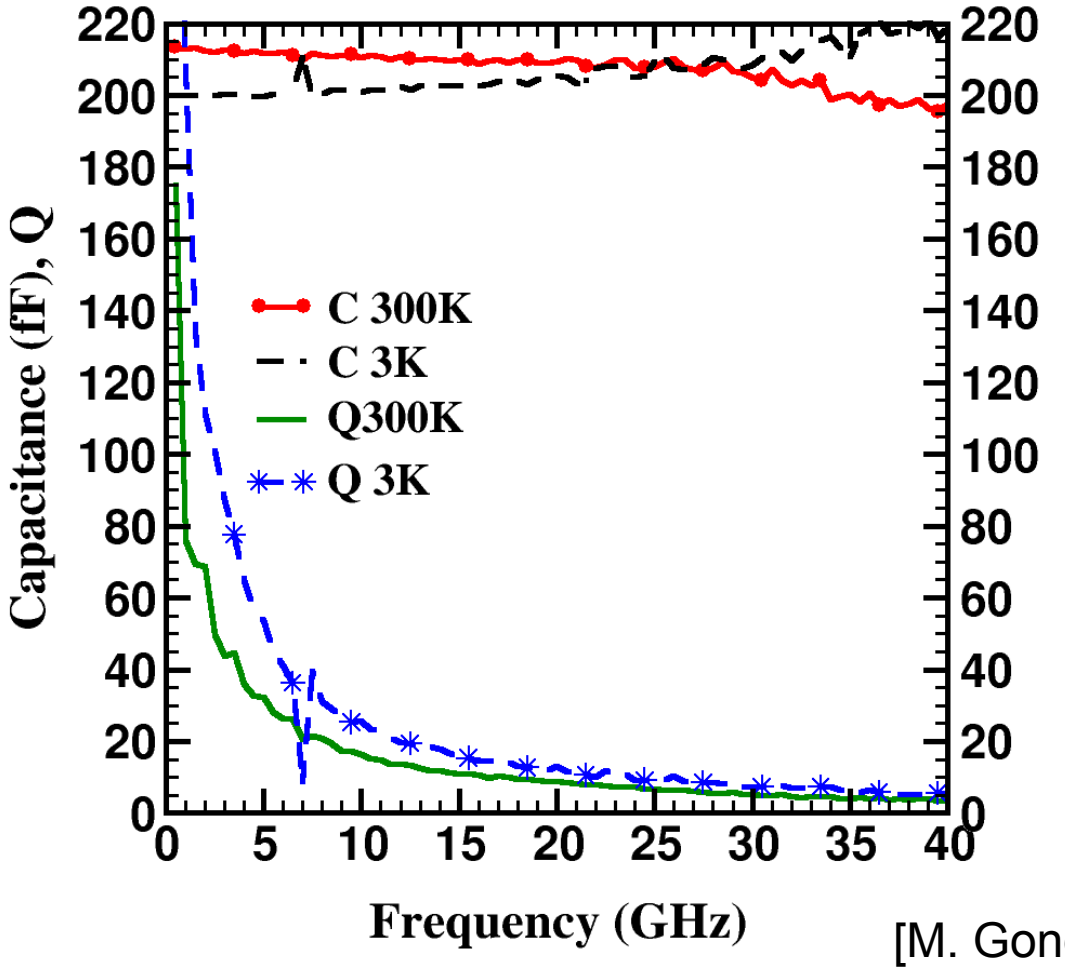
- Large gain, low power
- Bandwidth, noise
- Drive 50 Ω off chip with minimum size 1x18nmx70nm MOSFET
- Design kit models valid at 2-4 K

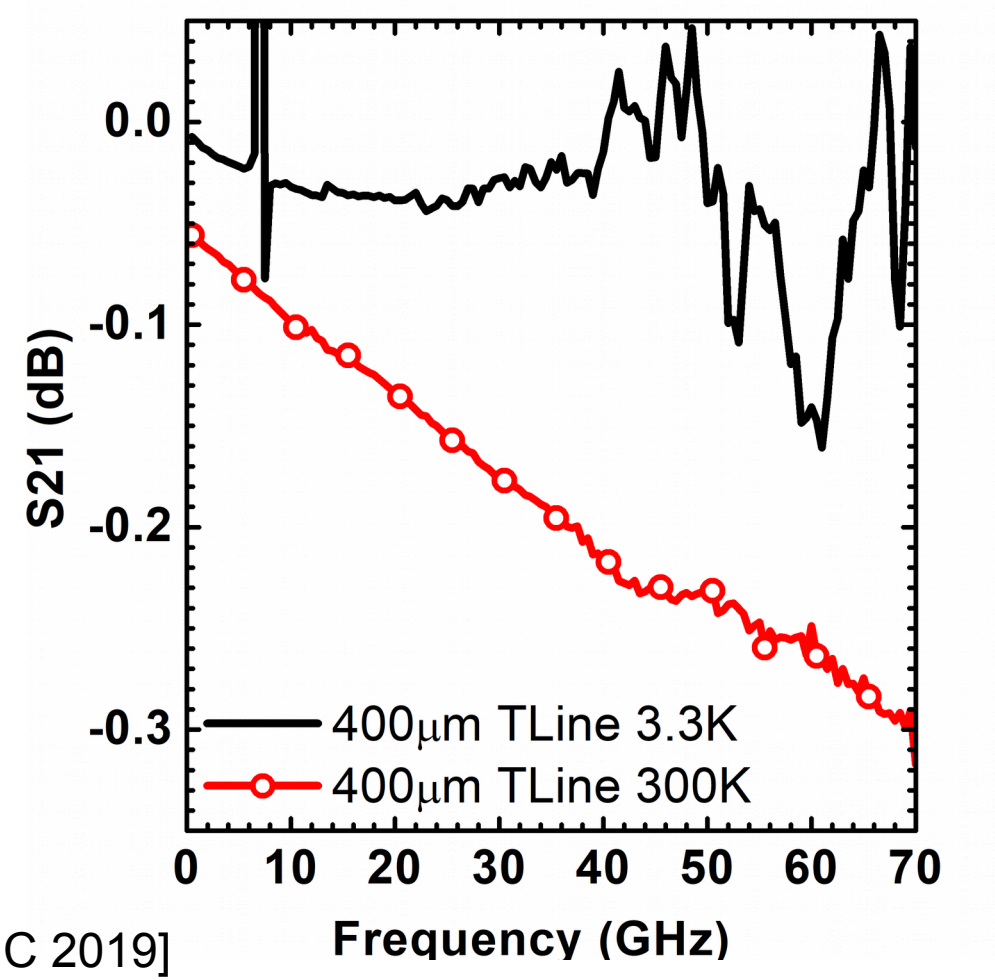
R_{poly} does not change over temperature



[M. Gong et al. RFIC 2019]

MoM Cap does not change but Q improves at 3 K



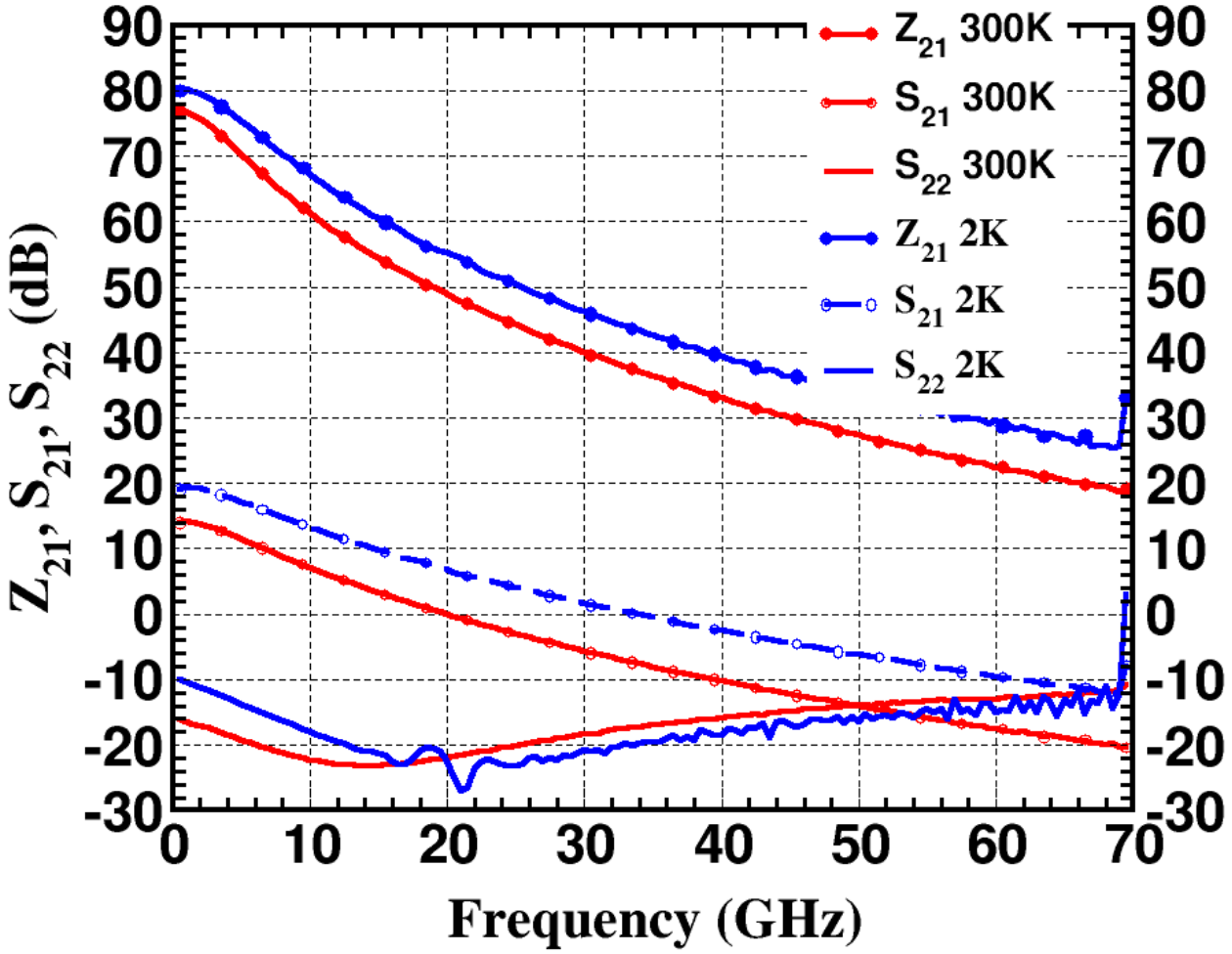


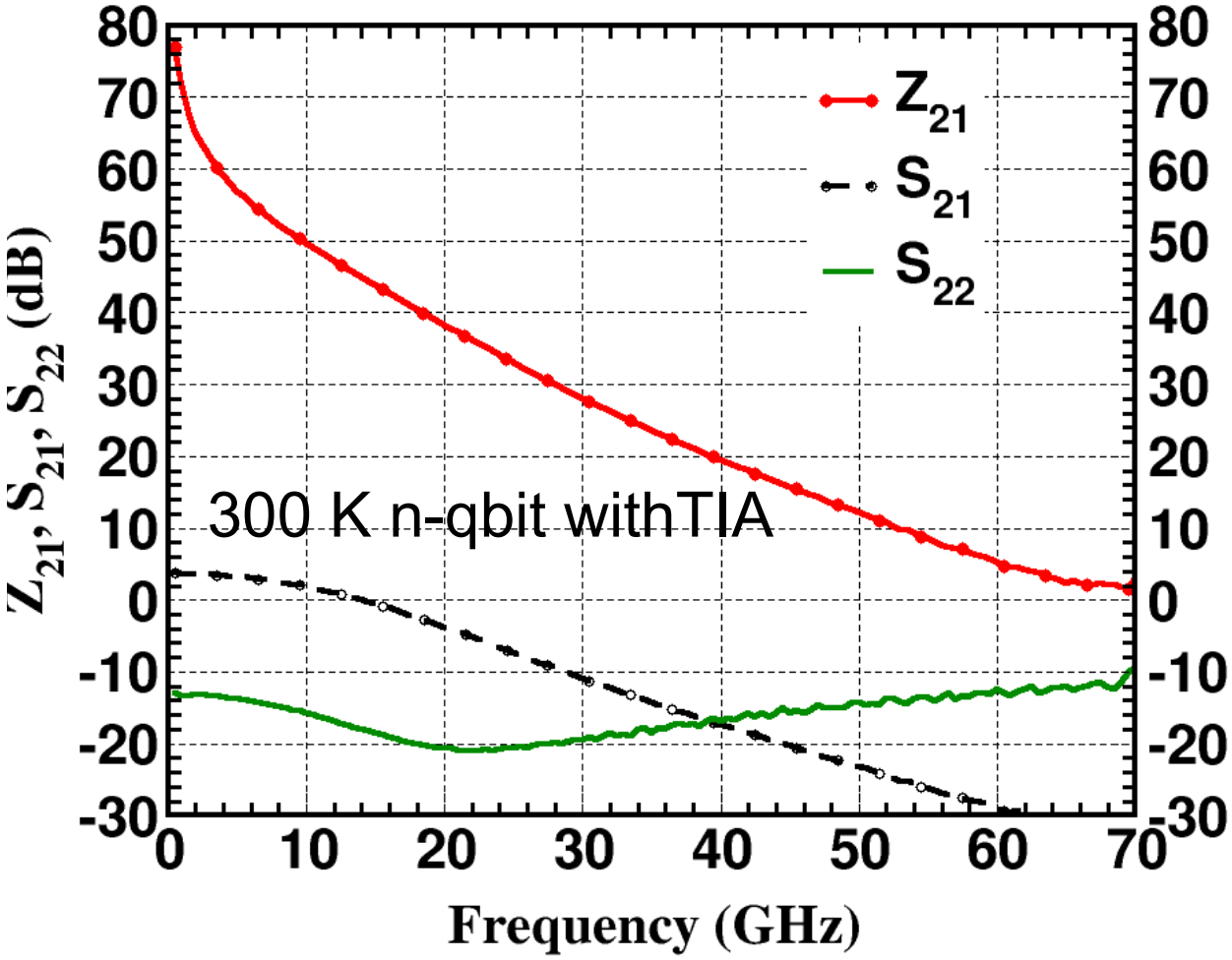
[M. Gong et al. RFIC 2019]

TIA and n-qubit+readout circuit vs. temperature

TIA

[S.Bonen et al. EDL 2018]

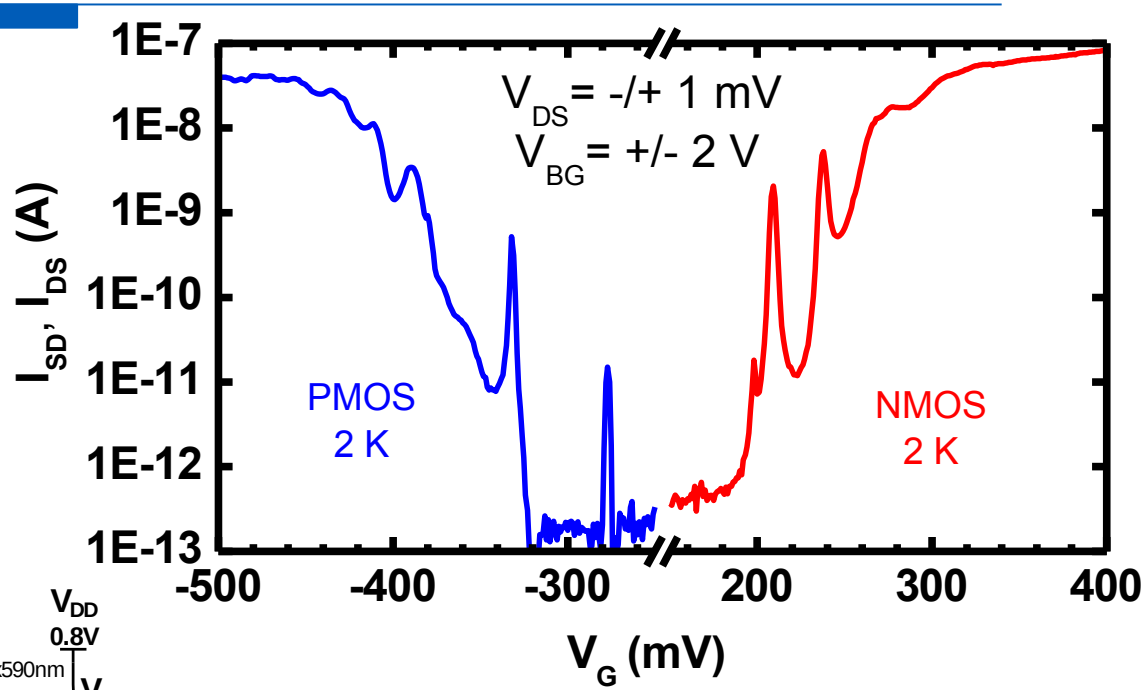


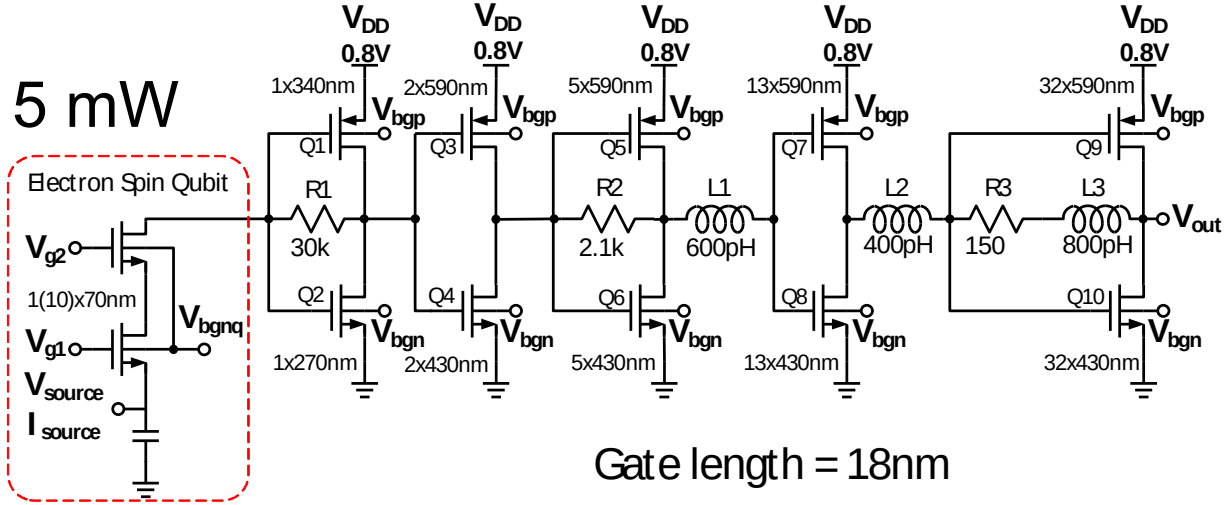


Specification and optimal TIA design for readout

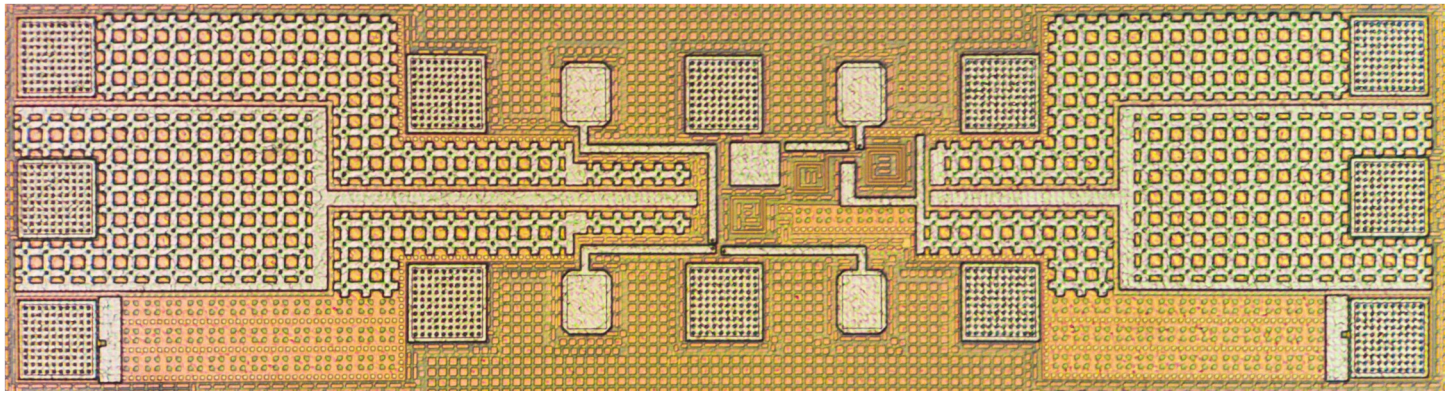
- Amplify 1pA...1nA to 10 mV

  => Z_{21} > 110 dBΩ
- Lowest possible noise
- BW > f_L /20 (f_L = 60-160 GHz)
- Z_{out} = 50 Ω
- P_{DC} < 5 mW



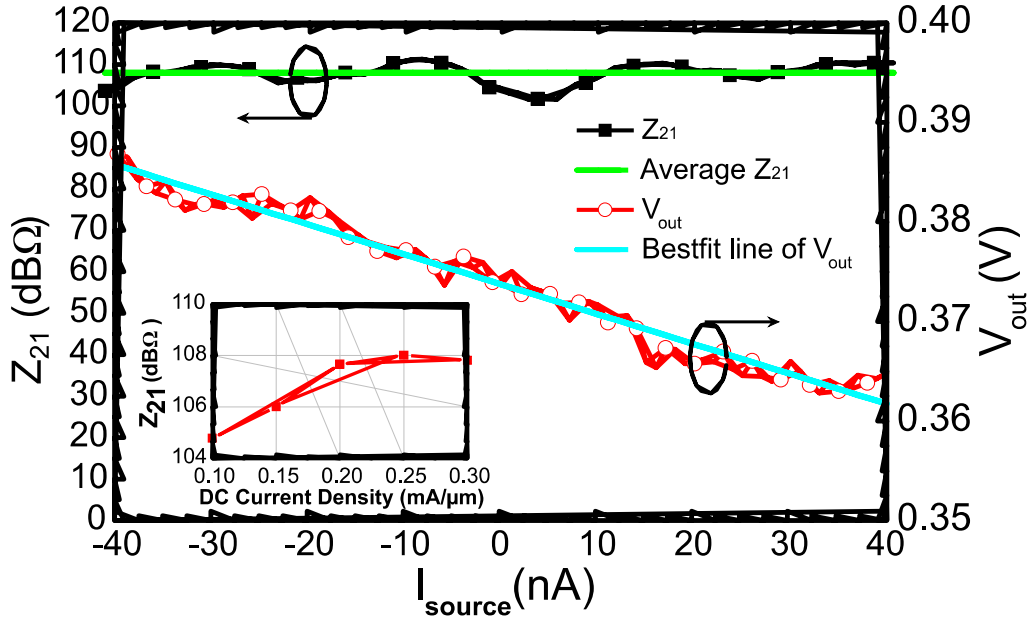


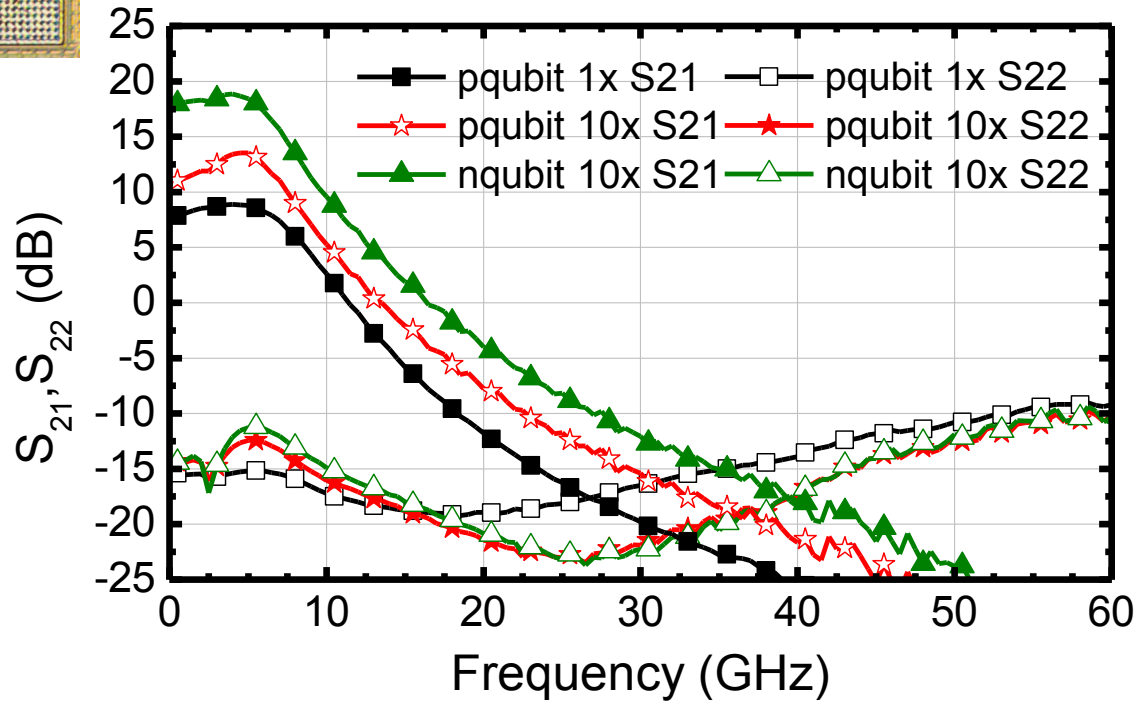
10 coupled double QD qubits with TIA readout



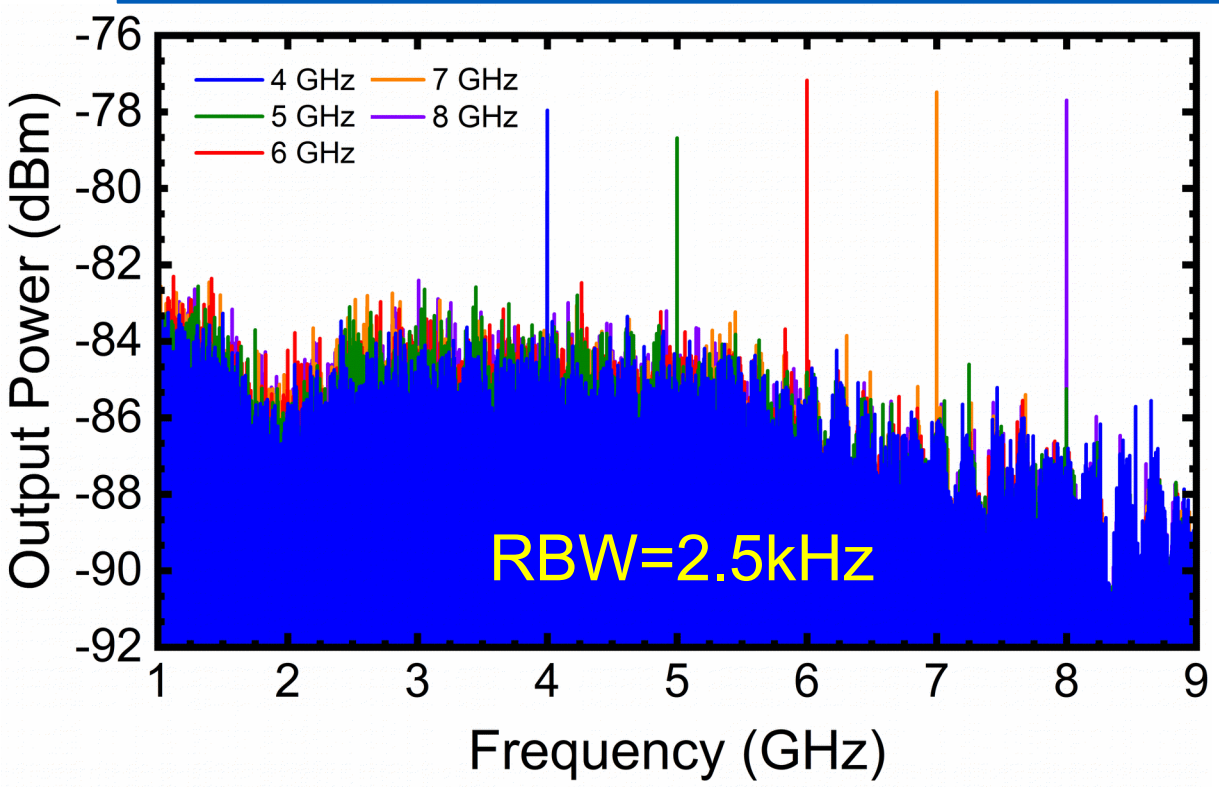
Improved gain and bandwidth

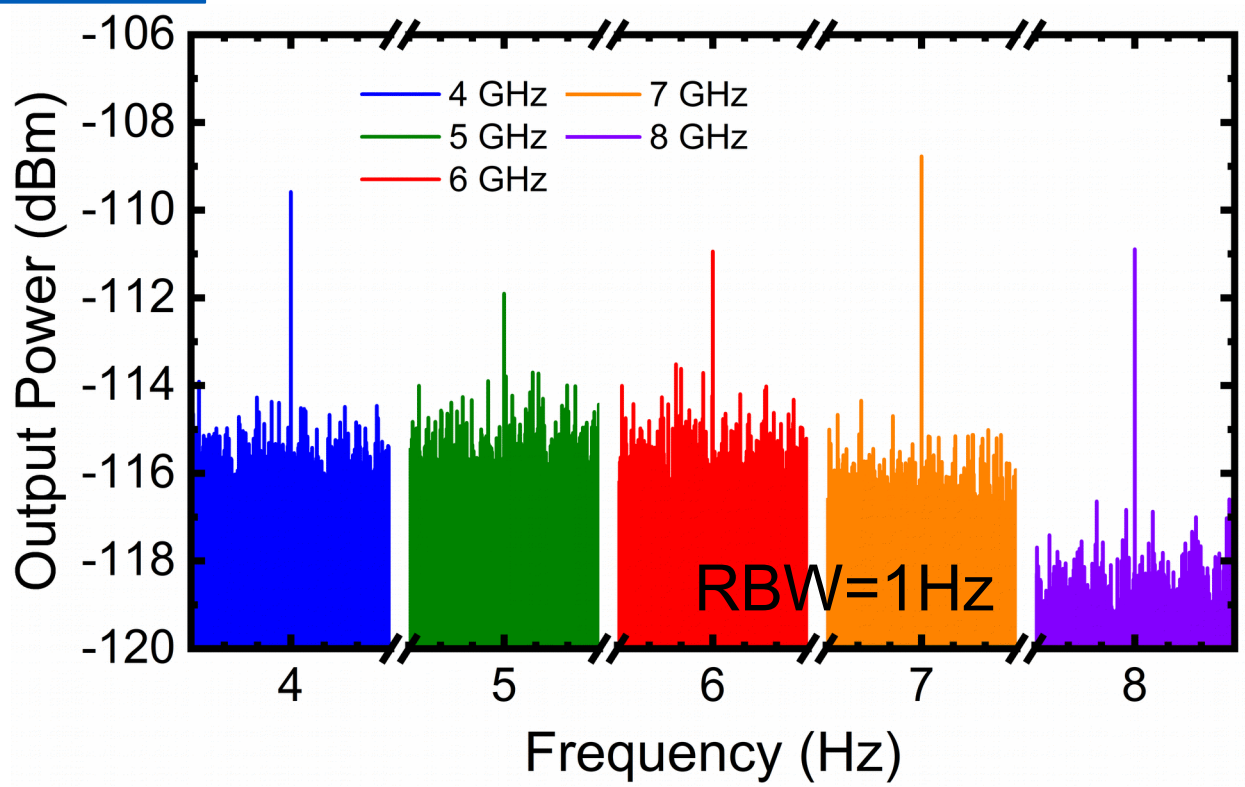
[M. Gong et al. RFIC 2019]





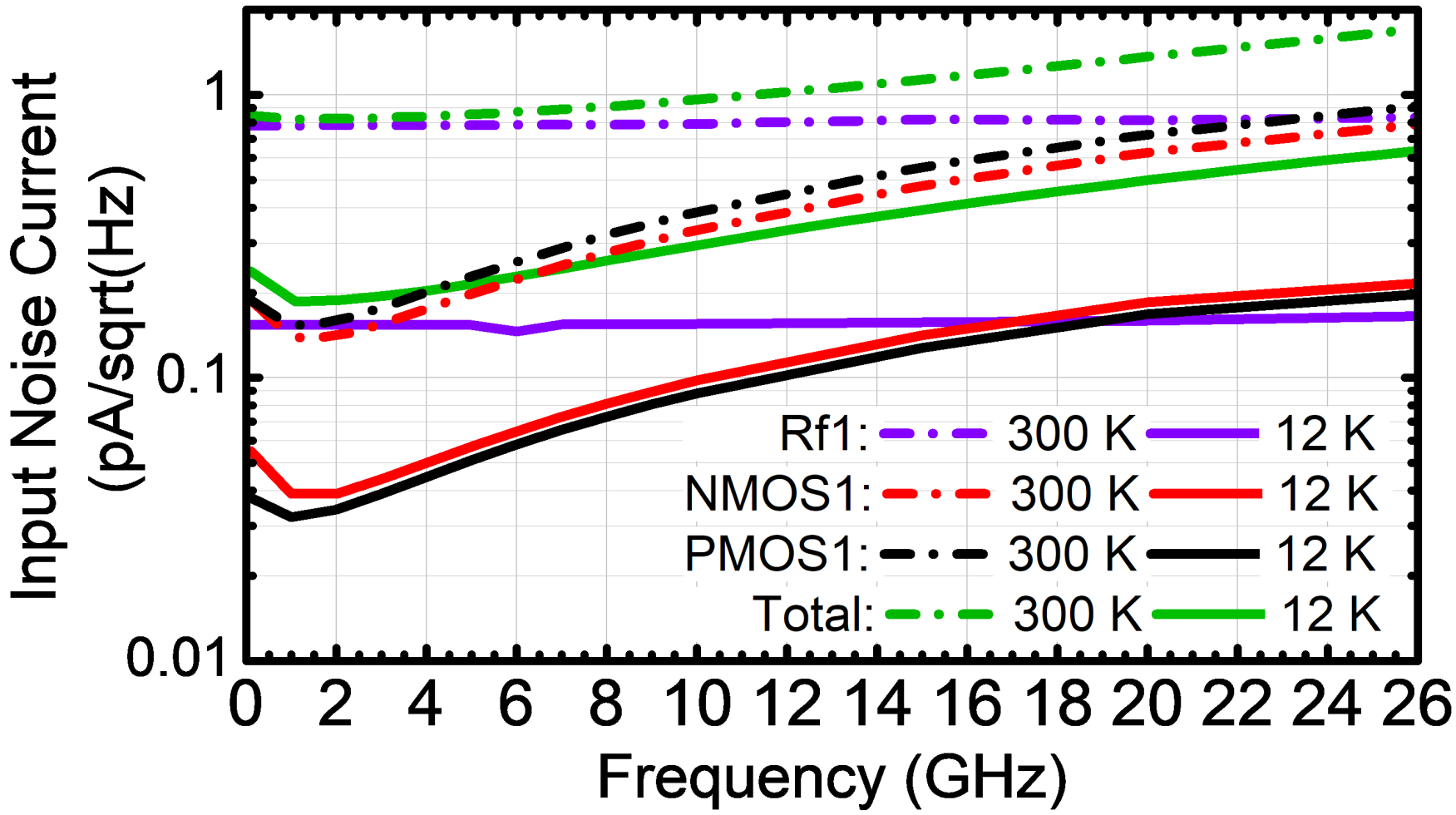
Meas. output spectra of 1x p-DQD+TIA at 300K





- Output spectrum measured with variable-amplitude sinusoidal signals applied to the gate of the DQD.
- At -110dBm output power, the 4GHz sinusoidal signal is clearly visible above the noise floor. Based on the 251 kΩ TIA gain, this corresponds to 3pA$_{rms}$ current at the input of the TIA.

Simulated noise contributions of TIA devices



Optimal TIA MOSFET size for minimum noise depends on temp

Thermal noise 5 times smaller at 12 K

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- **Impact of process variation**
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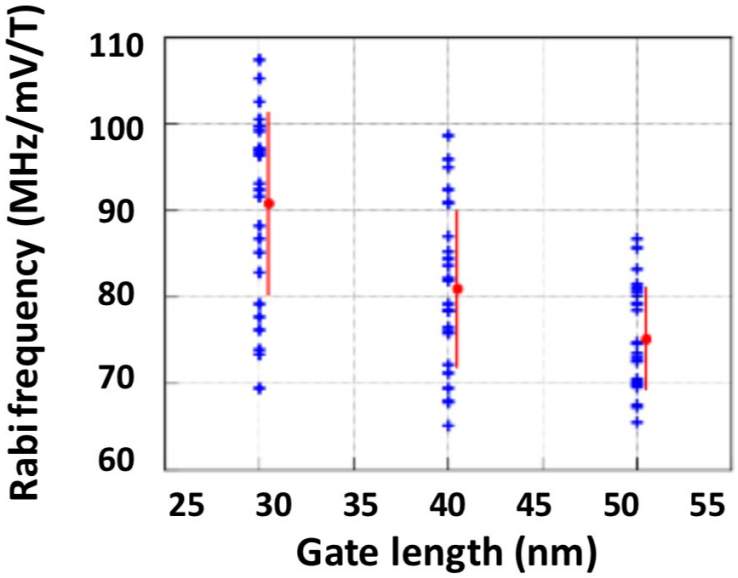
Impact of process variation

- ΔW, ΔL, $\Delta t_{Si(Ge)}$=> E_1-E_0, f_R
- Gate oxide spacer and source/drain-to-channel potential barrier => E_1-E_0
- Surface roughness => E_1-E_0
- DC external magnetic field value (feedback loop) =>E_m, f_{Larmor}
- Δt_{OX}, ΔW, ΔL, $\Delta t_{Si(Ge)}$ => V_T, f_R variation
- g?, f_{Larmor}, f_R

Some of them may be adjustable/corrected from back gate

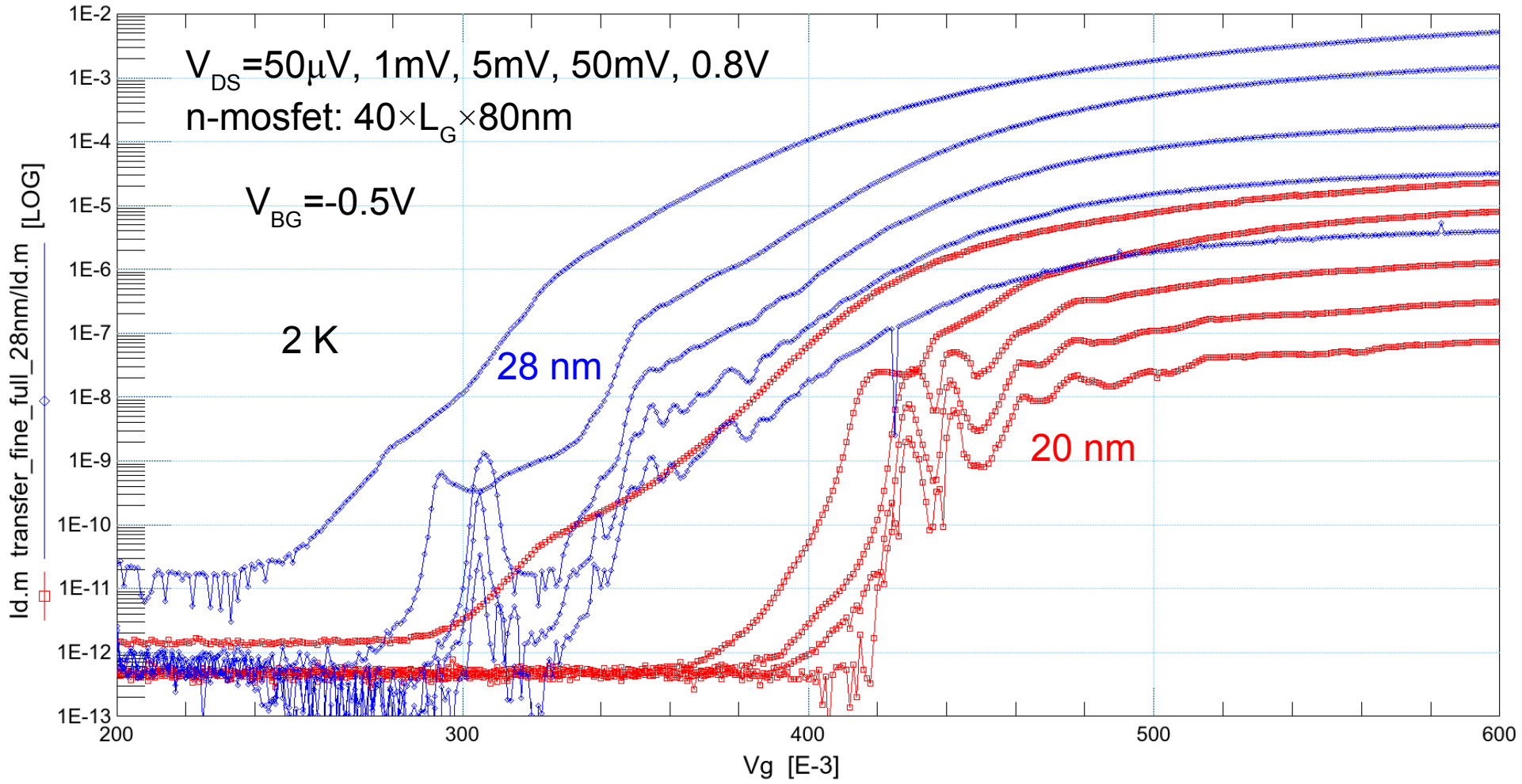
[M. Vinet et al., IEDM 2018]



FDSOI hole-spin qubit]

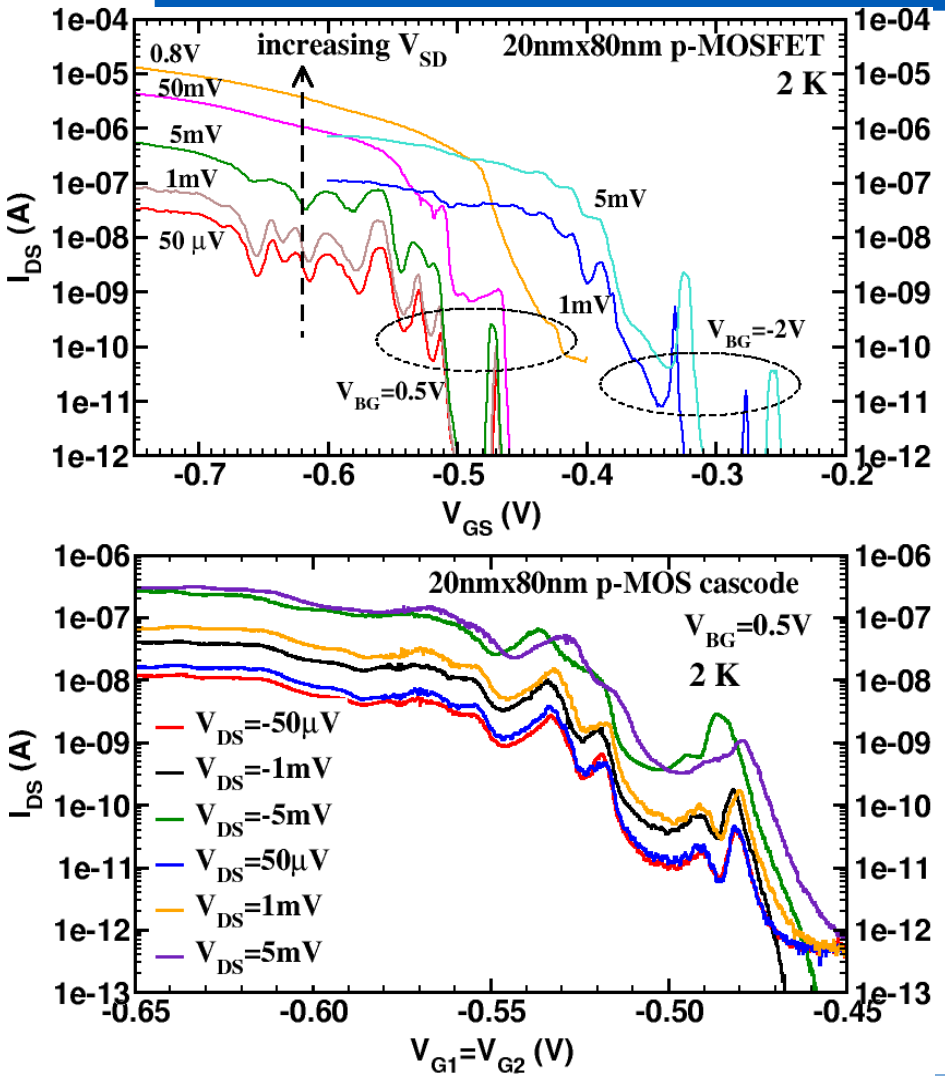
Fig. 3: Rabi frequency in rough hole qubit as a function of gate length. Each cross is a different realization of a Gaussian surface roughness profile with rms = 0.4 nm. The red dot and bar are mean and standard deviation.

Impact of process variation: L_G=20nm vs. 28nm

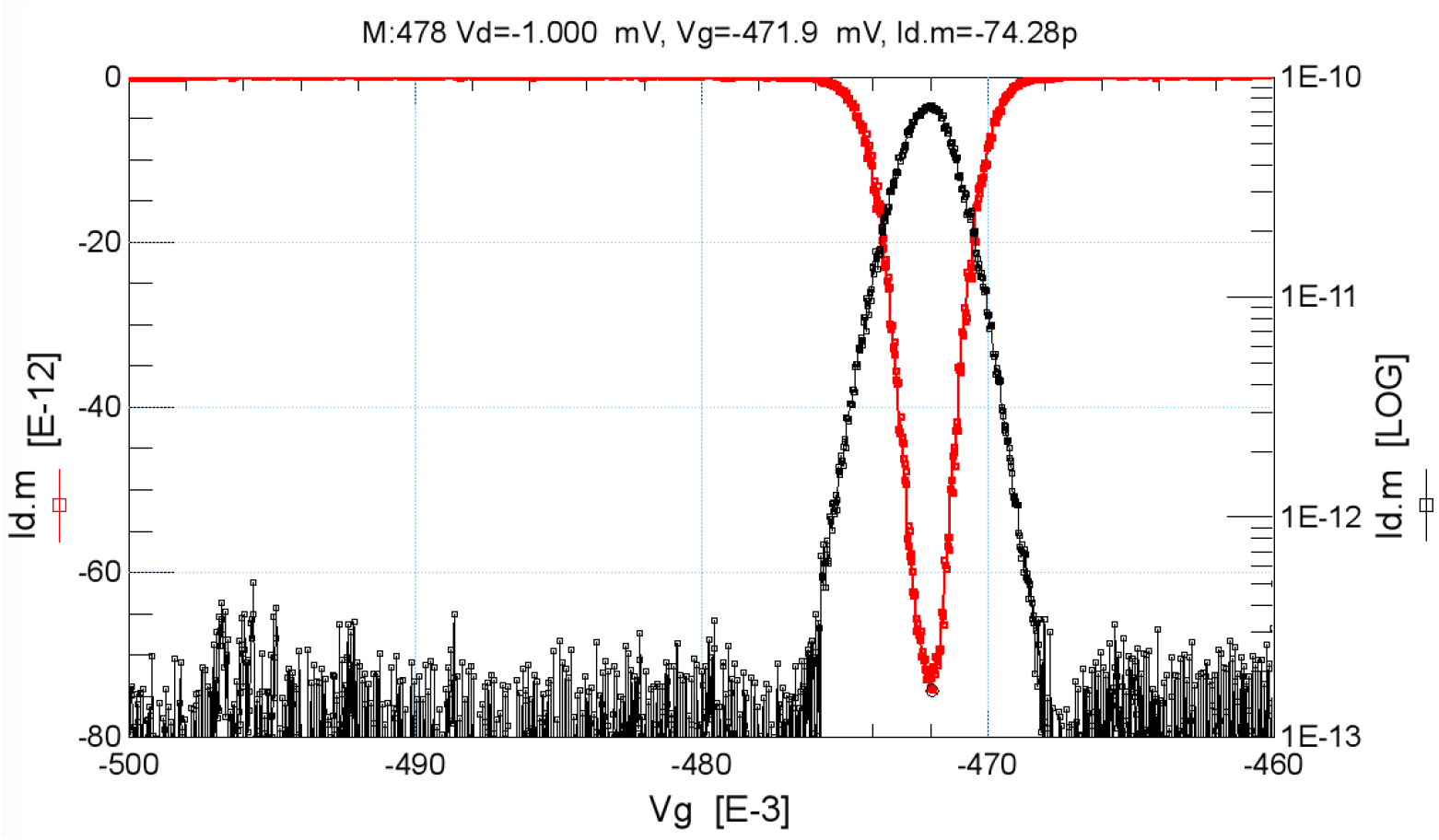


Plot GF_22nmFDSOI_40x20x80_SG_nmos_67G_TS_d19/dc_vbg_n0p5V/transfer_fine_full_die20/transfer

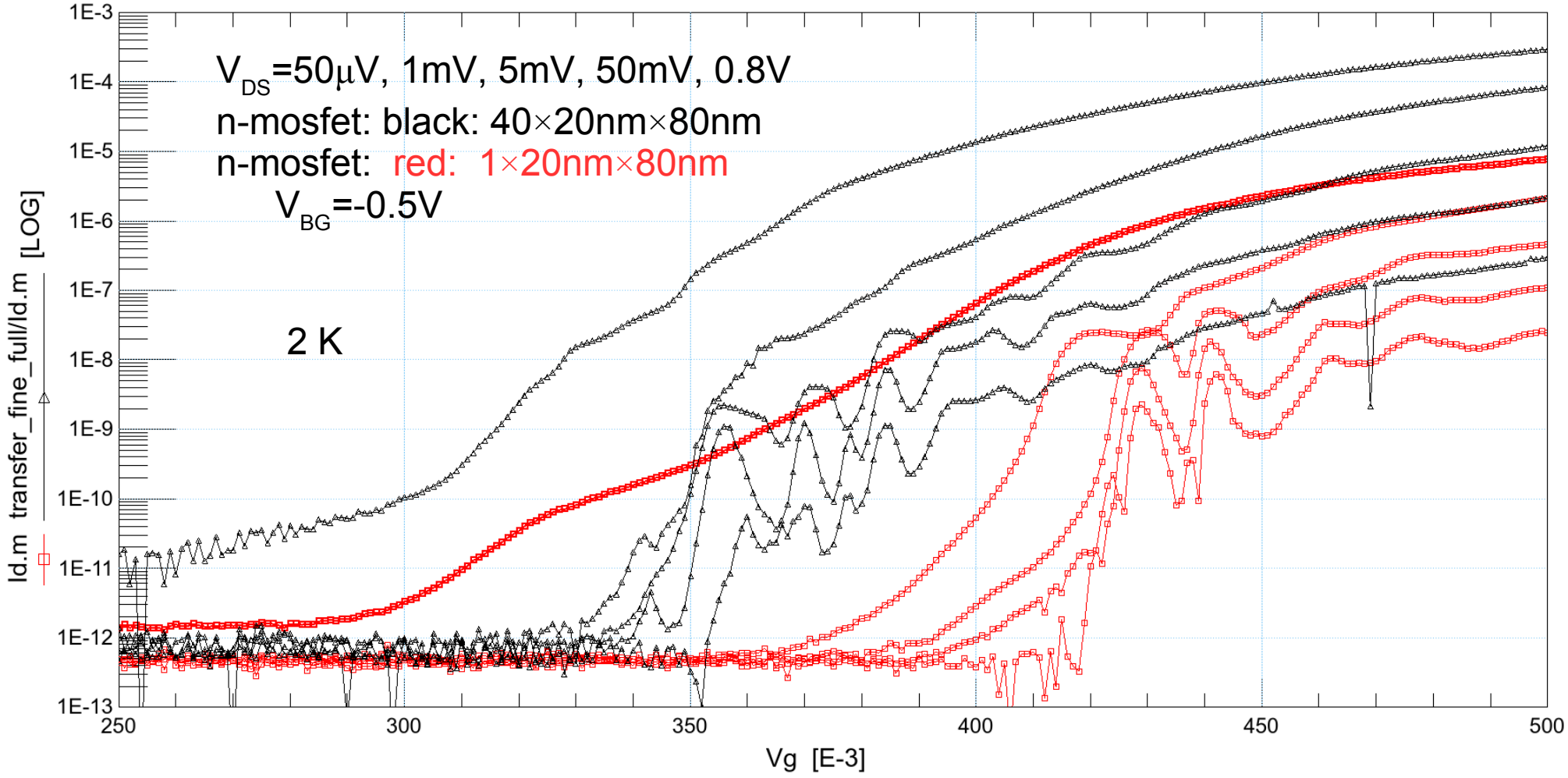
Impact of process variation: 22nm FDSOI



p-MOSFET V_{ds}= -1 mV zoom



Process variation: die to die and different N_f



Plot GF_22nmFDSOI_40x20x80_SG_nmos_67G_TS_d19/dc_vbg_n0p5V/transfer_fine_full_die20/transfer

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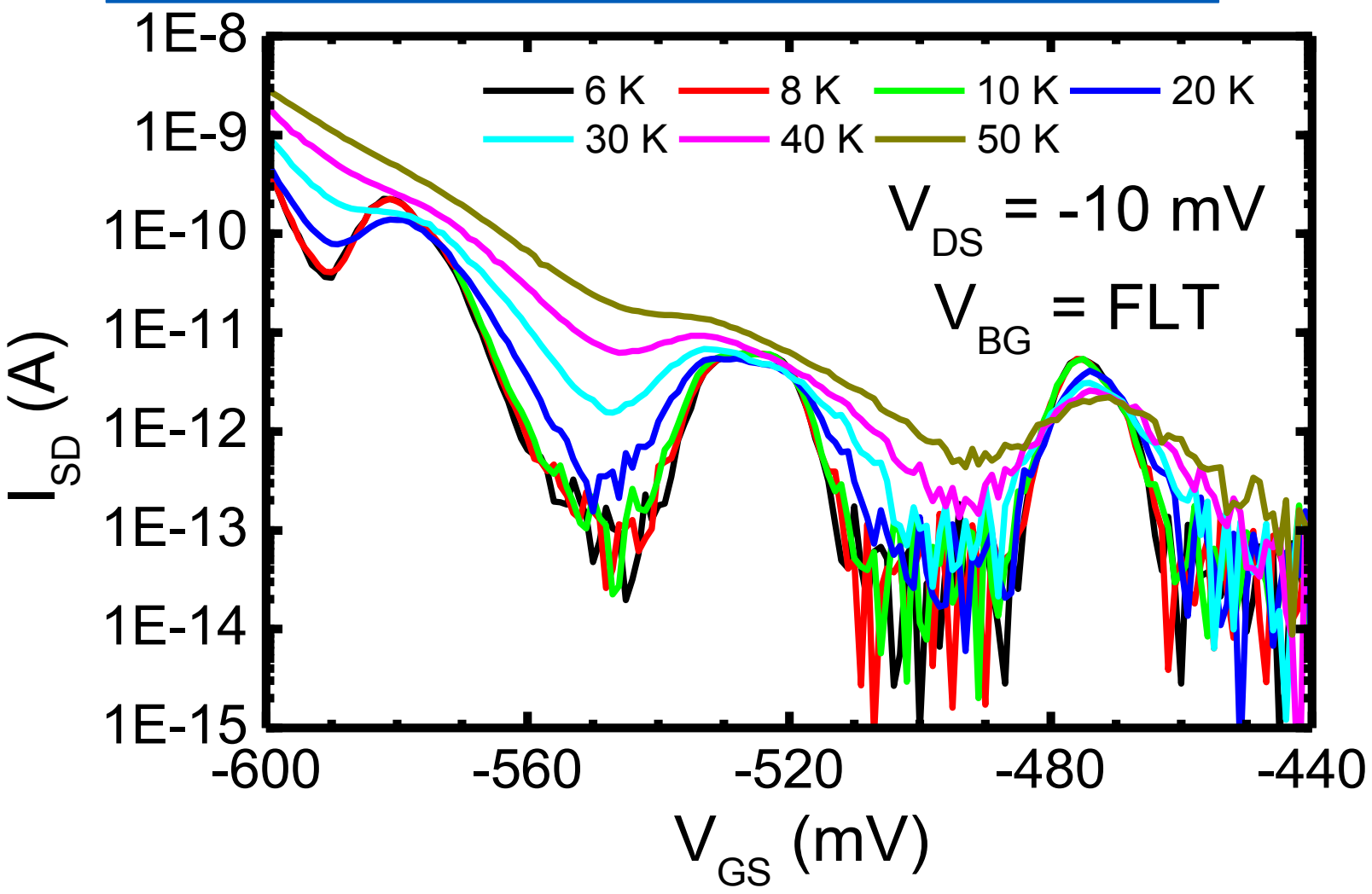
18nmx70nm p-MOSFET vs Temperature



Resonant tunnelling current peaks widen over V_{GS} and decrease in $|I_{DS}|$ height as temperature increases

More thermionic emission overboth barriers of the QD as temperature increases

Qubit operation temperature scaling

- f_L, T increase ~ L^{-2}, W^{-2} (very favourable scaling law)
- f_L, T increase linearly with dc magnetic field B_{dc}
  - B_{dc}=2.9T => ΔE_m=0.33meV, f_L=80.4 GHz, T=4 K, 22-nm FDSOI
  - B_{dc}=8.6T => ΔE_m=1meV, f_L=241.2 GHz, T=12 K, 12-nm feature?
  - B_{dc}=17.3T => ΔE_m=2meV, f_L=582.4 GHz, T=24 K, SiGe BiCMOS?
- Magnetic field and double-dot coupling energy limit T, f_L
  - Higher gyromagnetic factor helps => hole spin in SiGe channel

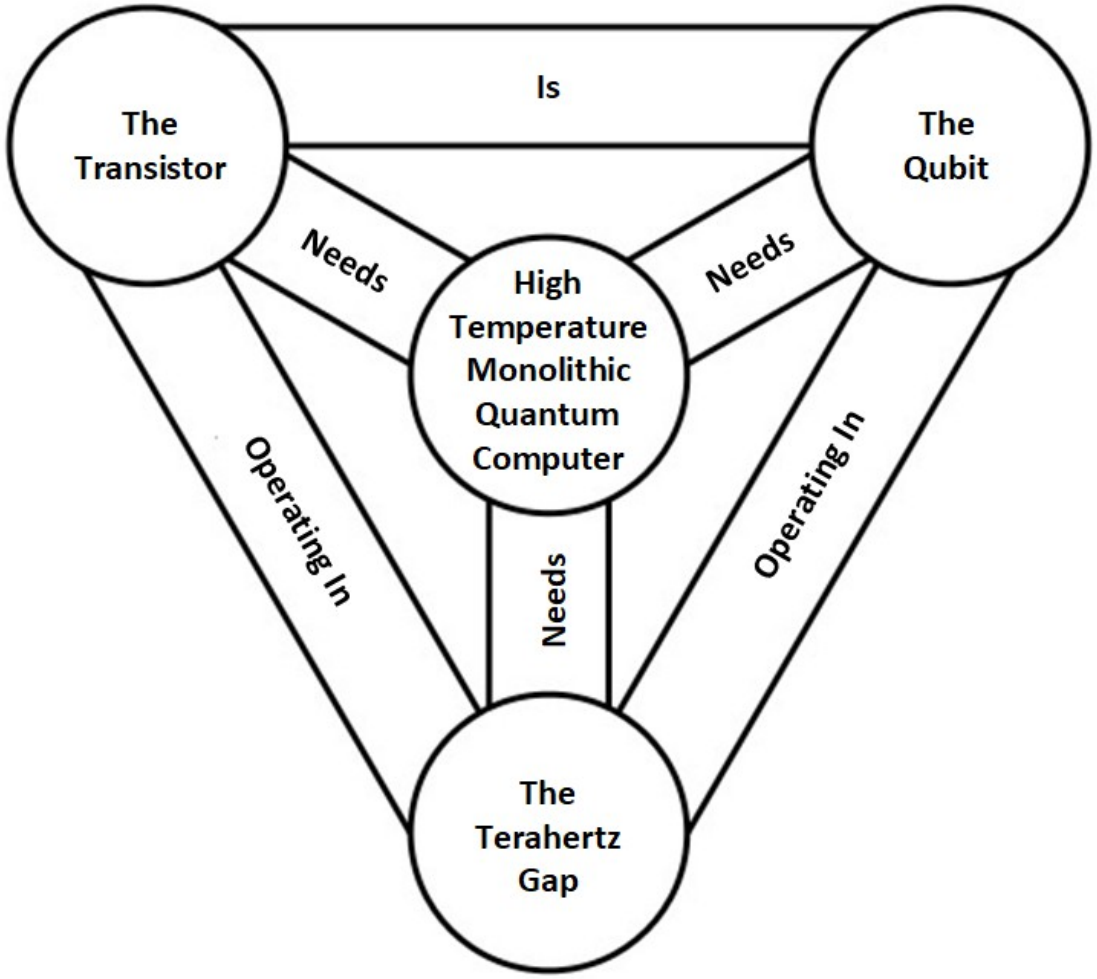
Challenges

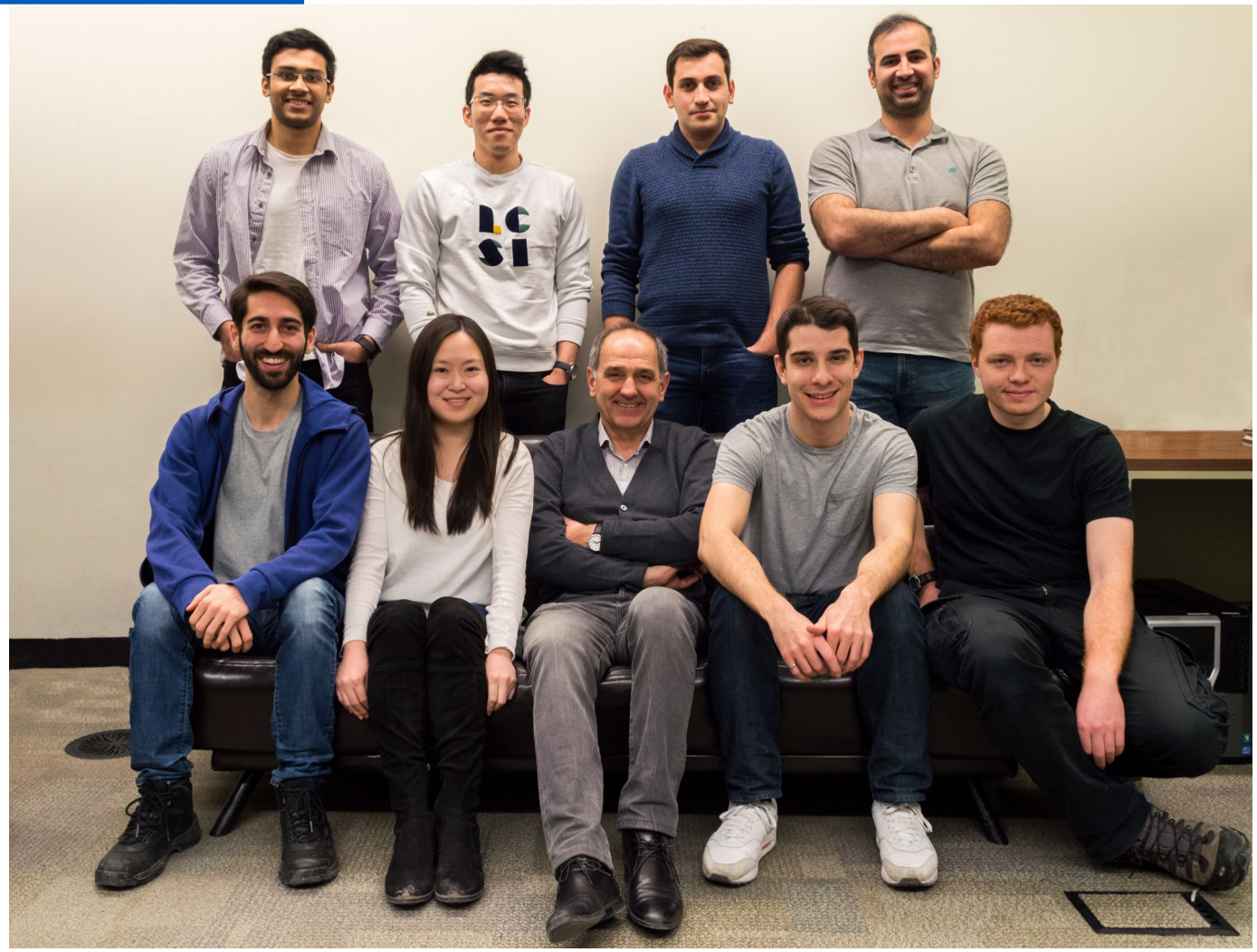
- Qubit fidelity << transistor fidelity => **Tradeoff: T vs. fidelity**
- Spin readout, qubit-to-qubit isolation
- Gyromagnetic-factor engineering for high-temp scaling
- W_f <= 50 nm (limits operation temperature today)
- CNOT Gate (or other 2 qubit logic gate)
  - (Minor) process/mask changes still needed
- Entanglement across multiple qubits

Conclusions

- **Monolithic integration** of CMOS spin control/readout circuits and qubits
- **SiGe hole-spin qubit** in p-MOSFET channel
- **> 60GHz** spin-manipulation/readout low-noise, AMS circuits needed
- At 2-4 K, minimum-size 22nm FDSOI MOSFET can be used as qubit in the subthreshold and as “classical” transistor in saturation
- 100-qubit processor < 2 W, probable now at 2-4 K in 22-nm FDSOI
- Future scaling to 10nm qubit gate length and 15nm width => 77 K operation?

In a nut shell: The Trinity





Acknowledgments

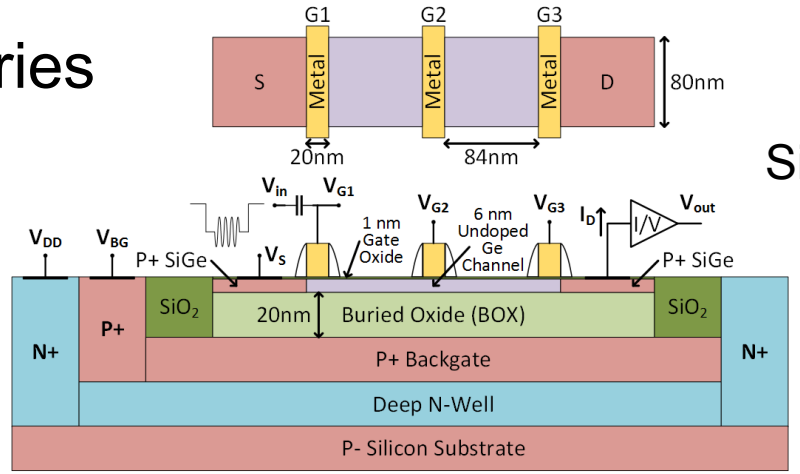
- Prof. P. Asbeck, UC San Diego
- Dr. A. Muller, Dr. M. Iordanescu, Dr. G. Adam, Dr. D. Daughton, N. Messaoudi Prof. R. Mansour, Dr. D. Harame, Dr. Nigel Cave
- NSERC for funding
- GlobalFoundries for technology access and chip donations
- IMT Bucharest, Lakeshore, Keysight, and U Waterloo for cryo measurements
- Integrand for EMX software
- CMC and Jaro Pristupa for CAD tools and support

Multi site measurements

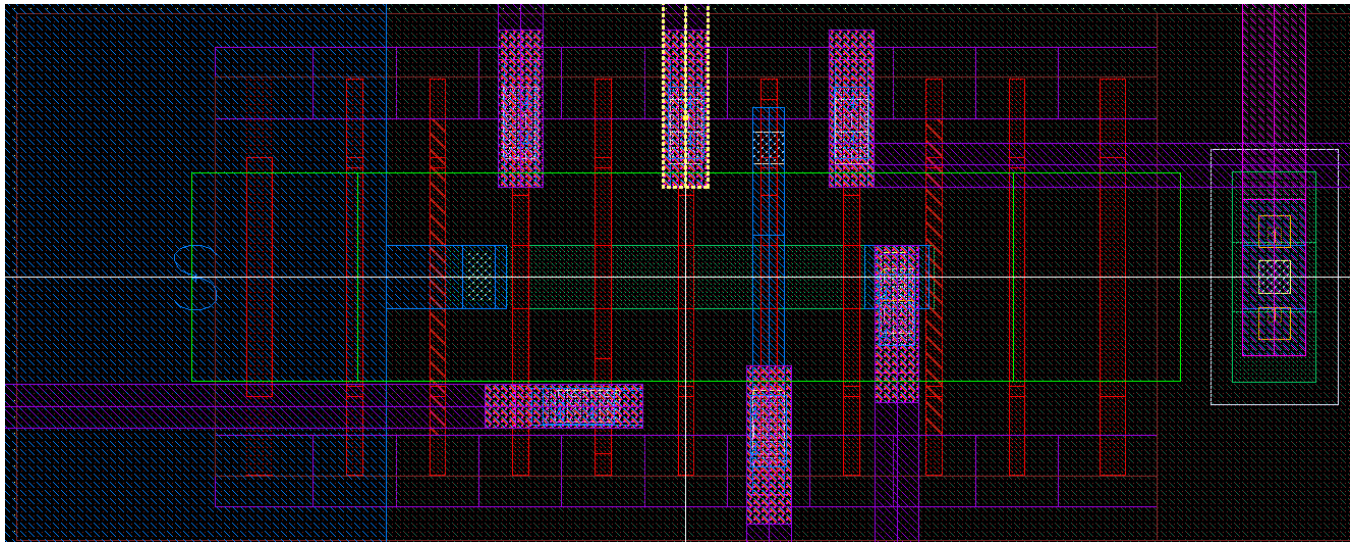
- IMT Bucharest: November 2017 to present
  - Custom-built cryostat DC-67 GHz, 6 K – 300 K
  - DC and non-calibrated GSG 2-port S-params w/o B-field: TIA, transistors, quantum dots, passives
- University of Waterloo, Ontario, Canada: March 2018
  - Lakeshore CPX 3.3 K commercial system
  - DC and calibrated GSG 2-port S-params: Transistors, passives
- Lake Shore Cryotronics, Westerville, Ohio, USA: June 2018)
  - Lakeshore CPX 2K commercial system
  - DC and calibrated GSG 2-port S-params: Single and double QDs, TIA

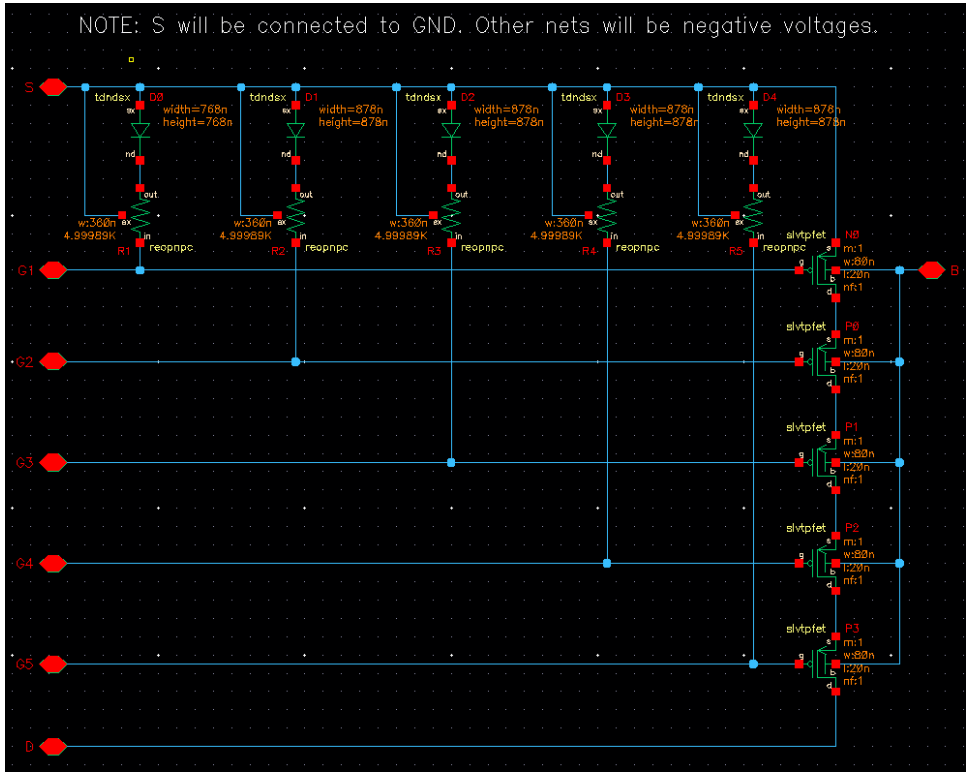
3 and 5 coupled QD hole-spin qubits

3 series QDs



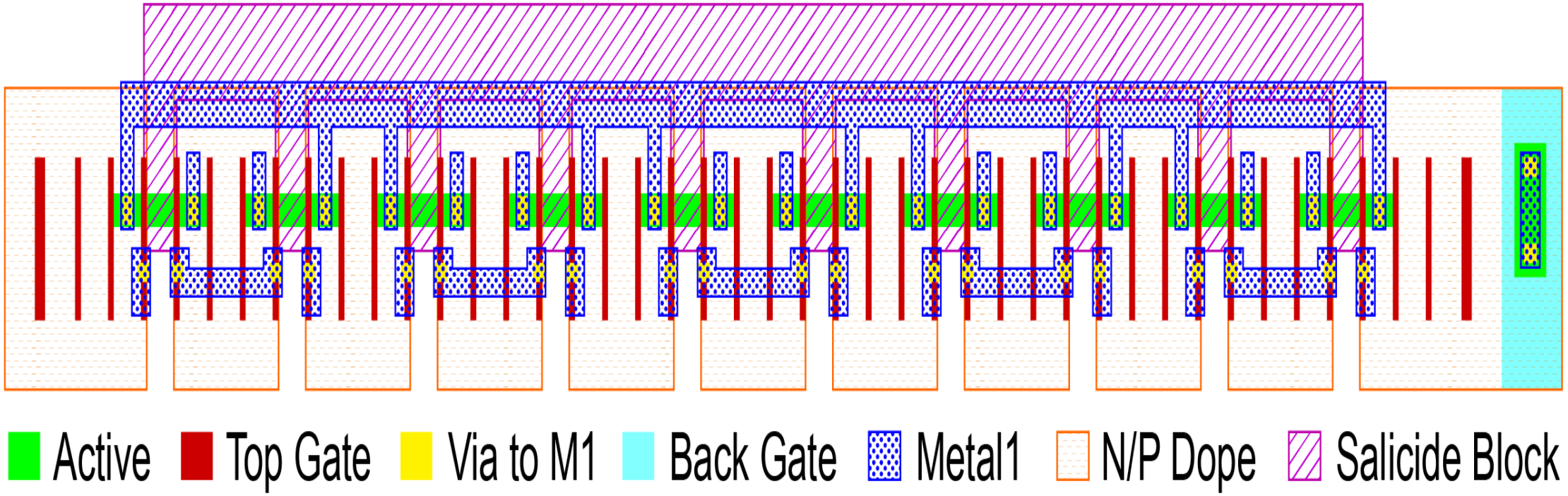
$Si_{0.7}Ge_{0.3}/Si_{0.75}Ge_{0.25}$





5 gates = 5 serially coupled qubits
Analogy with charge coupled devices and series stacked cascodes

10 coupled double QD qubits in parallel

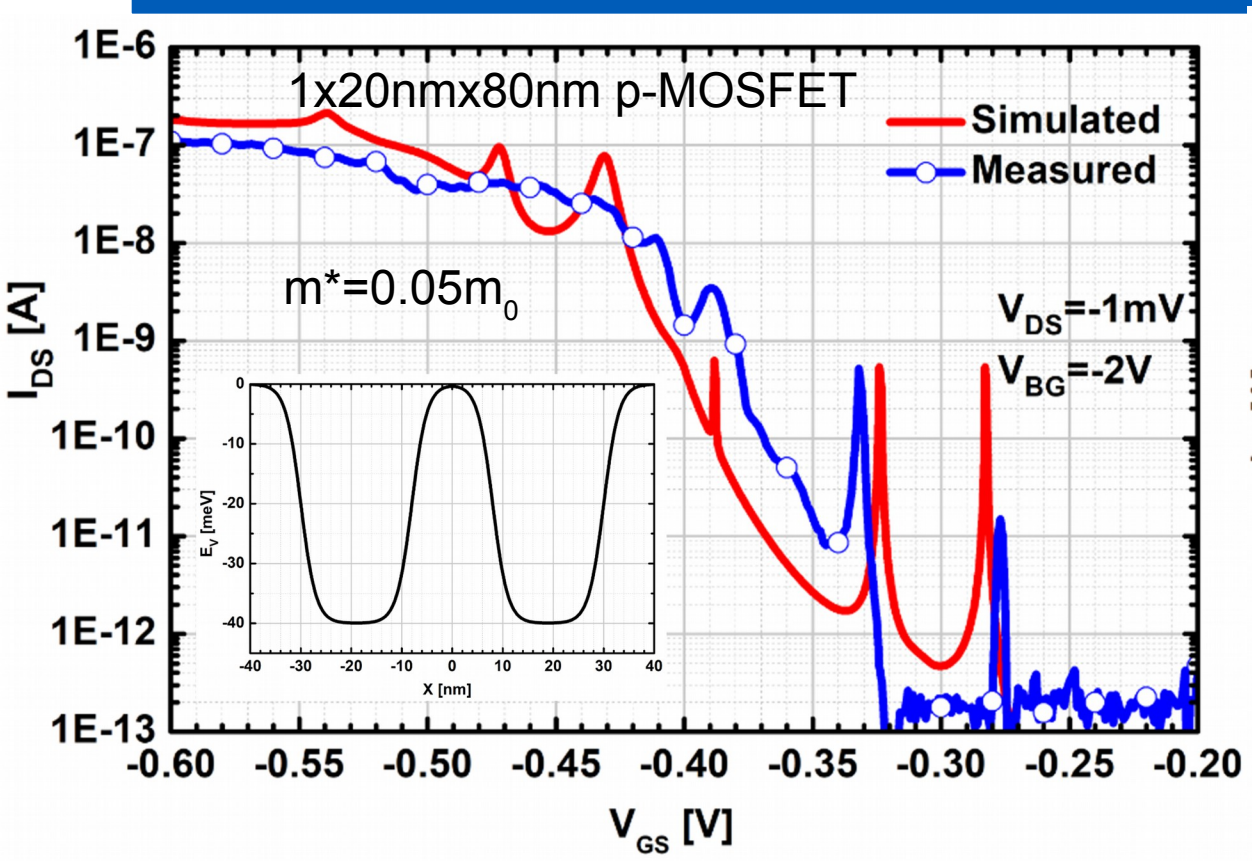


Improves matching

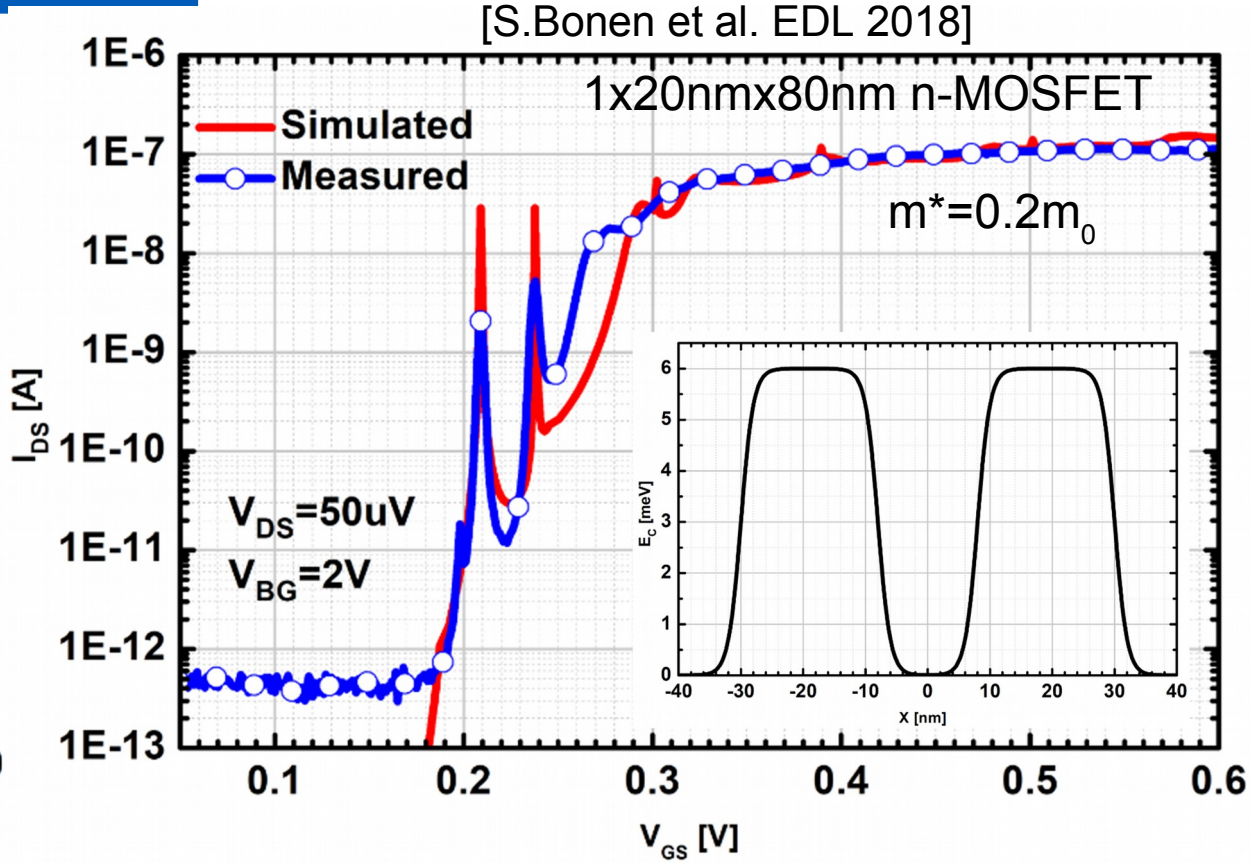
Qubits spins manipulated in parallel => 10 electron/hole spins majority gate

Equivalent to redundant qubits for measurement readout error correction?

Quantum effects stronger in p-MOSFET



[S.Bonen et al. EDL 2018]

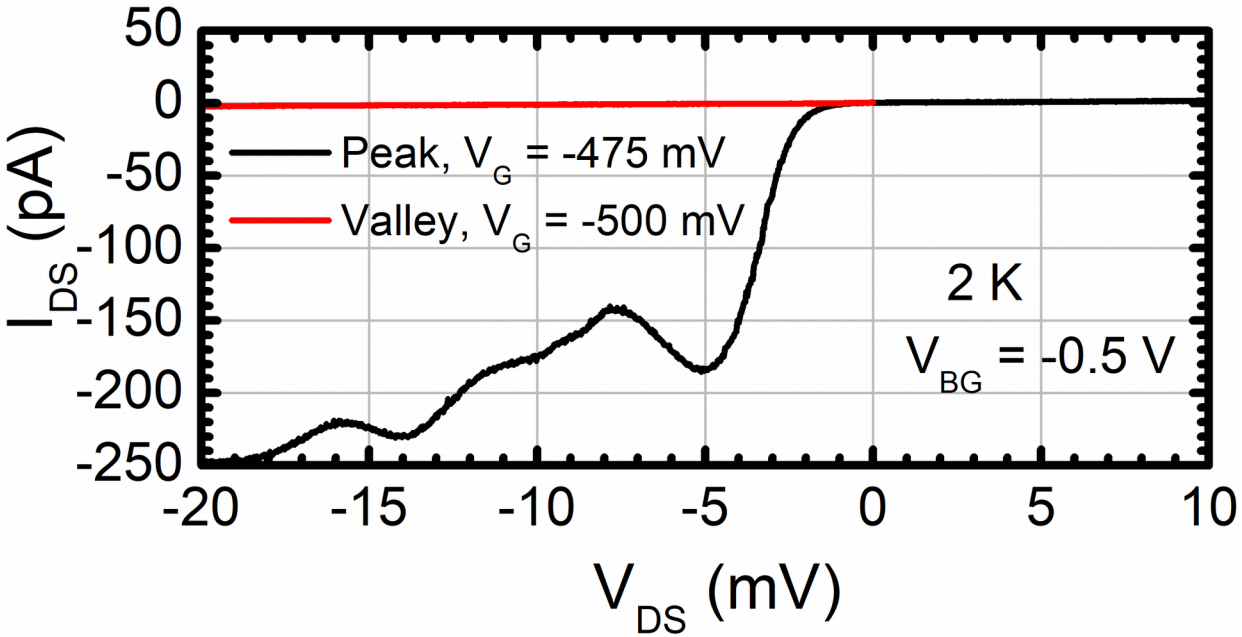


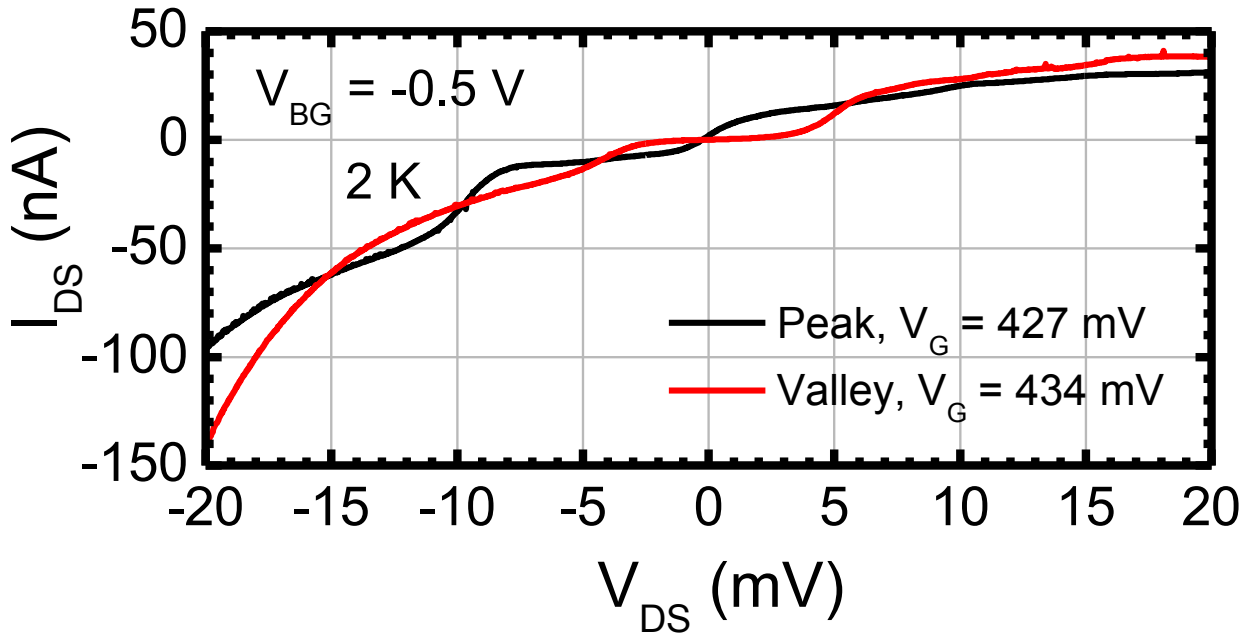
$Si_{0.7}Ge_{0.3}/Si_{0.75}Ge_{0.25}$ S/D-channel heterojunction provides better confinement barrier.

ΔV_{GS} (hence ω_R) doubles in p-MOSFET compared to n-MOSFET

Coulomb Blockade in Output Characteristics

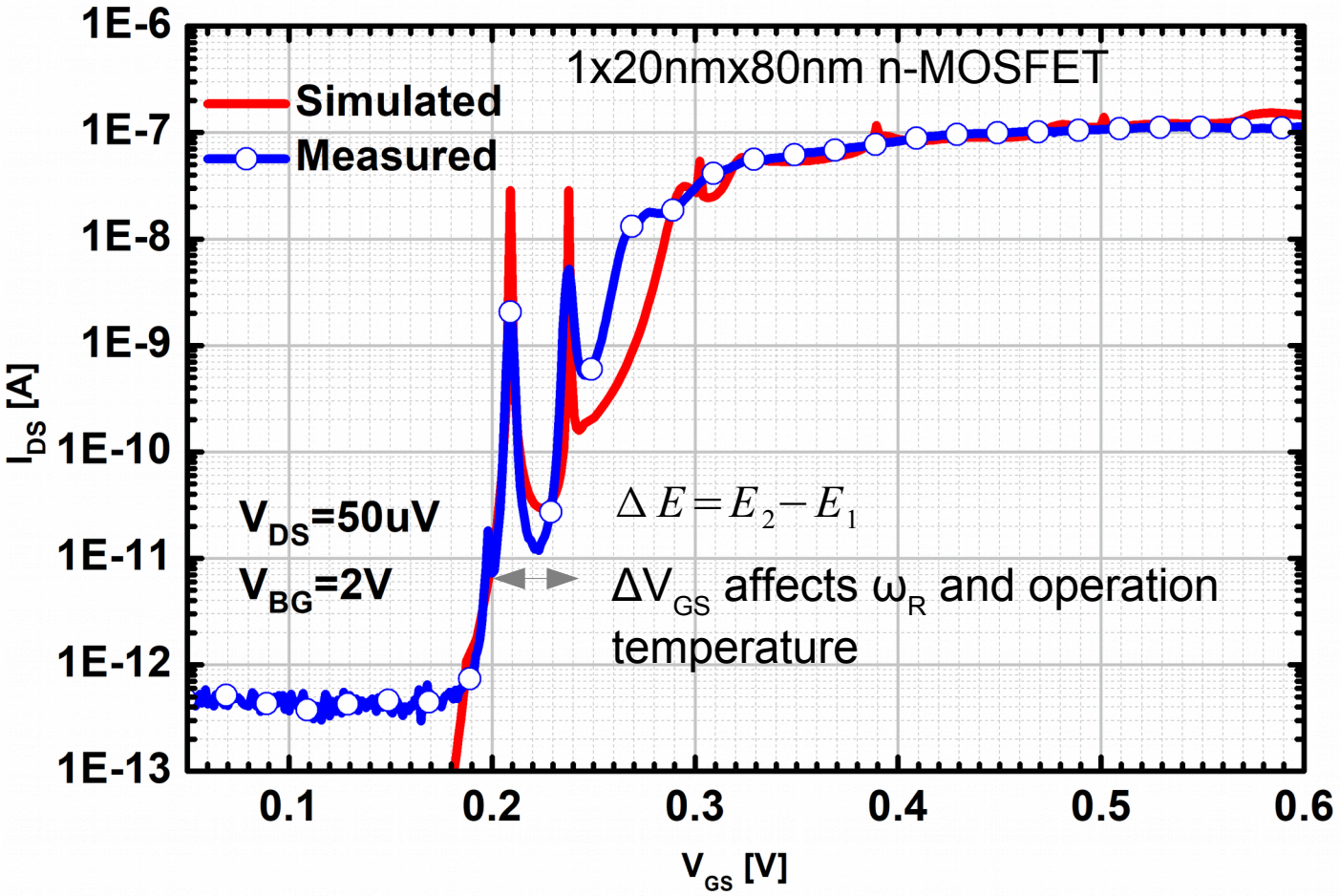
1x20nmx80nm p-MOSFET [M. Gong et al. RFIC 2019] 1x20nmx80nm n-MOSFET

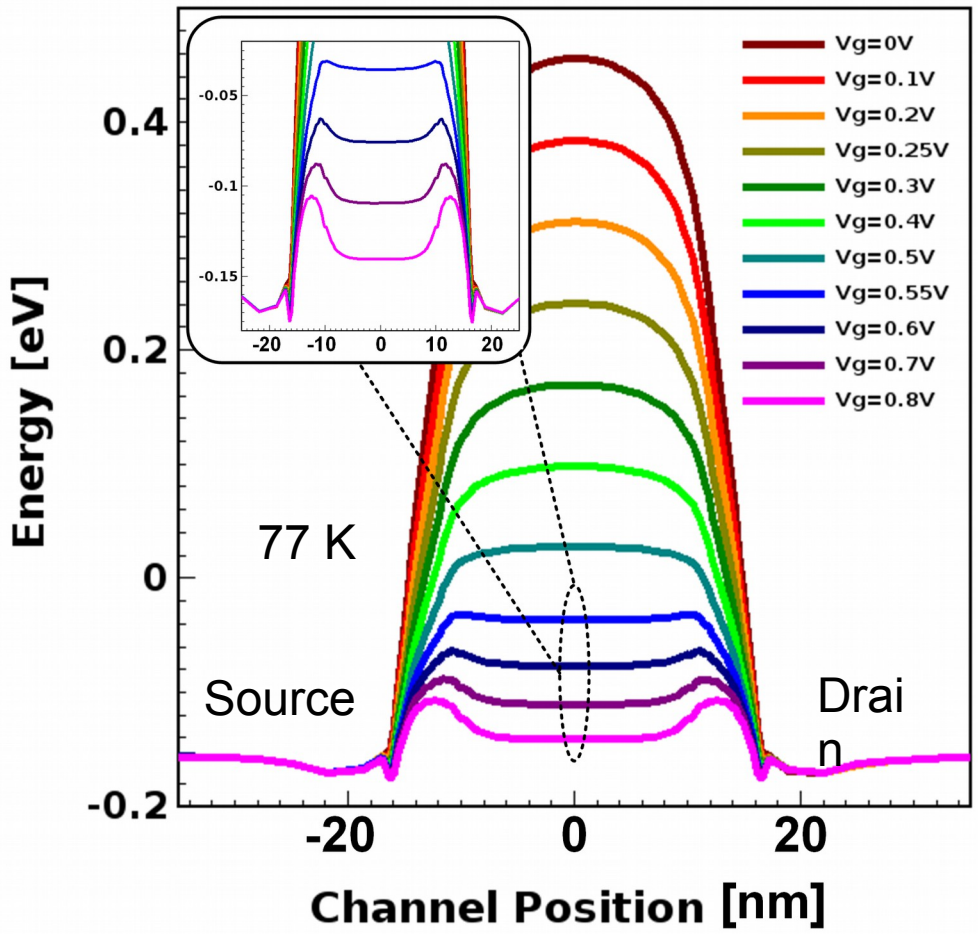




- Present in both devices; shows single electron/hole charging events
- Asymmetry in p-MOSFET due to heterojunction
- Hole gyromagnetic factor in $Si_{1-x}Ge_x$ between 2-20 => smaller magnetic field needed for given operation temperature

Modelling Resonant Tunnelling in n-MOSFET at 2 K

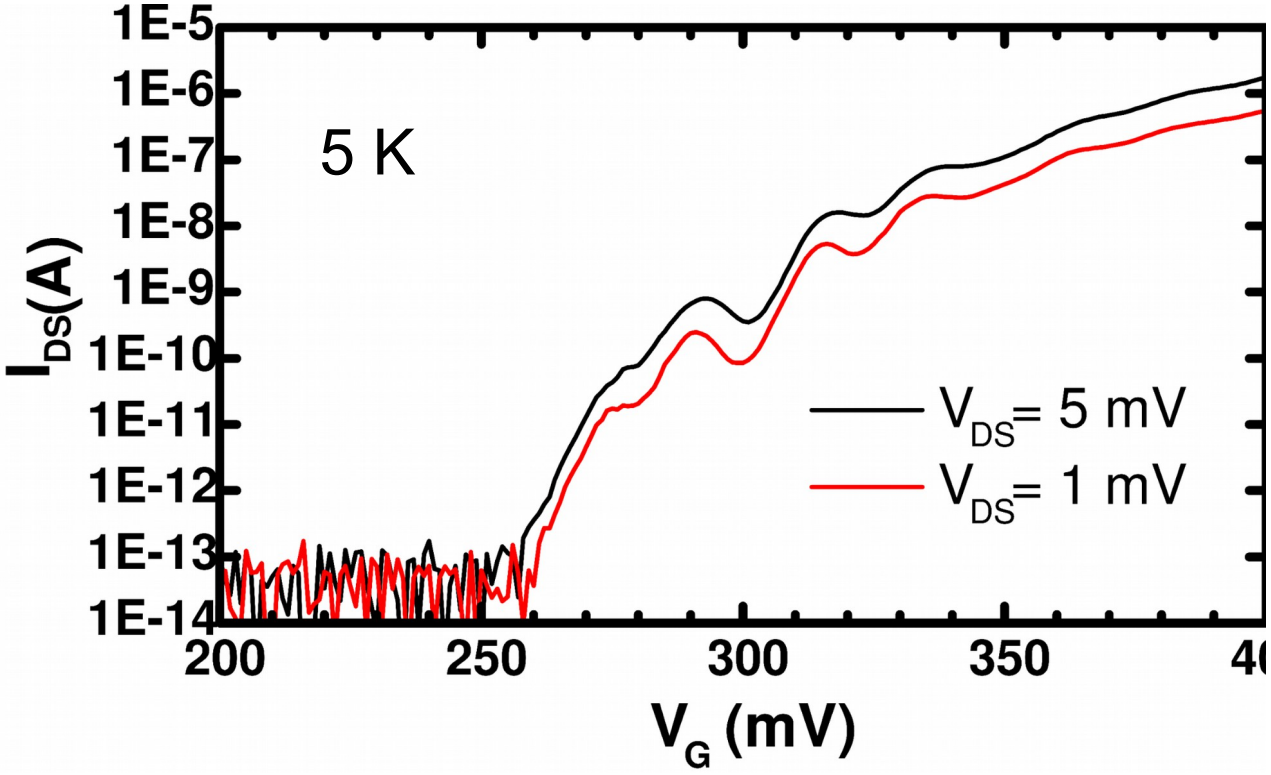




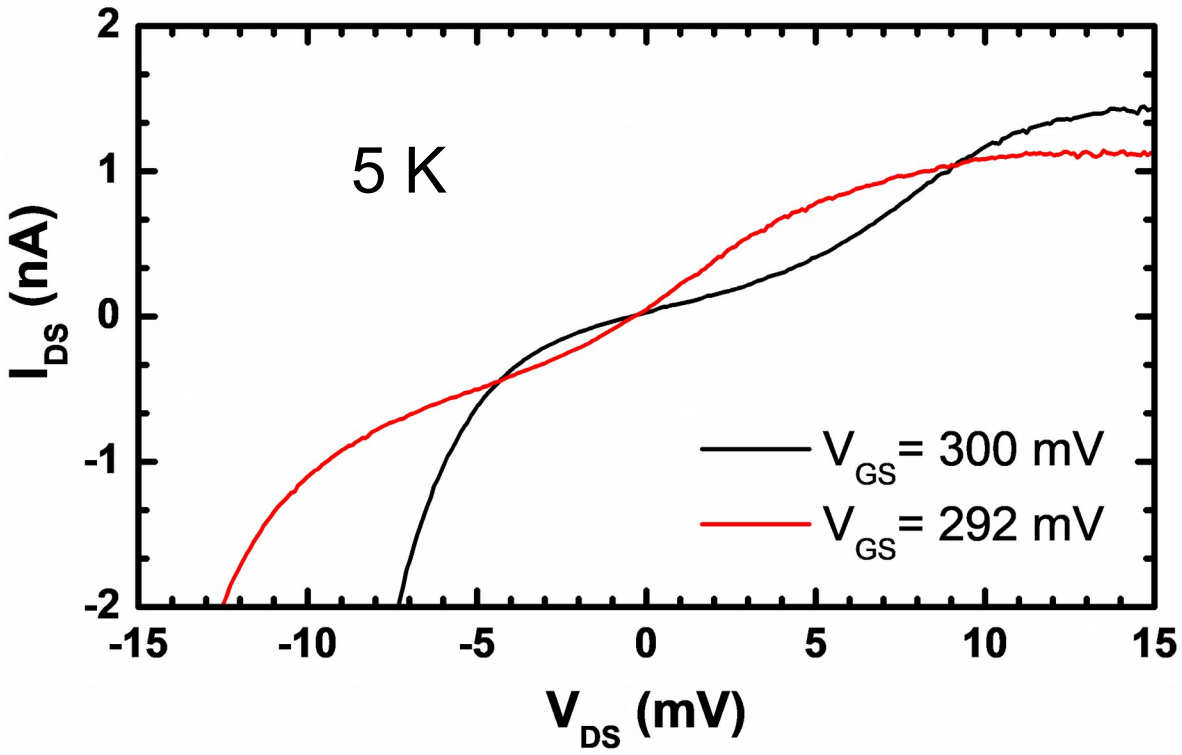
NEGF modelling code by Prof. Peter Asbeck

[S.Bonen et al. EDL 2018]

Quantum effects in 40x18nmx70nm n-MOSFET

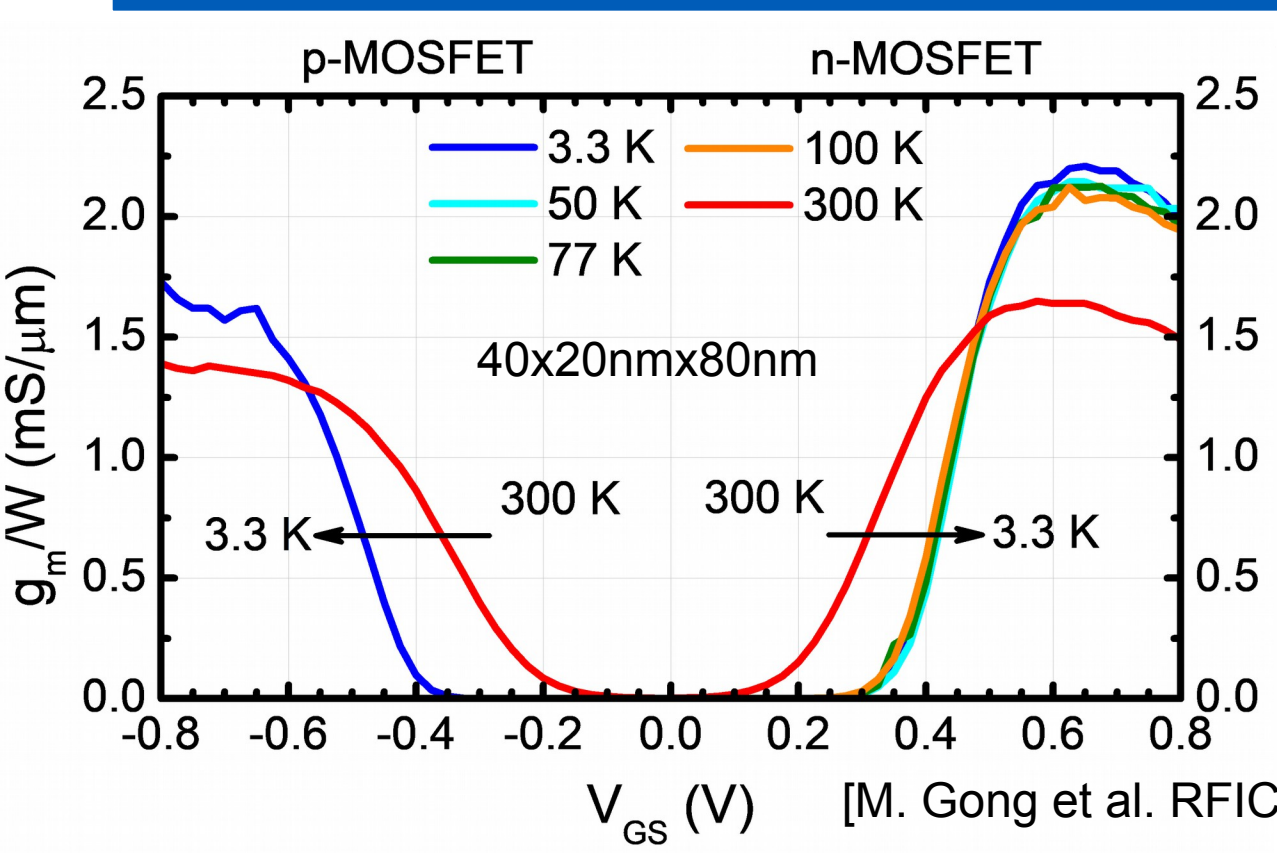


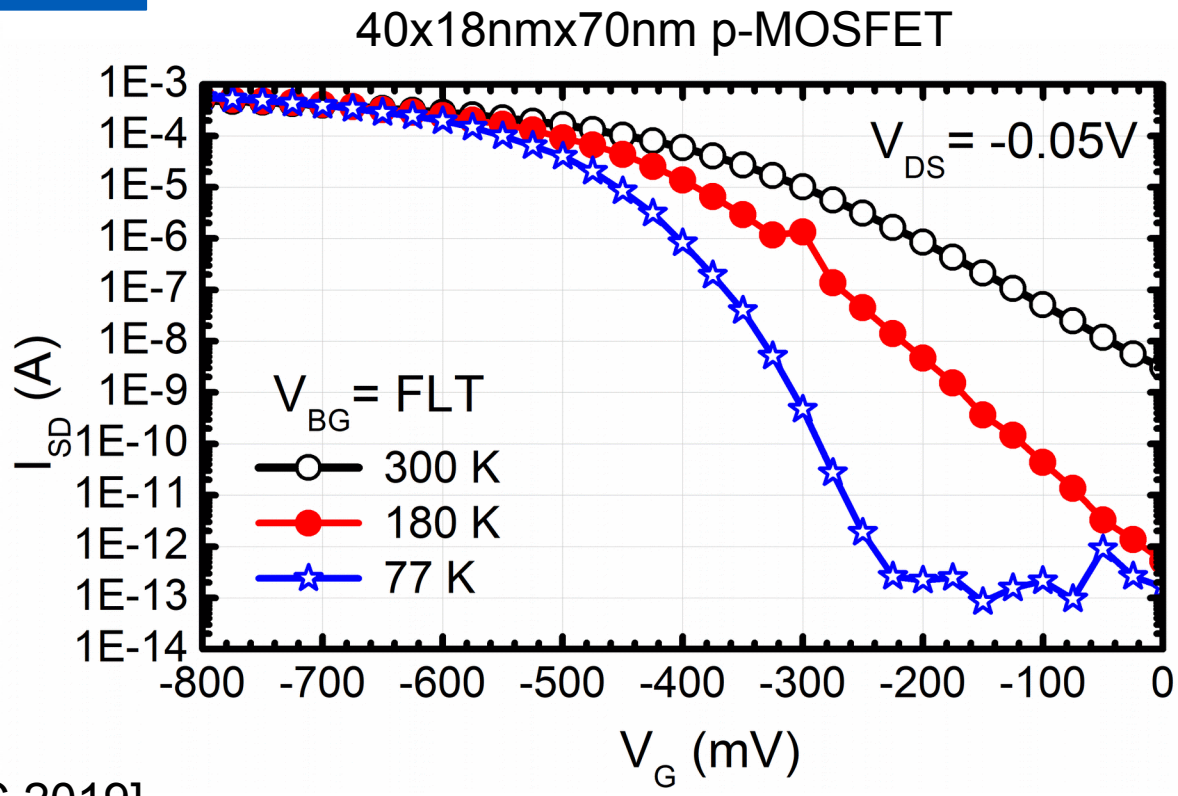
Transfer characteristics



Output characteristics at first peak and valley

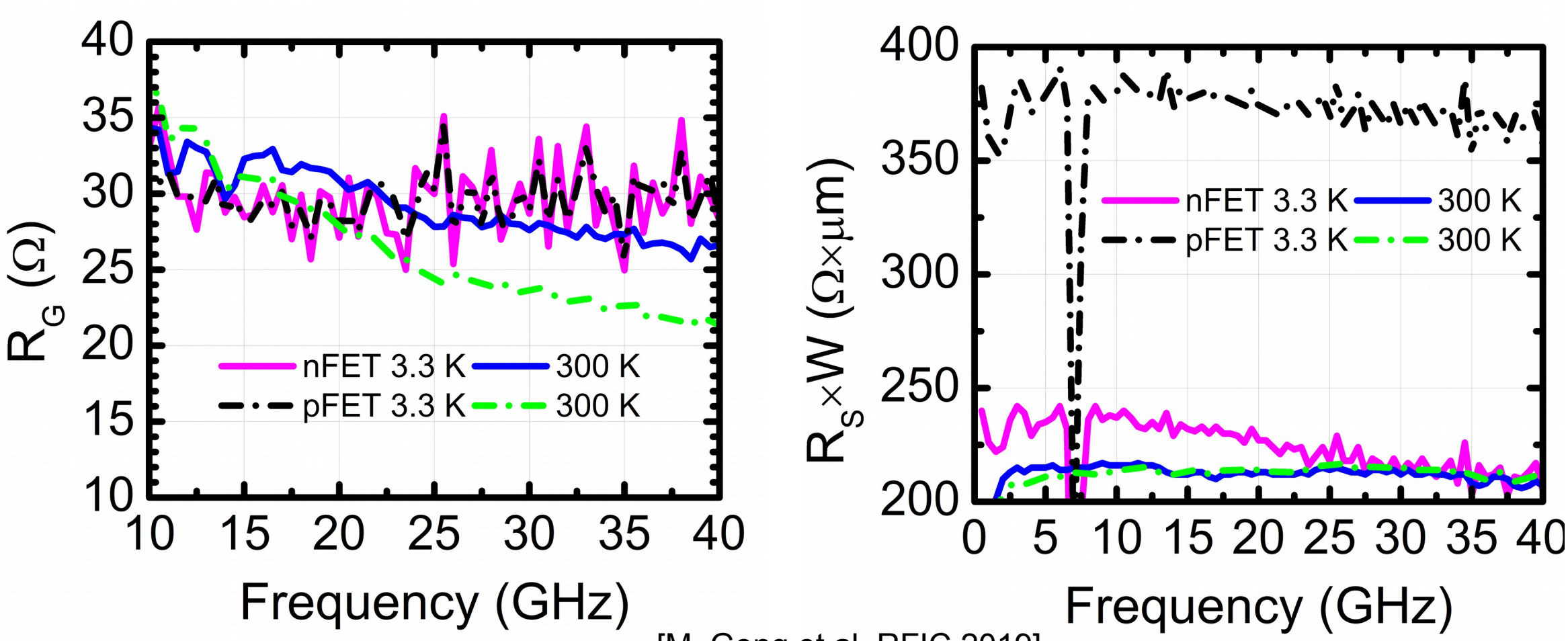
MOSFET variation over temperature





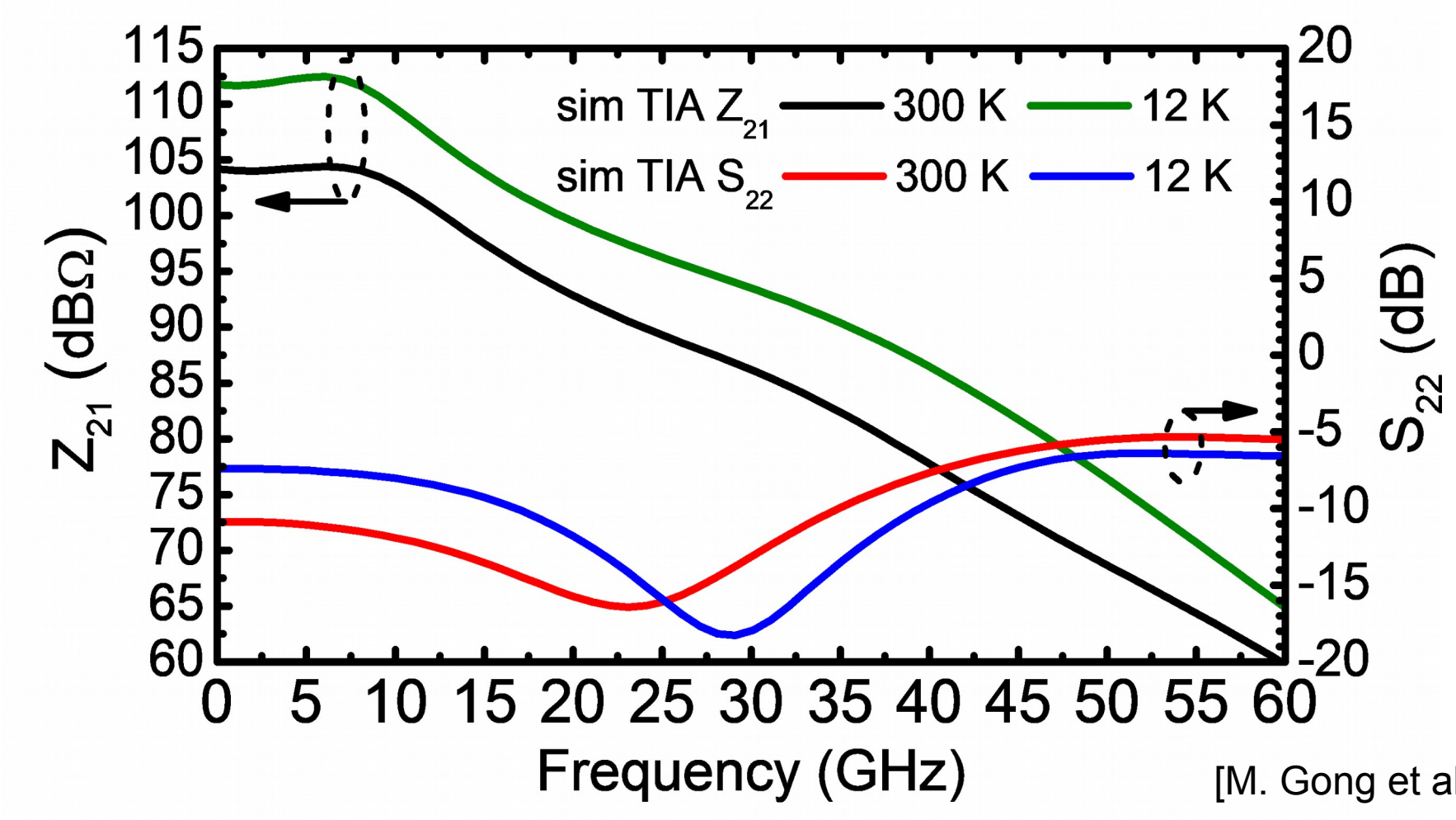
Most threshold voltage and transconductance variation with temperature occurs between 300 K and 77 K with little change afterwards

Gate Resistance and Source Resistance



[M. Gong et al. RFIC 2019]

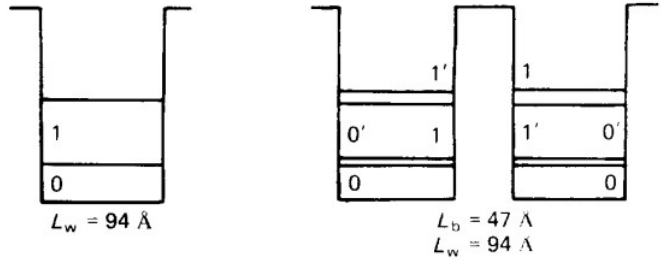
Simulated TIA performance over temperature



[M. Gong et al. RFIC 2019]

E-level splitting due to coupling between QDs

AlGaAs/GaAs/AlGaAs double well



Coupling frequency $f_C = \frac{2\Delta E}{2\pi\hbar}$; $2\Delta E = 1\text{meV} \rightarrow 241.47\,GHz$

ΔE (or t or J) = coupling energy

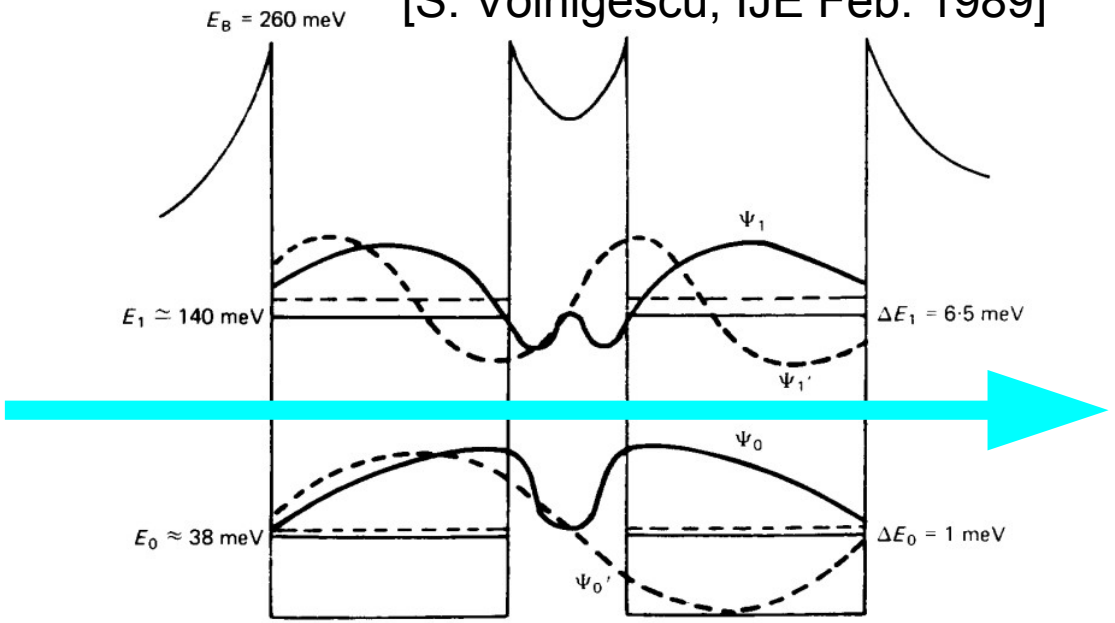
ΔE must be > kT

Want electric control of ΔE (barrier) for Swap or C-NOT gate

$$E_{0+} = E_0 + \Delta E$$

$$E_{0-} = E_0 - \Delta E$$

[S. Voinigescu, IJE Feb. 1989]



gure 6. Subbands and wave functions in an idealized quadruple heterojunction structure with quantum channel coupling.

QD coupling energy splitting, *T* with scaling