CE Cables

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CE cables routing

- We have to route the cables for the lower APA through the tubes of the APA frame
  - 10 “signal” bundles on each side tube (one cable per FEMB)
  - 10 low voltage power bundles on each side tube (one cable per FEMB)
  - 8 bias voltage cables on one side tube (SHV board only at one end of the APA)
- ProtoDUNE cables
  - “signal bundle”: 12 low-skew shielded twin-axial cables with custom designed connector (PCB on the cable side)
  - low voltage power bundle: 9 AWG20 twisted pair cables with SAMTEC IPL1 connector
  - bias voltage cables: RG-316 coaxial cables with SHV connector

The problem

- The frame size was increased to 4” x 4” to make sure that the cables for the lower APA would fit
  - Added conduit with 2.5” diameter, CE bundle runs inside the conduit
  - Made the assumption that we could decrease the number of connections
- Tests done with 9 “ProtoDUNE signal bundles” and 9 “ProtoDUNE low voltage power bundles”
  - 9 “ProtoDUNE signal bundles” = 108 low skew twin-axial cables
  - 9 “ProtoDUNE low voltage power bundles” = 81 AWG20 twisted pair cables
- Assumption was made we could reduce the number of connections
  - 10 “signal” connections per FEMB (10*10=100 < 108)
  - 8 “low voltage power” connections per FEMB (8*10=80 < 81)
- Except for the connectors (that are anyhow staggered) the tests done so far would be meaningful if we the DUNE FEMBs work with these connections

Does it work (signal)?

- Can the WIB communicate with the FEMB with only 10 connections (12 in ProtoDUNE) ? Yes
  - four connections for readout at 1.28 Gbps (two connection for each COLDATA chip)
  - two 64 MHz clock lines (one for each COLDATA chip)
  - one fast command line (shared between two COLDATA chips)
  - three I2C-like control lines (clock, data-in, data-out, arrive at one COLDATA chip, that then shared the I2C information with the second COLDATA chip)
- This requires that the fast command line (~2 MHz signal) is shared (i.e. single line connected to both ASICs) between the two COLDATA chips
  - to be demonstrated with tests when we build the first FEMBs (late Summer 2019)

If it doesn’t work (signal)

- Alternatives
  - transmit data at 2.56 Gbps (reduce number of data transmission lines from 4 to 2)
  - daisy chain I2C connection between different FEMBs (requires inter-FEMB connections)
- Alternatives allow for
  - further reduction in cable bundle size
  - build redundancy
- Alternatives may have their own risks / complications

Does it work (LV power)?

- Can the WIB provide enough power to the FEMB with just 8 twisted pairs ?
  - Yes, see document attached to these slides
  - Each FEMB consumes at most 47 mW per channel at 2.5V (2.4 A total)
  - Power provided with 7 AWG20 pairs (8th pair used to provide bias voltage to the linear voltage regulator)
  - At warm: bundle of 7 AWG20 twisted pair wires has resistance of 41 mΩ for 9 m length (upper APA), 101 m Ω for 22 m length (lower APA), to compensate voltage drop WIB will provide 2.7V to upper APA, 3.0V to lower APA, power dissipated in cables: 0.5W per FEMB (upper APA), 1.2W per FEMB (lower APA)
  - At cold: resistance and power dissipation in cables reduced by factor 3 (operate at ~2.6V for upper APA, 2.7V for lower APA)
  - Lower APA: at most 10W total dissipated inside each APA side tube when cold (power for 20 FEMB is 120 W)

Does it work (LV power)?

- Voltage drop is still reasonable (particularly when cold)
- Exact value of voltage provided from the WIB to the FEMBs will be configurable (and measured/controlled) on the WIB
- If we allow for slightly larger voltage drop, larger heat deposit in the twisted pair cables we could
  - Further reduce number of connections, or
  - Reserve 1 pair for voltage sensing
- We could also consider adding voltage monitoring capabilities on COLDATA

If we use the CRYO ASIC

- CRYO power requirement is smaller, will use 7 AWG20 pairs for 2.5V, last AWG20 pair reserved for voltage sensing
- CRYO data connections:
  - four 896 Mbps links (two from each CRYO chip)
  - two 56 MHz clock signals (one for each CRYO)
  - four SACI signals for configuration (shared between the two CRYO chips)
- This cannot be tested until we fabricate the 2nd version of CRYO (Spring 2020)
  - Currently require five SACI signals for two CRYO ASICs, need to add internal address in CRYO chip (via e-fuses or wire bonds on board) to make this work

Conclusions

- We do not have an hardware demonstration that the number of cables can be reduced (will come in Fall 2019
- However the assumption that we can use only 10 signal connections and eight AWG20 twisted pairs for power is on more solid ground
- Further reductions are possible, could be used to build redundancy in the system, facilitate cable sliding / contraction inside the APA frame
- The power dissipated in the cables inside the APA frames is small (5 W total over 6m of tube, for each of the two side and lower and upper APA, 20W total), small compared to the power dissipated in the FEMBs (6W per FEMB)