JAVIER FERNANDO CASTAÑO FORERO

PhD in Applied Science
Postgraduate Diploma in Telematics
Electronics Engineer (BSE)

Assistant Professor
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PROFESSIONAL PROFILE

PhD in Applied Science, Electronics Engineer (BSE). Teaching and research experience for the development of R+D+i activities, in the areas of radiation and particle detectors, applied cryptography, digital systems, reconfigurable hardware, digital signal processing, applied mathematics and telematics; with experience in administrative tasks and emphasis on ethics, dedication to service and teamwork; with an open mind to research and innovation.

EDUCATION

✍ DOCTORATE (2013-2016)

PhD in Applied Science, Universidad Antonio Nariño-Bogota (Colombia)

Scholarship from Universidad Antonio Nariño

Researcher in the Detectors Laboratory and the Complex Systems Group (Universidad Antonio Nariño)
Thesis: Visible light communication system based on silicon photomultipliers: optical wireless multiple access. Advisor: Rafael M. Gutierrez, PhD.

Subject: Development of a new multiple access technique for Optical Wireless Communication systems, Ethernet-UART bridge implemented in FPGA using VHDL and the complete hardware for router capabilities and network connection.

✍ POSGRADUATE DIPLOMA (2010)

Universidad Autonoma de Colombia - Bogota
Concentration: Telematics

Thesis: Study of cryptographic hardware and its impact in telematics systems

Subject: Development of cryptographic hardware on FPGA and performance evaluation for telematics applications

✍ GRADUATE (2006)

Universidad de los Llanos - Villavicencio
Electronics Engineer BSE

Thesis: Design and implementation of a prototype of point-to-point data transmisión with encryption based on elliptic curves. (Magna cum laude)

Subject: Development and evaluationof elliptic-curve cryptography on FPGA and application in telematics.

OTHER RESEARCH EDUCATION

ICFA School for particle detectors and applications 2013. Universidad de los Andes (Colombia) and CERN

INTERNATIONAL RESEARCH EXPERIENCE

- Visiting Research Fellow in the University of Bristol (UK), from February 2019 to April 2019 (7 weeks). Developing of PUMA (Plataforma Utilizada para Muestrear Arapucas), a 40-channel, 14-bit, 65MSps digitizer board focused to acquisition of signals from SiPM
- Research Stay in the IFIC (Instituto de Física Corpuscular) of the Universidad de Valencia (Valencia, Spain), from January 2017 to March 2017 (3 months), participating in the NEXT Experiment, funding by Invisibles Plus ITN of the EU.
- ESR Secondment Invisibles ITN Network, Internship in Hamamatsu Photonics (Iwata, Japan), from October 2014 to December 2014 (2 months). Trainning on PMT (Photomultiplier tubes) test and applications.

SKILLS

- C/C++ Language for microcontrollers
- VHDL and Verilog hardware design and implementation in Xilinx and Altera FPGA(CPLD)
- Digital communications systems design, Ethernet protocol and interfaces
- Python Language
- Matlab
- Xilinx ISE Design Suite and Vivado
- Altera Quartus
- Cadence Allegro
- 32-bit ARM-based microntrollers
- System-on-chip SoC applications
- Raspberry Pi applications

LANGUAGES

- Spanish (Native)
- English