LArPix v1 testing

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DUNE Pixel Readout Weekly Meeting

2019/5/9

BERKELEY LAB

LArPix v1 demonstrated performance

- See paper: arXiv:1808.02969

Main performance specs:

  - Leakage current: 500e-/ms (warm), 500e-/s (cold)
  - Gain: 1mV/250e- (rough)
  - Pedestal: 350mV (warm), 550mV (cold)
  - Pedestal RMS: 1.5mV (warm), 1.1mV (cold)
  - Trigger threshold: 12-18mV (both)
  - Power: 62uW/ch (tuned supply voltages)

LArPix v1 “quirks”

- See appendix for complete description

Quick list of quirks / issues:

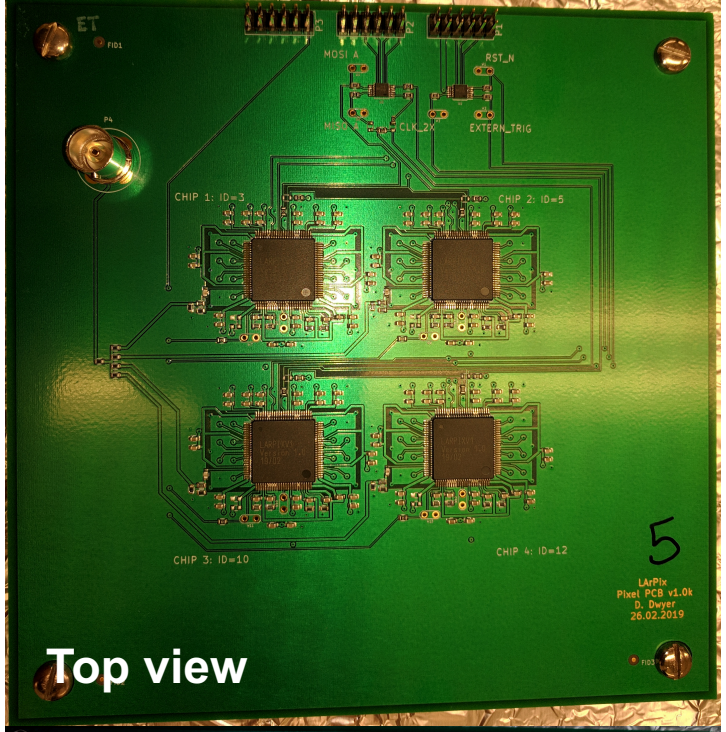
- ADC bit errors (Missing MSB and LSB)
- Test pulser issues (risetime and linearity)
- Bad initial configuration
- Deadtime
- Buffer risetime
- FIFO timestamp
- Leakage current (due to surface properties)
- Periodic reset
- Daisy chain IO difficulties

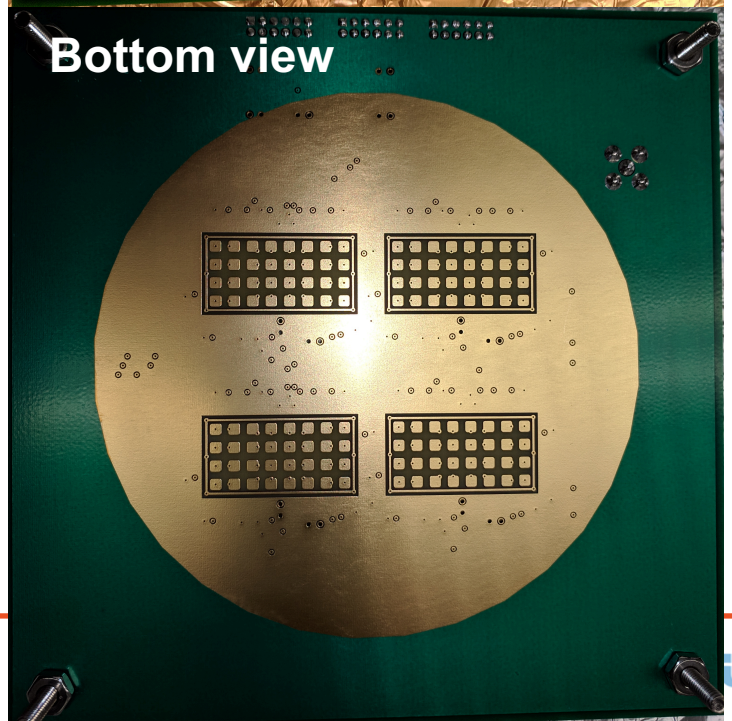
Testing of chip packaging with v1 ASIC

LArPix v1.5 anode

Dedicated test anode to evaluate chip packaging and single-board PCB design

- Unified 8-layer board construction
- Hosts 4 QFP100 packaged LArPix v1 ASICs
- 120 active channels with square pixel pads
- 4 external test-pulse channels (1 per chip)
- 4 unbonded reference channels (1 per chip)
- MISO test point for each chip
- Diode array for ESD protection on external MISO/MOSI lines

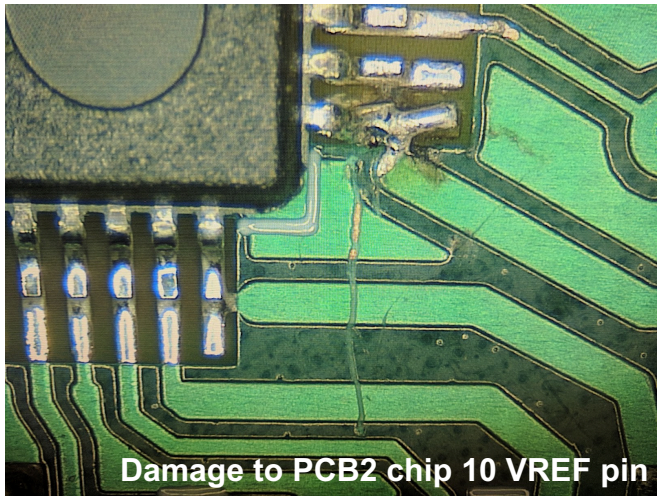




Basic functionality

Visual inspection

- OK, some damage to one pin but did not introduce a short or break

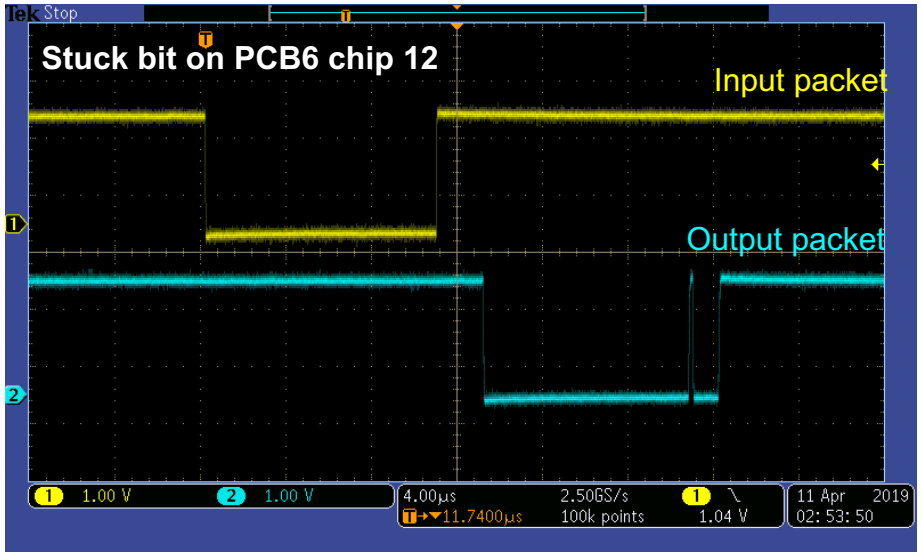


Continuity

- OK, no observed shorts or breaks between external lines or on chip pads

IO functionality

- 1/20 (95%) chips showed a stuck bit in the MISO data packet



Noise

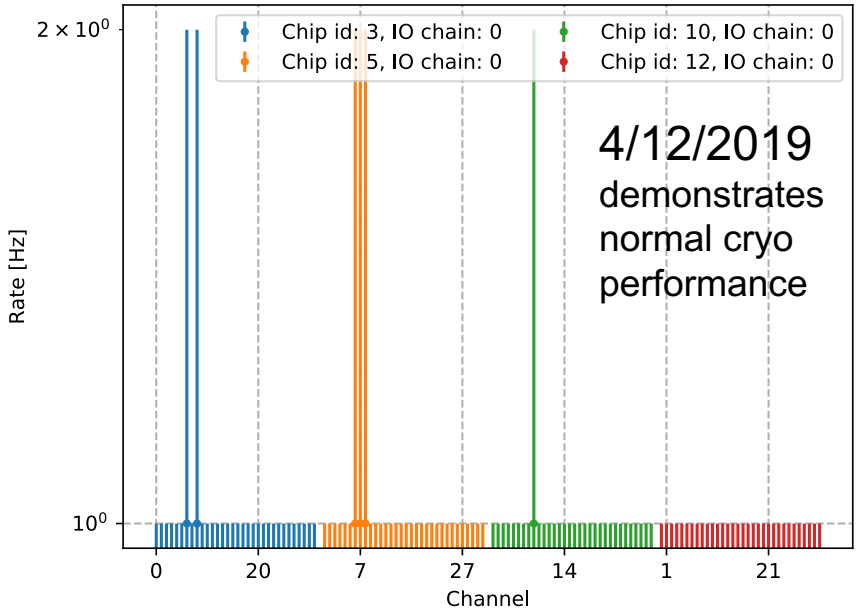
- OK, no significant increase in pedestal RMS from wirebonded board

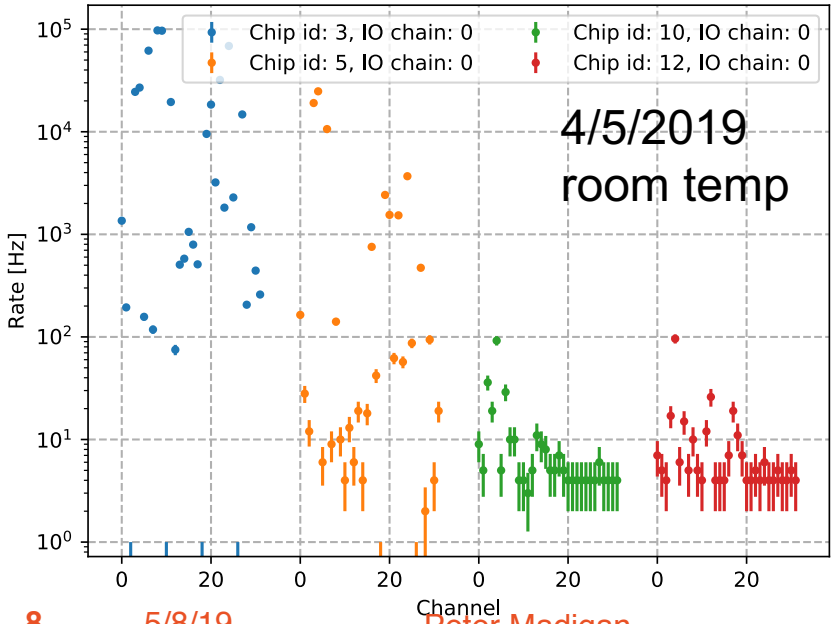
Time-varying leakage current

For 2/20 chips (chips 3, 5 of PCB4), observe time-dependent leakage current

- Initial testing showed very high leakage current that was not resolved with cleaning
- Subsequent tests show declining leakage current over the next 10 days

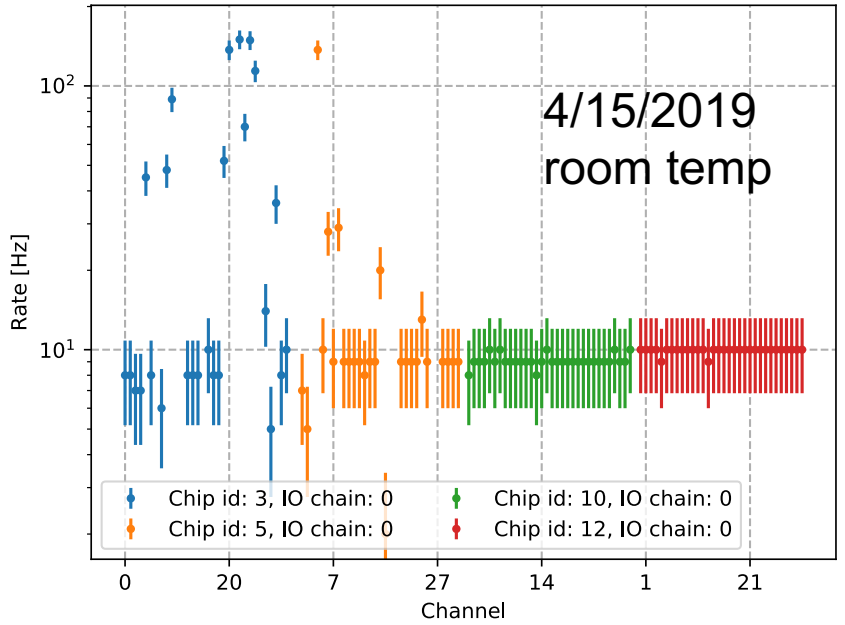
After 7 days, chips showed normal leakage at cold and only slightly elevated leakage at room temp.





10 days

>~1000x reduction

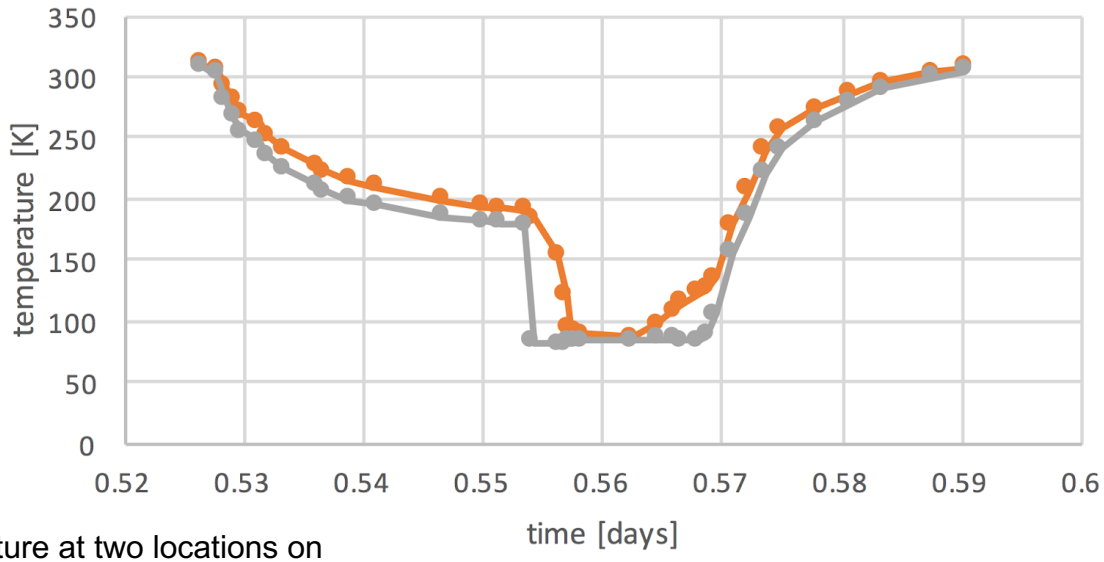


Cryogenic testing

Tested 19 remaining chips in LN2 bath

Results:

- No failures during cryocycle
- Noise and leakage performance is comparable to wire-bonded chips
- Multi-cycle testing of one board (4 chips) shows no failures after at least 5 rapid cryocycles
  - Note: failed header pin connector during rapid cycle testing



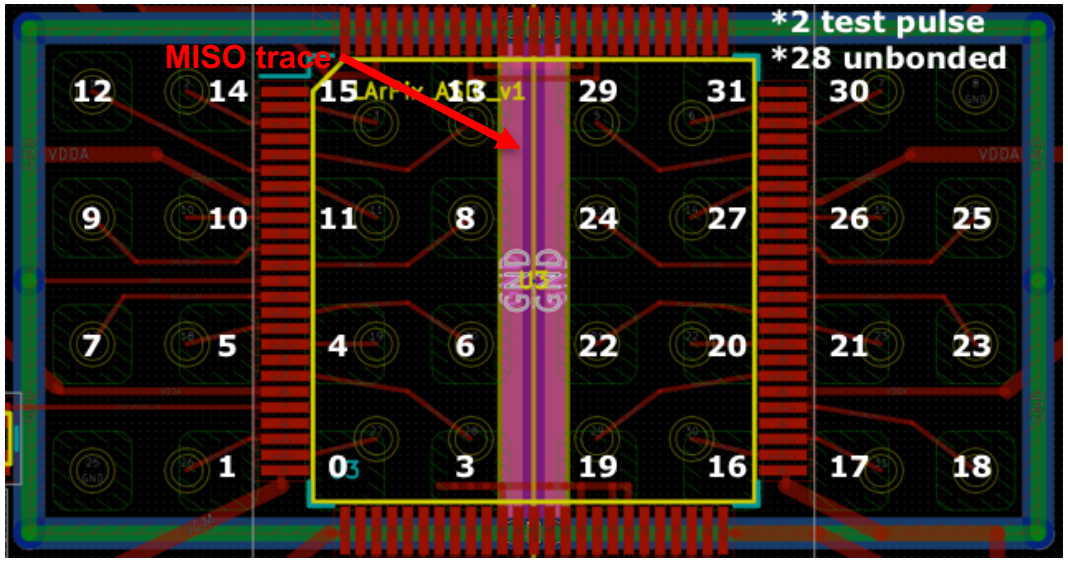
Temperature at two locations on PCB during one complete cryocycle

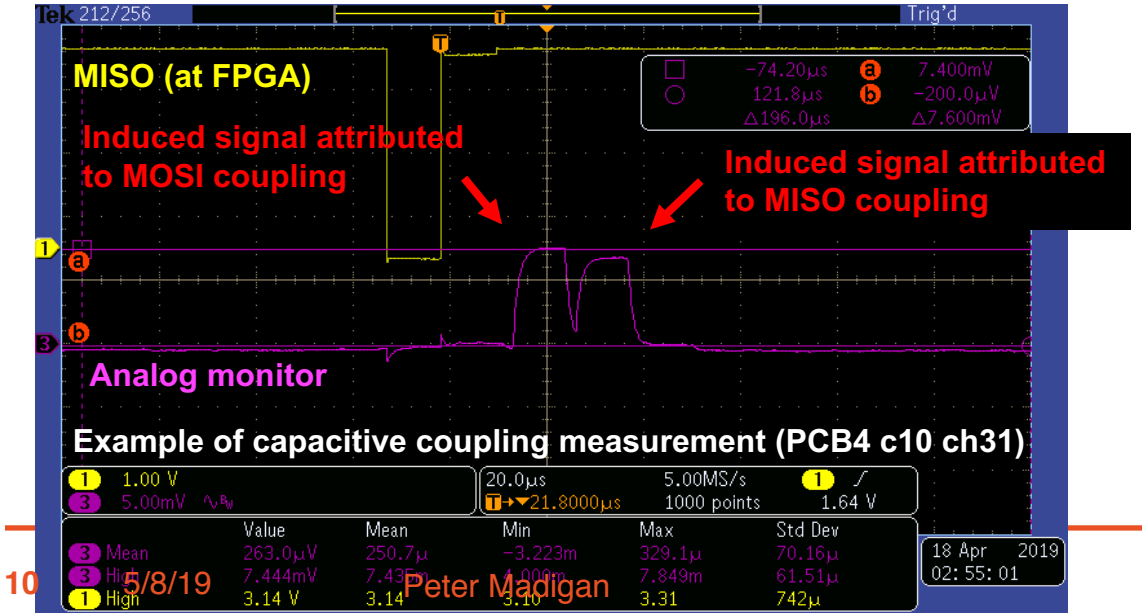
Capacitive pickup

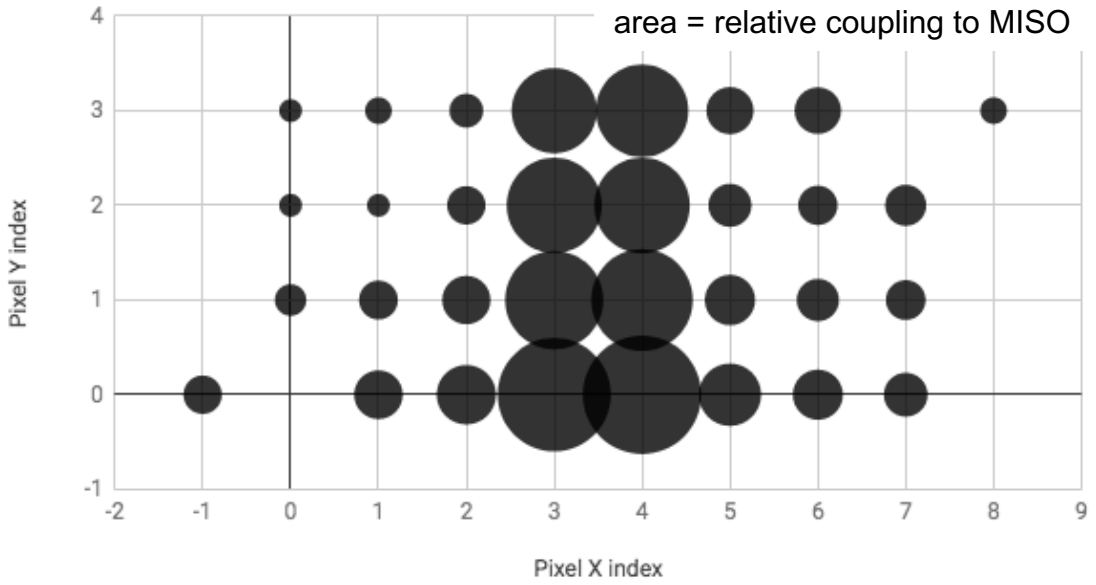
Observed significant capacitive pickup from digital IO lines

Measured capacitance between MOSI/MISO and front-end to be ~50aF (typical) to ~1fF(worst)

Strongest coupling for channels adjacent to trace under chip







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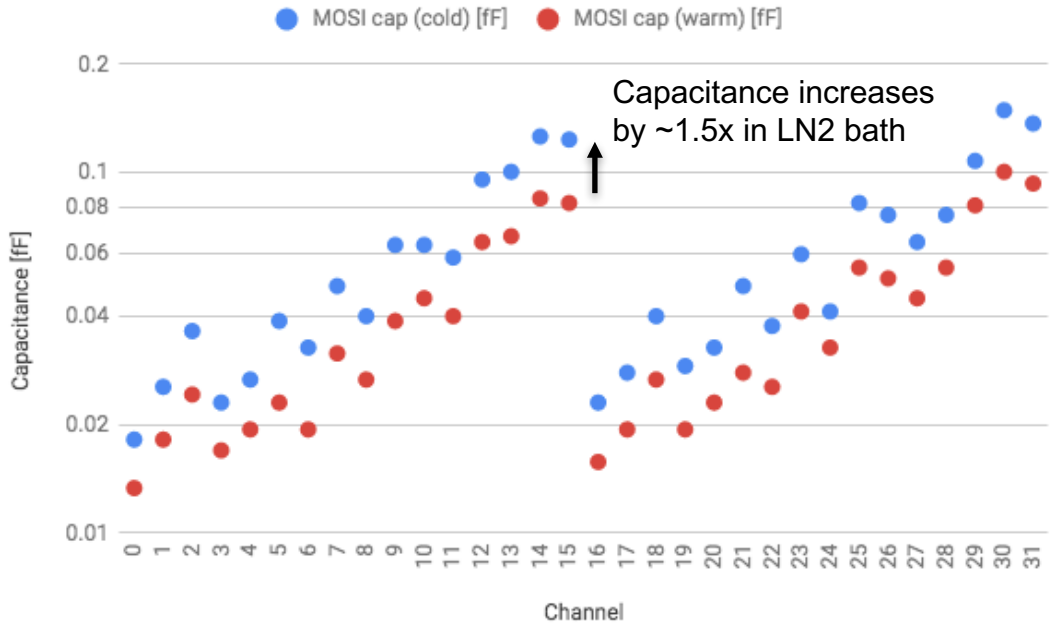
Capacitive pickup mitigation

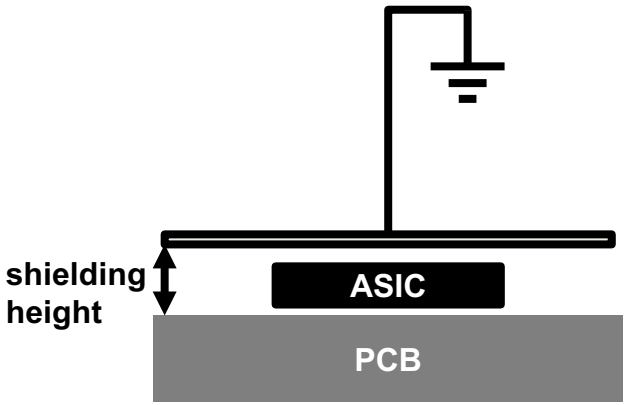
Coupling increases ~1.5x in LN2 suggesting that field lines exit chip packaging

Tested mitigating capacitive pickup via grounded shield above chip

- v2 will also have the capability for differential signaling, further reducing capacitive effect



Modification (PCB4 c10 ch28)	MISO coupling	MOSI coupling
None	2.8mV	4.5mV
Grounded plate @ 9mm	1.1mV	2.7mV
Grounded plate @ 2.5mm	<0.5mV	<0.5mV
Remove packaging foot	2.3mV	3.8mV



Packaging and assembly yield

3 bad chips were identified by vendor

- Wirebonding failure

No issues encountered during assembly

PCB6 chip 12 had stuck bit in outgoing packet

PCB2 chip 3had all front-end channels saturated

No issues encountered during cryo-tests

Stage / test	Input [chips]	Pass [chips]	Fail [chips]	Yield [chips]
Packaging	158	155	3	98.1%
Assembly	20	20	0	100%
IO functionality	20	19	1	95%
Front-end functionality	20	19	1	95%
Cryo functionality	19*	19*	0*	100%*
			Net:	88%

*includes chip with saturated front-end, since digital functionality was ok in LN2

Summary of package chip testing

- Overall dicing to operation in LN2 yield is ~90%
- No cryogenic failures have been observed with packaged chips
- Time dependent leakage current physical process is still unclear
- Very small capacitances to large voltage swings lead to significant induced signals, mitigation will be important for low threshold operation
  - Potential avenues to be pursued:
    - differential signaling with v2 chip
    - package shielding (at what cost?)
    - external shielding (at what design headaches?)

Continuing packaging testing efforts

- Compare measured capacitance with/without packaging (and potentially with wirebonds of different lengths)
  - Appears as though the capacitive coupling has increased (since it was not noticed before), this should be confirmed
- Perform a more complete assessment of capacitive pickup with a proxy mitigation technique
- Develop a socket board to repeat baseline tests on remaining 135 chips
- Perform a replacement of the non-functioning chips and assess performance
- Investigate time varying leakage current closer (revisit data and map out channel variations)
- Produce 5 additional DAQ boards for v1 ASIC for groups interested in getting involved (UTA, Caltech, CSU)
  - Waiting on component delivery
  - In recent visit, Zoya and Leon (Caltech) were up and running with control software in just a couple days
  - Documentation is ongoing

Broader efforts in preparation for v2 testing

- Testing database and tracking:
  - Have: basic web-app and database with QR code support
  - Need: hosting (nersc?) and determination of QR code attachment (cryogenic stickers or production etching)
- Control software revamp:
  - Have: larpix-control software for v1 ASIC and IO structure
  - Need: larpix-control software for v2 ASIC and IO structure
  - Want: incorporate a standard testing library that helps automate running tests / uploading results to database
- DAQ system:
  - Have: a python-based DAQ framework and webpage gui (Sam K)
  - Need: implement and use this in standard operation

Lots of places for groups to get involved!

Appendix

Bad default configuration

Issue: Default configuration threshold is too low and one bit is incorrectly set

Consequences:

- Chips quickly saturate FIFOs and continuously produce data on reset
- No packet priority in daisy chain, so downstream chips cannot be configured with upstream chips in saturated state

Temporary fix: None, just be aware of this during start up. Care must be taken to configure chips in the proper daisy chain sequence

v2 fix: Default configuration will have all channels masked

ADC bug

Issue: Race condition in SAR ADC implementation

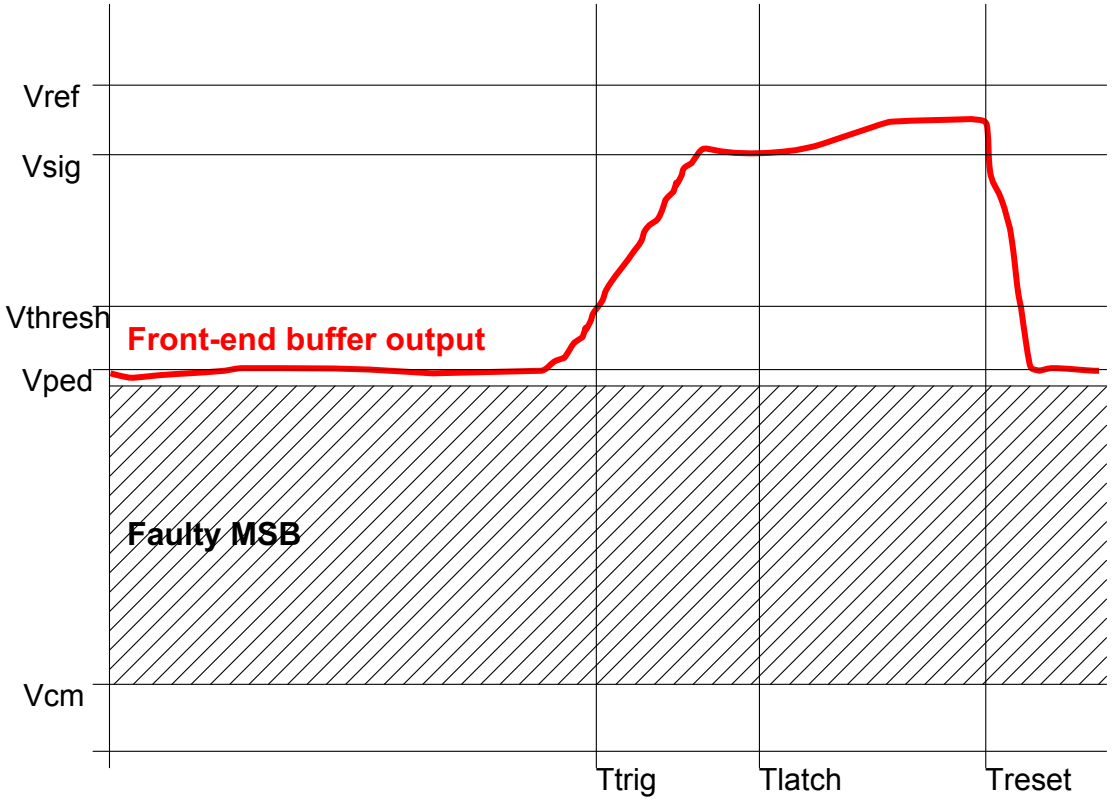
Consequences: Faulty MSB in range of 0-128 and stuck LSB in ADC data

Temporary fix: Tune VREF and VCM for 6-bit operation near signal region

- VREF = max(Vsig) + max(Vped)
- VCM > 2min(Vped) - max(Vped) - max(Vsig) > 200mV
- e.g. min(Vped) = 335, max(Vped) = 365, max(Vsig) = 100 -> VREF = 465, VCM = 205

v2 fix: Already fixed in design, confirmed with full timing simulations

Front end timing diagram



FIFO timestamping

Issue: Packets are timestamped when they enter the FIFO, not when the trigger is registered

Consequences: Multiple triggers that occur at the same time on the same chip will be timestamped sequentially with 3 tick offsets

Temporary fix: None, just be aware that there is a timing resolution degradation for multiple simultaneous triggers

v2 fix: Minor modifications to the trigger logic -> latch timestamp when discriminator fires

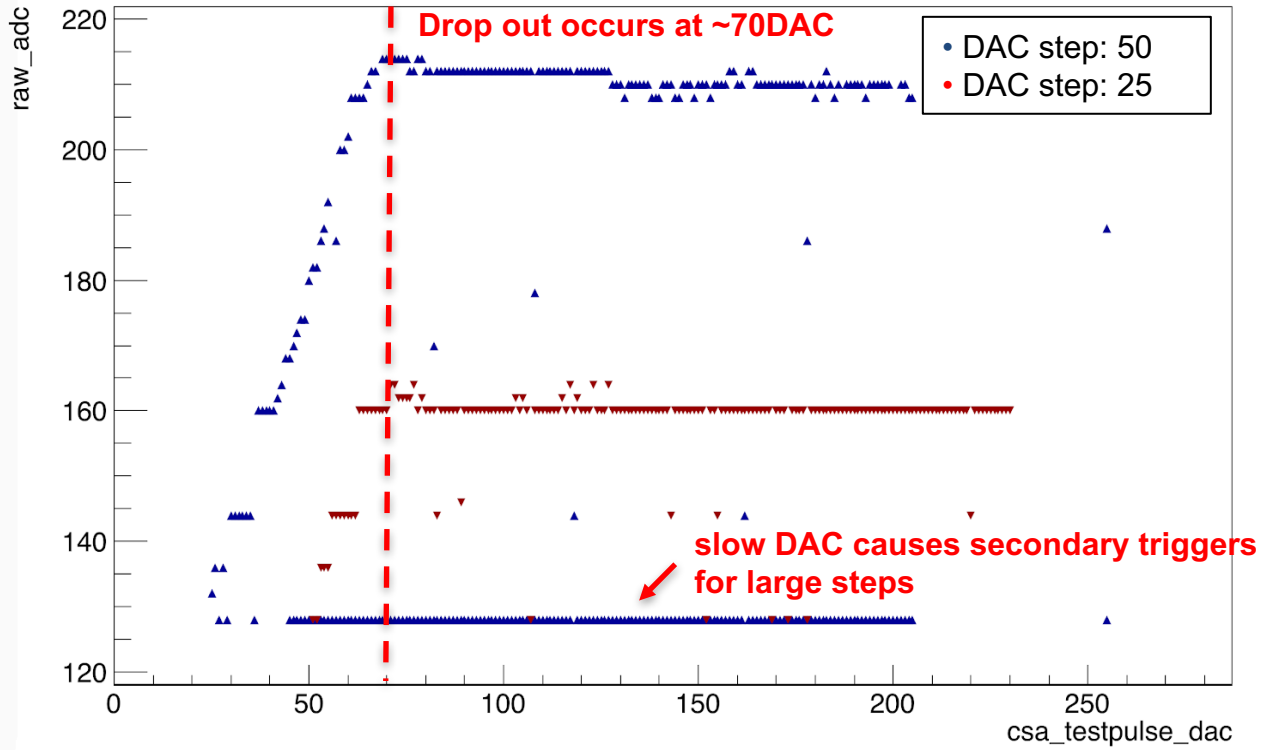
Pulse injection issues

Issues:

- Testpulser DAC is slow
- Testpulser is non-linear for low DAC values (<~70)

Temporary fix: Only test pulse in the upper half of DAC values

v2 fix: update DAC implementation to reduce drop out and increase speed



Channel dead-time

Issue: Channel reset occurs after ADC conversion

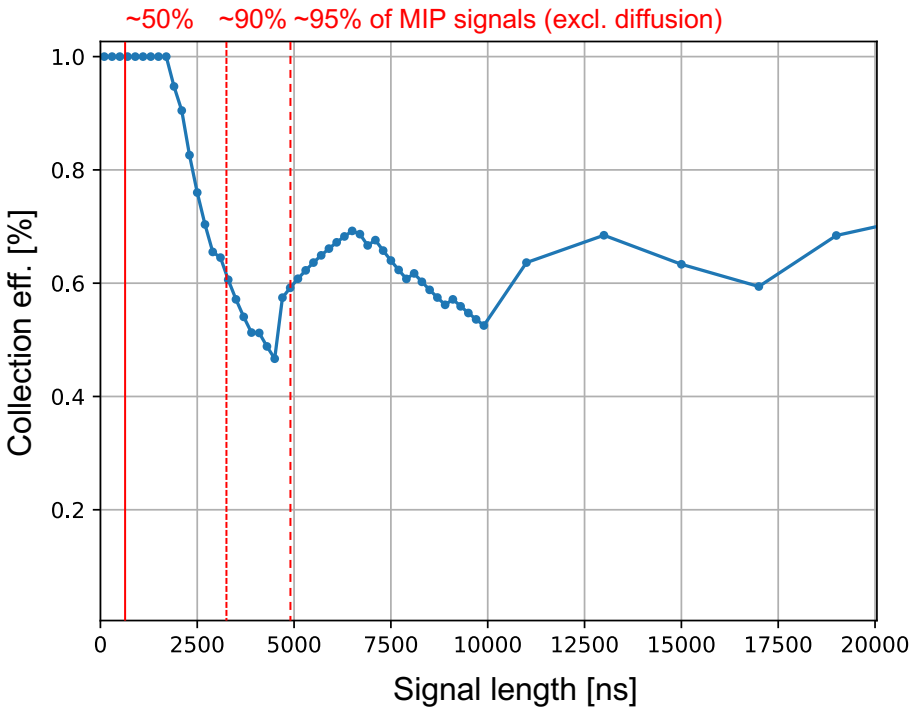
Consequences: Substantial dead time is introduced immediately following a channel trigger

Temporary fix:

- Utilize burst mode to digitize multiple times
- Increase digitization delay (sample_cycles)

v2 fix: Minor changes to the trigger logic

Primitive simulation of charge loss due to dead-time:



Buffer rise time

Issue: Buffer output from front-end CSA into ADC and discriminator has a rise time of ~1.6us

Consequences:

- Introduces dead-time
  - charge collected on front-end will only be reflected in ADC ~1.6us after collection
- Introduces secondary triggers
  - After reset, takes a while for output to settle to pedestal. Large amplitude signals can induce a ghost trigger

Temporary fix: increase digitization delay (sample_cycles) to let output settle before digitizing

v2 fix:

- reduce capacitive load on buffer
- increase buffer bias current

Leakage current

Issue: Surface properties can dramatically effect observed leakage current into front-end

Consequences: leakage current quickly integrates producing a high trigger rate on affected channels

Fix: Clean PCB surfaces with isopropanol*

*works in many cases, see description of chips with time-dependent leakage

Periodic reset

Issue: Periodic reset occurs regardless of channel's trigger state

Consequences: If periodic reset occurs during trigger, signal charge can be flushed before ADC latch

Temporary fix: None, just keep in mind that when periodic reset is enabled

- a small number of triggers may show subthreshold charge
- large digitization delays (sample_cycles) increase the likelihood of reset occurring during trigger

v2 fix: Periodic reset is ignored if channel has been triggered

Daisy chain IO troubles

Issue: With daisy chain IO structure, a single chip failure results in full daisy chain failure

Consequences:

- Difficult to diagnose chip failures without test points
- Anodes are particularly susceptible to single chip failures

Temporary fix: Include test points and bypass resistors on PCB to enable testing and re-routing of daisy chain

v2 fix: Switch to network IO structure (Hydra IO) that Dan has described elsewhere