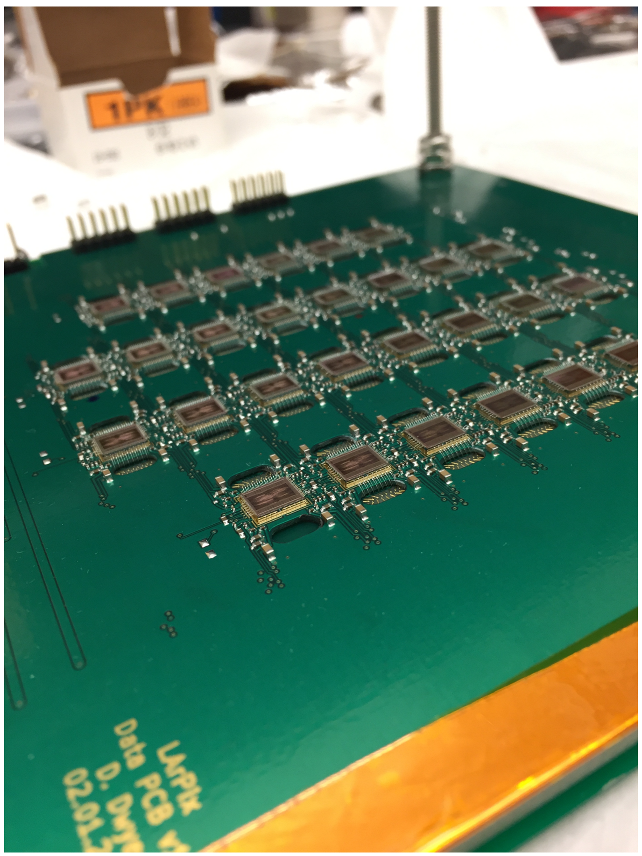
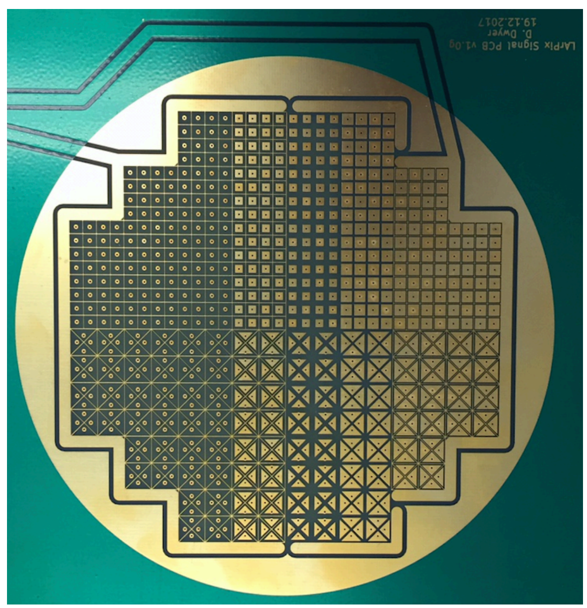
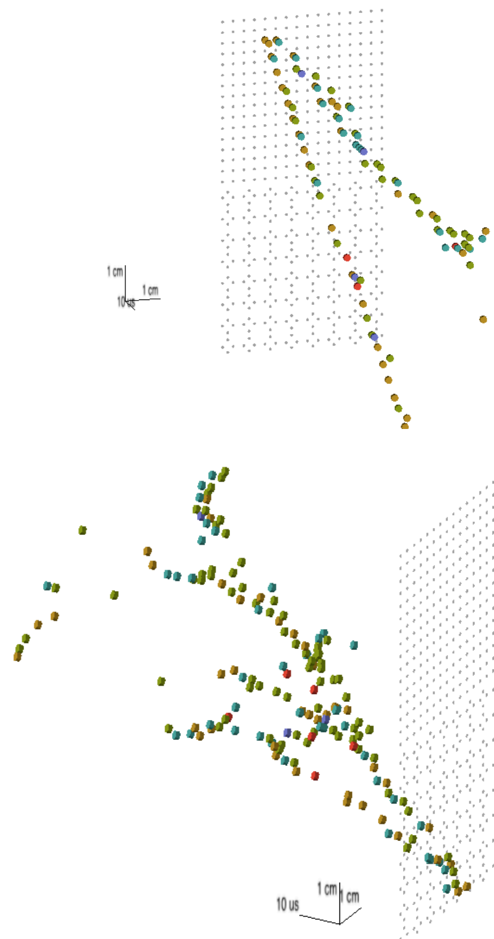
LArPix Design Details

Dan Dwyer (LBNL)

May 16, 2019







Introduction

Important that LArPix-v2 satisfies requirements for:

- Assembly, testing, and operation of the ArgonCube 2x2 Demonstrator
- Input for the DUNE Near Detector Technical Design Report

This talk:

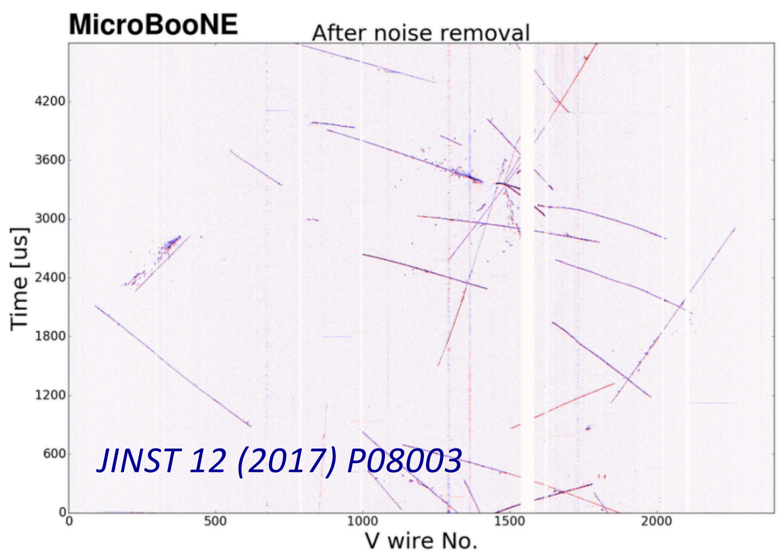
- Examine expected signal characteristics
- Describe LArPix-v2 analog and digital requirements
- Discuss modifications that facilitate assembly and operation

LArTPC Signals

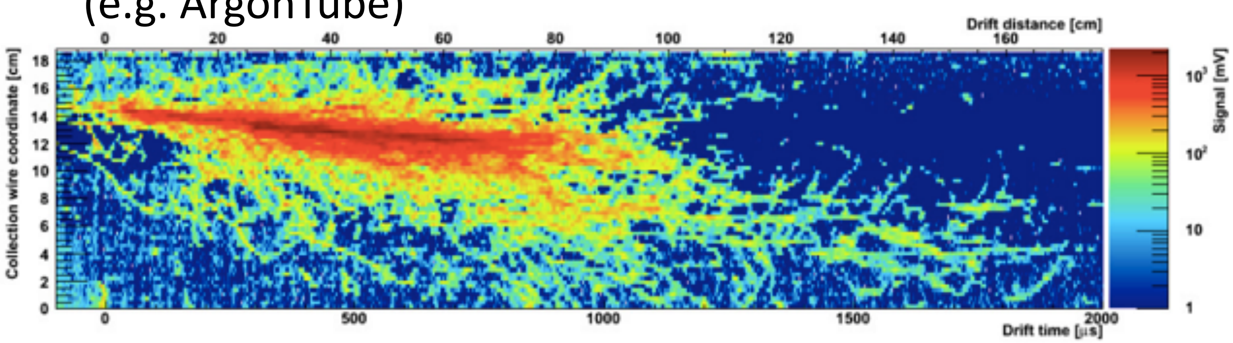
Primary signals of interest for ArgonCube 2x2 Demonstrator:

Operation on surface at Bern:

- Mostly MIP cosmic rays:

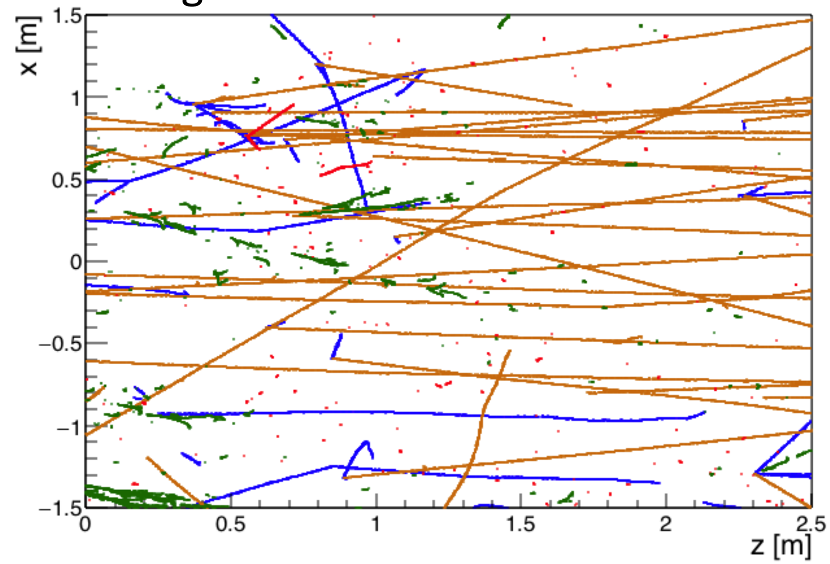


- Occasional intense cosmic shower
  (e.g. ArgonTube)



Operation underground at FNAL:

- Mostly neutrino interactions
  (mix of MIP tracks and small showers)
- Signals occur in bursts at ~1Hz



Example:
One simulated DUNE beam spill @ 2MW

LArTPC Spatial Resolution

Many aspects of design driven by desired LArTPC 3D spatial resolution:

- Resolutions of 3mm to 5mm in 3D are the regime of interest for DUNE signals.
- Above 5mm, clear degradation of physics performance for signals of interest
- Below 3mm, performance gain unclear. Electron diffusion during drift (~1 mm/√m) will eventually limit gains.

Anode spatial resolution:

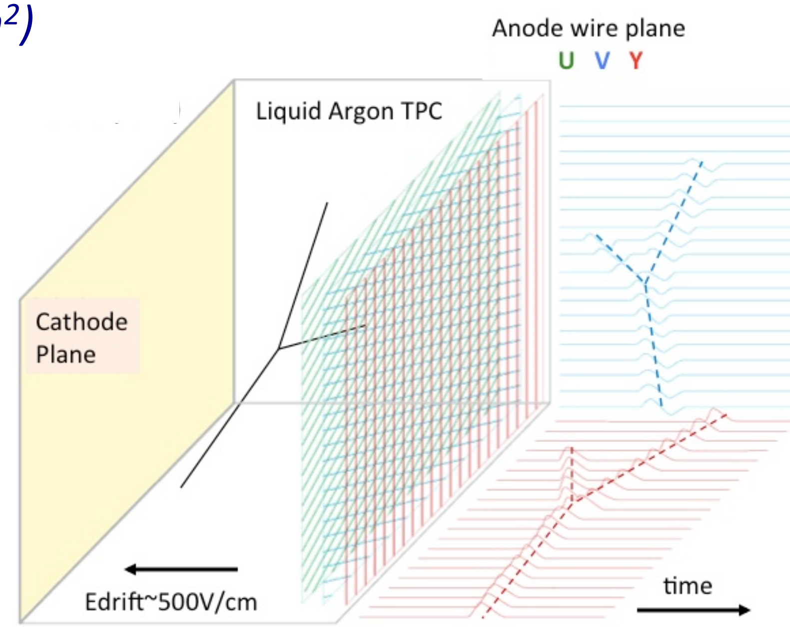
- Determined by pixel spacing.
- LArPix-v1 pixel system: 3mm pixel spacing
- ArgonCube 2x2 Demonstrator: Targeting 4mm spacing.

→ *Determines channel density (~62k channels/ m^2)*

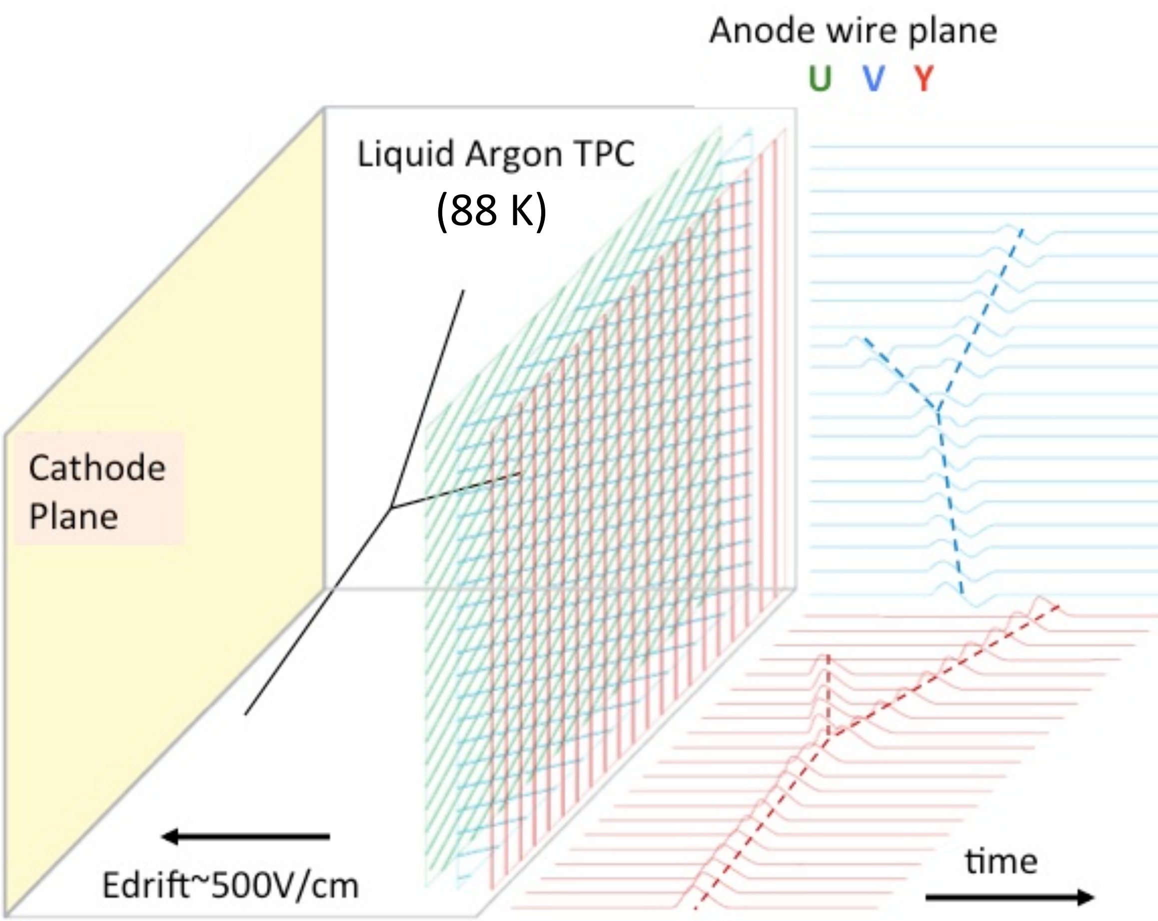
Anode time resolution:

- Time resolution of anode readout determines spatial resolution along direction of drift.
- Drift velocity varies with drift field, reference: 1.6 mm/µs at 500 V/cm
- 3mm-5mm resolution corresponds to 2-3 us 'binning' of incoming charge.

→ *Determines channel bandwidth, timing*



LArTPC Signals



Standard detection technique: Wire planes
Provide three views of interaction,
each 1-D vs. Z (i.e. drift direction)
arXiv:1107.5112

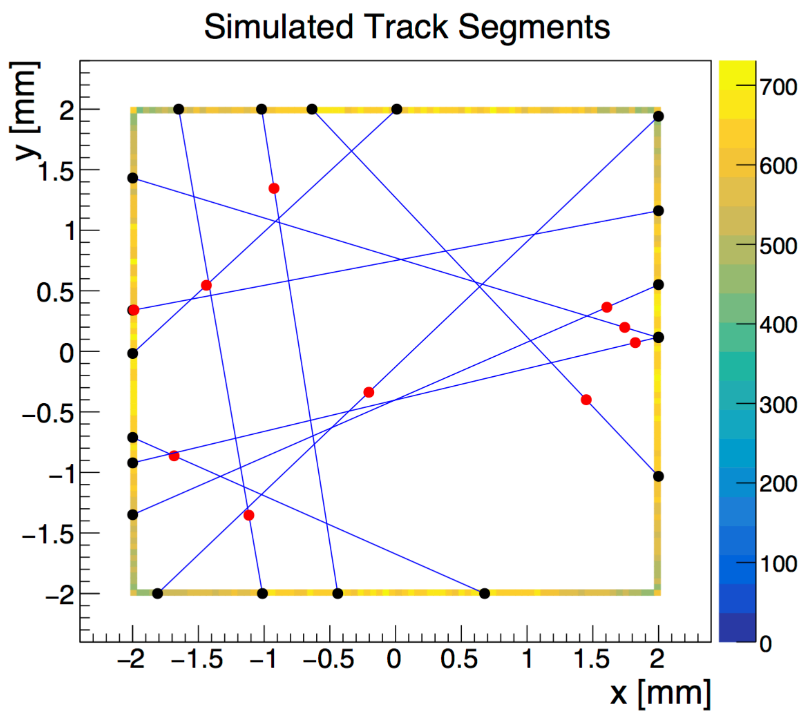
Ionization electrons:
23.6 eV per e-
→ ~42,000 e- / MeV
Recombination loss: *@500V/cm*
MIP: ~30%
Proton: ~70%
Drift velocity: *@500V/cm*
~1.6 mm/μs
Drift loss:
Few-% to ~50%, depending on
LAr purity and drift distance.
Charge signals: (approx.)
MIP: ~20k e-
Multi-proton: ~250k e-
(assuming 4mm pitch)

Minimum-Ionizing Signals

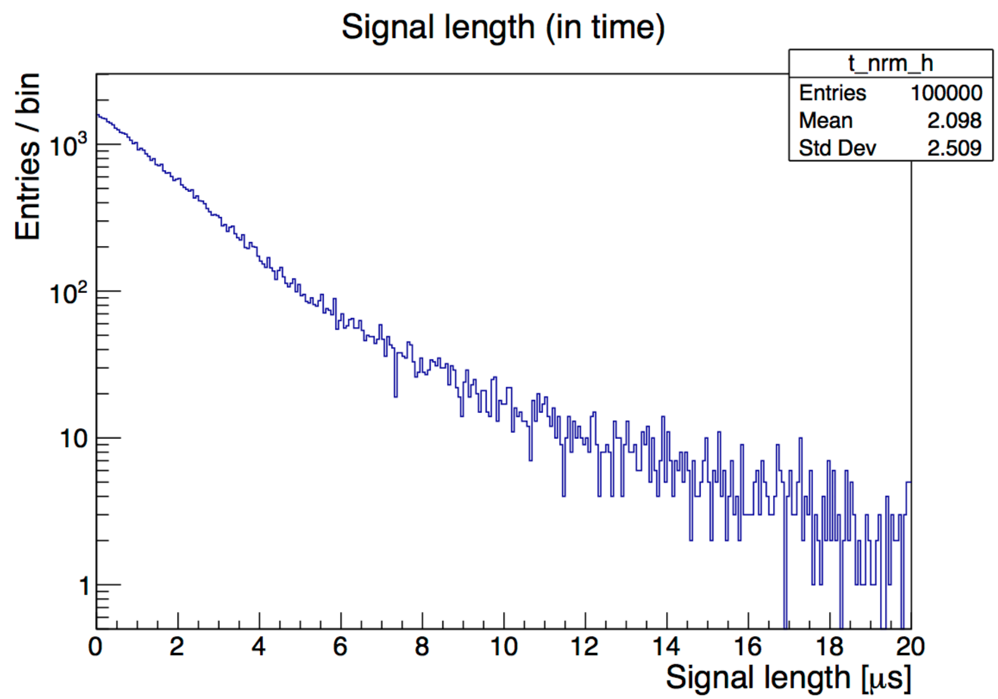
Rough calculation of expected MIP signal:

Model MIP track segments as ~5000 e-/mm, uniformly distributed in space

Simulated track segments in field of view of one 4mm pixel



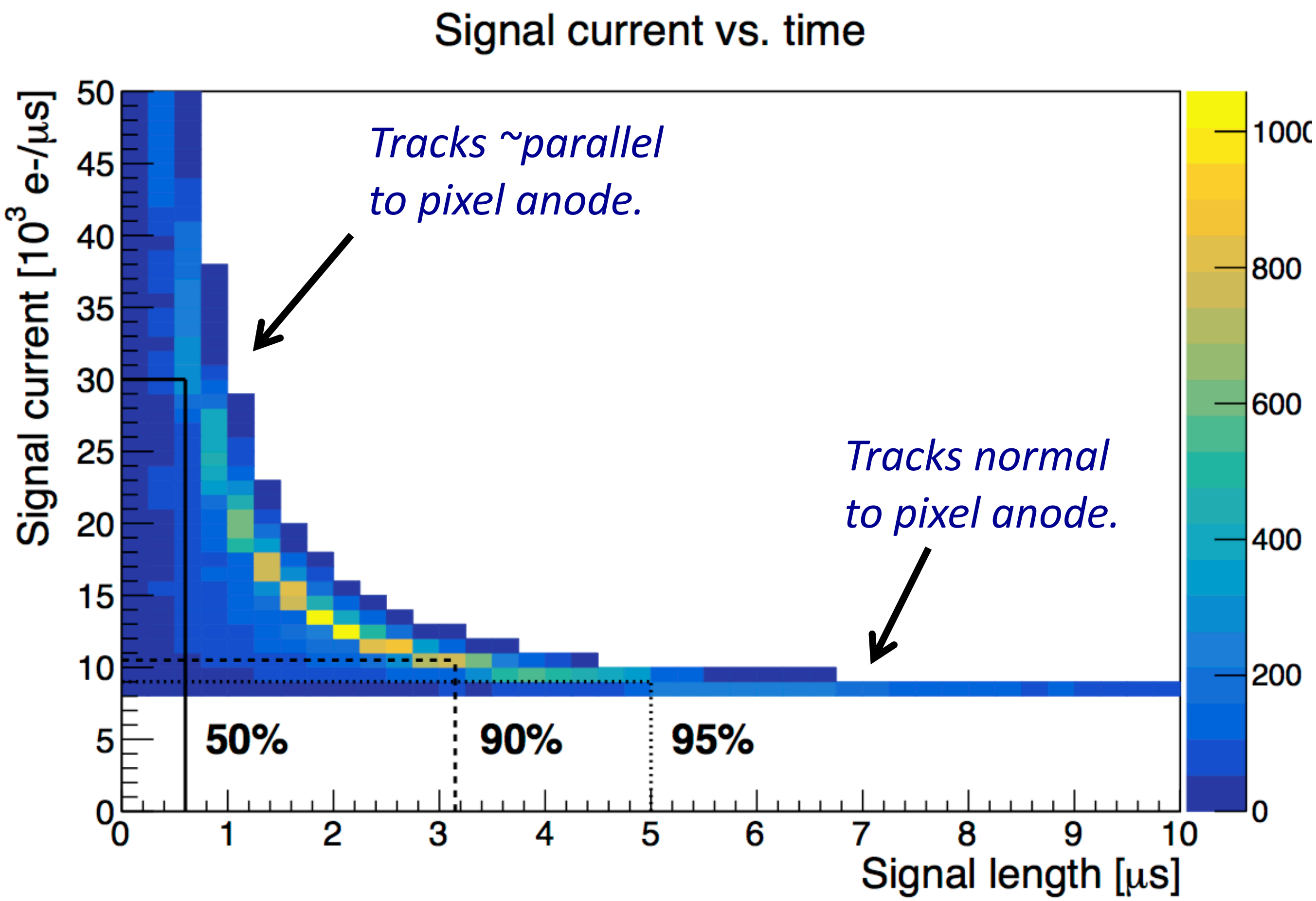
Length of signal in the drift direction, assuming drift of 1.6 mm/µs.



Minimum-Ionizing Signals

Rough calculation of expected MIP signal:

Model MIP track segments as ~5000 e-/mm, uniformly distributed in space



Note:
Electron diffusion during drift (~1 mm/√m) and pixel response will add dispersion to input signal.

Most MIP signals have short duration (<1 us) and total charge of ~20 ke-.
Few MIP signals have long duration (>5 us), with current of ~8000 e- / μs.

Pixel Signal Modeling

Implemented 3-D field and charge drift for pixel signal modeling.

Electron Paths:

Start in middle of 2-cm box,
along z=1cm ‘slice’,
from x=0.7cm to 1.3cm

Propagate in e-field until
electron strikes surface.

Configuration:

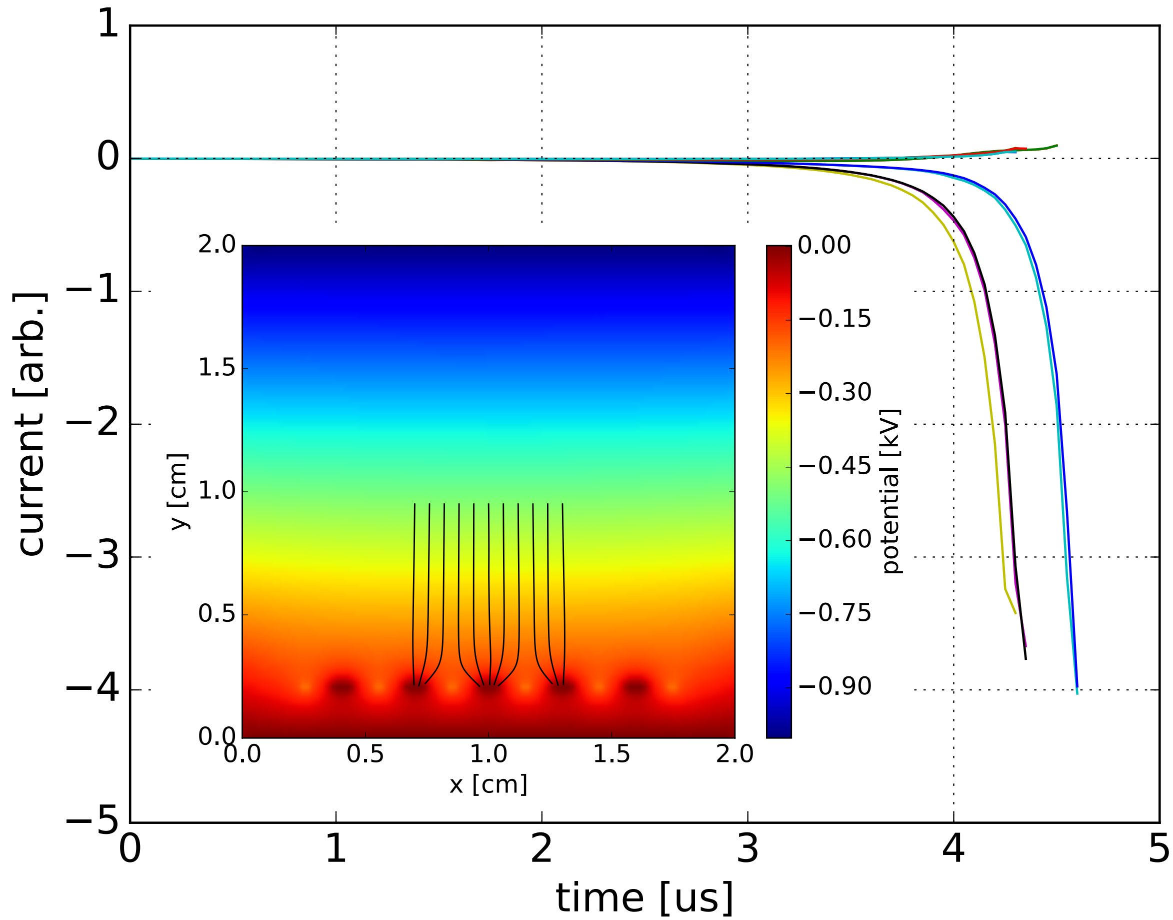
Drift Field: 500 V/cm

Focus grid potential: -200 V

Pixel pitch: 3mm

Observations:

- 200V focusing sufficient
- Signal time scale: ~1µs
- ~0.3µs variation in e- arrival
- ~3% signal induced on neighbor



D. Douglas now working on more refined model

Dynamic Range

Dynamic range of charge signals (in ~2 us intervals):

Low end:

Fraction of a MIP in one pixel: ~0.1-0.25 MIP → 2000 e- to 5000 e-

High end: (Not well understood)

DUNE:

Resolve ~5 protons stopping in one 'voxel' near neutrino vertex: ~250 ke-

Resolve MIP track ~parallel to wire

My rough estimate:

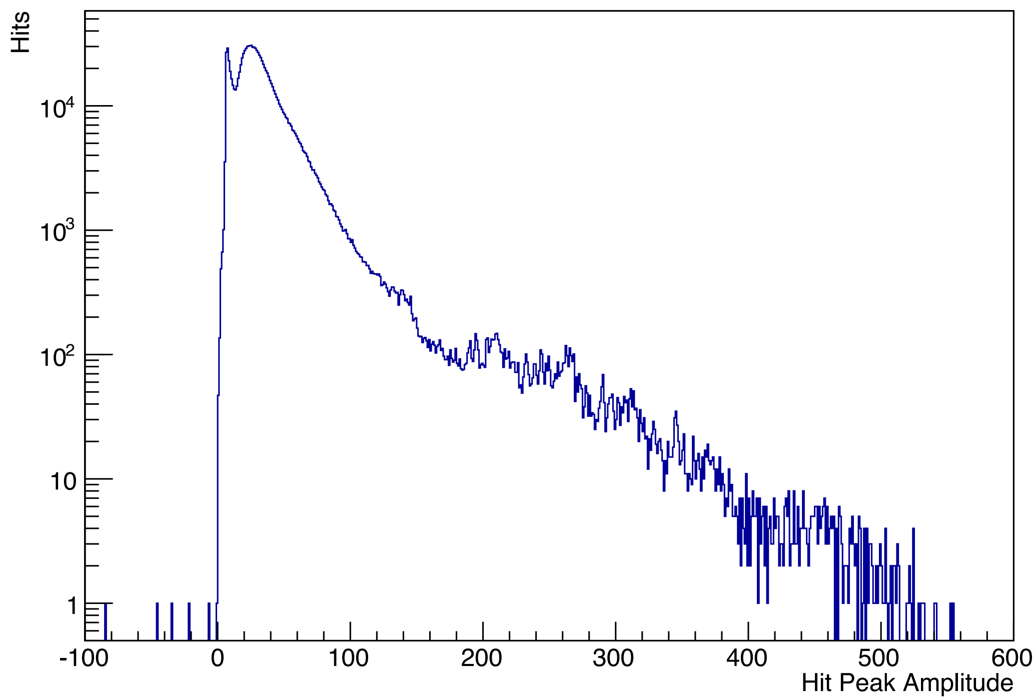
- Examine ProtoDUNE wire signal peak amplitudes (at 2 us shaping)
- Taken from 1 GeV particle beam run (mostly cosmics, with some beam signals)
- MIP peak: ~25, Max signals: ~500

→ *Suggests required dynamic range of ~20 MIPs.*

Caveat:

I'm not an expert in ProtoDUNE data, so might be overlooking some important aspects of this data (e.g. wire pileup).

Further study required.



Charge Uncertainty

Charge Uncertainty:

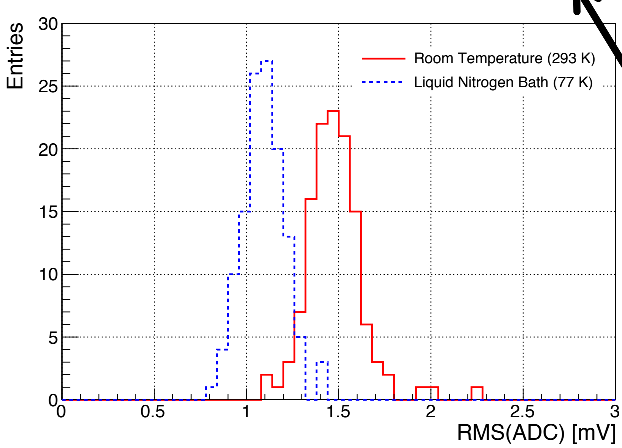
Any effect that distorts measurement of signal charge: noise, bias, etc.
DUNE: 500 e- ENC sufficient. Lower is better.

My rough estimate:

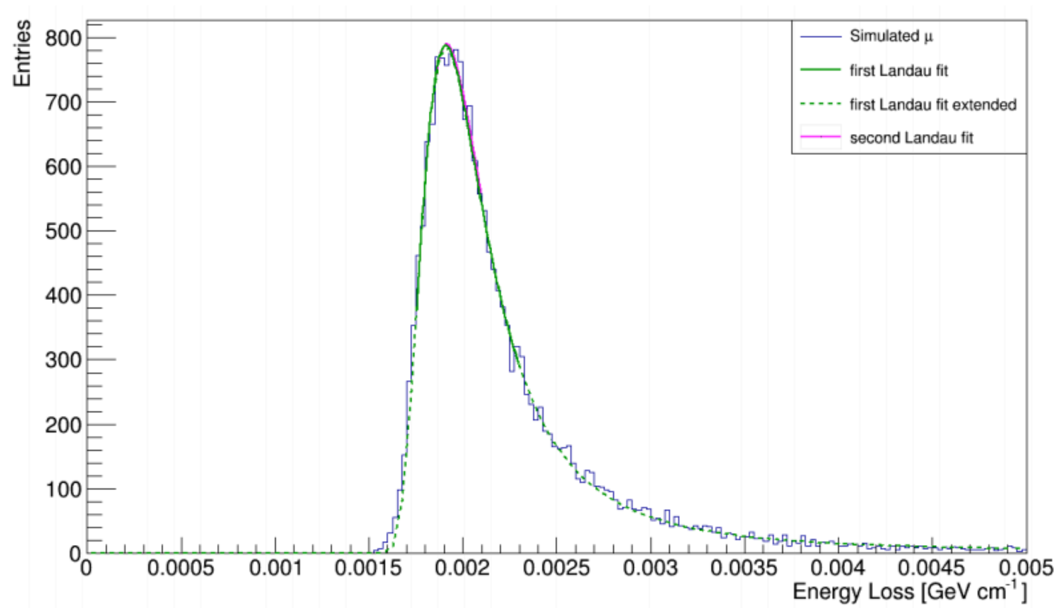
- Readout uncertainty should be smaller than natural stochastic fluctuations in particle energy loss per ‘voxel’.

→ Suggests < 5% uncertainty in measured charge

< 1000 e- ENC for MIP-level signals
< ~20k e- ENC for 20-MIP-level signals



~300 e- ENC demonstrated for LArPix-v1 ASIC in LN² bath.



Example Landau distribution for 200 MeV muon energy loss in liquid argon, as simulated using GEANT4 (K. Ingles, Muon Energy Loss in Liquid Argon, 2017)

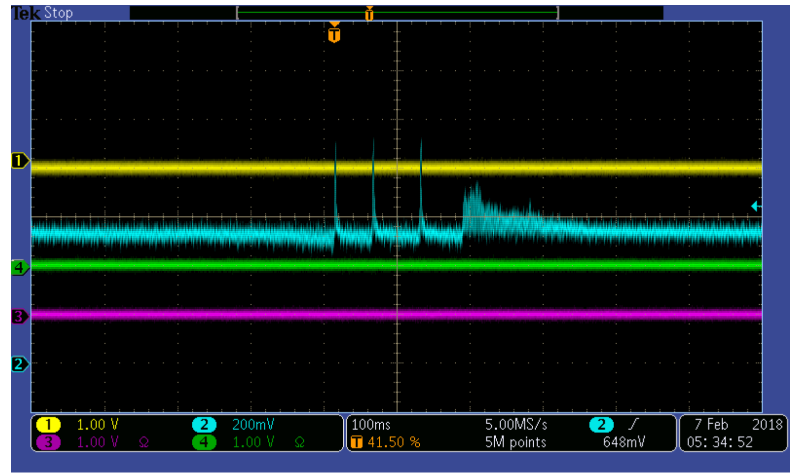
Question: Is a linear 12-bit ADC necessary?

Power

Heat generation in liquid argon must be controlled:

- Should be less than total heat flux through cryostat: ~10 W/m^2
- Local heating can boil LAr, impacting TPC performance. Limits on local heating poorly quantified.

Spurious signals from boiling seen with LArPix-v1 ASIC



Lessons from LArPix-v1:

- Minor boiling observed during initial operation
- Measured power consumption: ~62 µW/channel
- Slight increase in pressure (~6 cm of LAr) sufficient to suppress boiling.

Table 3. Average power consumption per channel for a 128-channel readout system at a clock operating frequency of 5 MHz. Values are given for two configurations: an initial default configuration of the supply voltages, and a configuration tuned for low-power operation.

Configuration	Source	Voltage (V)	Current (mA)	Average Power (μW/channel)
Default	VDDA	1.5	2.0	24
	VDDD	1.8	3.6	51
	VDDIO	3.3	8.5	219
				Total: 294
Low-power	VDDA	1.5	2.0	24
	VDDD	1.1	2.1	18
	VDDIO	2.0	1.3	20
				Total: 62

Cryogenic Operation

ASIC must stably operate in liquid argon (~87 K):

- Have operated ~60 LArPix-v1 ASICs in LAr. No cryogenic failures identified.
- ~25 v1 ASICs survived >3 thermal cycles with no noticeable change in performance.
- Successfully operated 16 v1 ASICs for continuously for ~1 week in LAr with no noticeable change in performance.

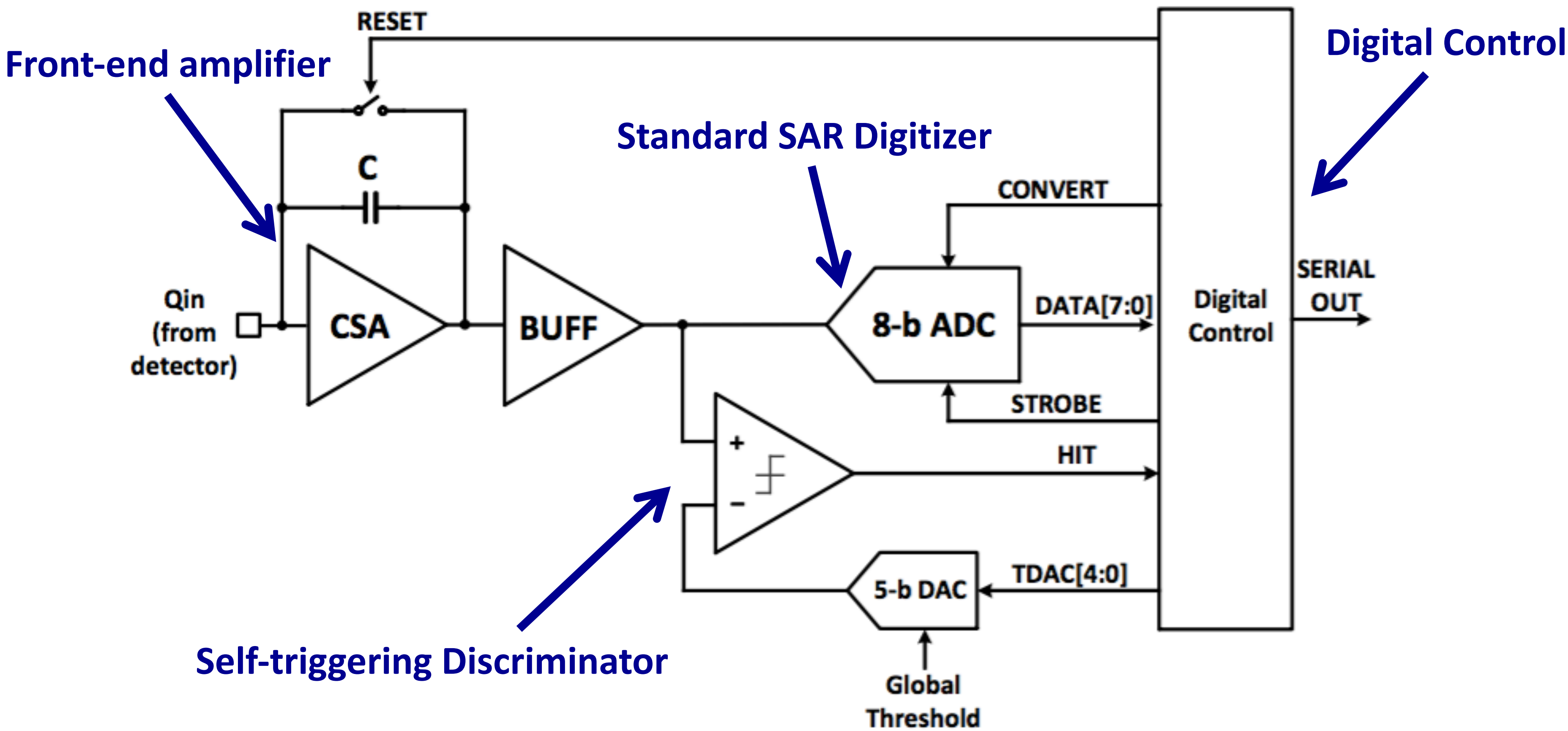
Requirements for LArPix-v2 in ArgonCube 2x2 Demonstrator:

- As a technical demonstrator, could likely suffer up to 5% ASIC loss during the planned ~6 months of ArgonCube 2x2 Demonstrator operation and still satisfy TDR needs.
- Loss here is defined as ASIC performance out of target specs.

LArPix Design

True 3D readout: A dedicated front-end channel for every pixel

Approach: Amplifier with Self-triggered Digitization and Readout



Achieve low power: avoid digitization and readout of mostly quiescent data.

LArPix: Design Details

Specification	Value	Units	Note
Number of Analog Inputs (channels)	~~32~~ (single-ended) 64 (v2)		
Noise	300 @ 88K 500 @ 300K	ENC, e-	Stipulated charge deposition is 15 ke- per MIP for a track in LAr
Channel gain	4 or 45	μV/e-	Digitally programmable
Time resolution	2	μs	with 10 MHz master clock rate
Analog Dynamic Range	~1300	mV	max signal ~ 250 ke-, minimum detectable signal ~ 600 e-
ADC resolution	~~6~~ 8 (v2)	bits	programmable LSB, 4 mV nominal (1 ke-)
Threshold Range	0 – 1.8	V	
Threshold Resolution	< 1	mV	nominal
Channel Linearity	1	%	
Operating Temperature Range	88 - 300	°K	
Event Memory Depth	2048	memory locations	~8 ms without data loss in case of track normal to pixel plane
Output Signaling Level	3.3	V	Tunable
Digital data rate	5	Mb/s	With 10 MHz master clock
Event readout time	5	μs	

LArPix Triggering

Self-triggering with pulsed reset ≠ Zero suppression

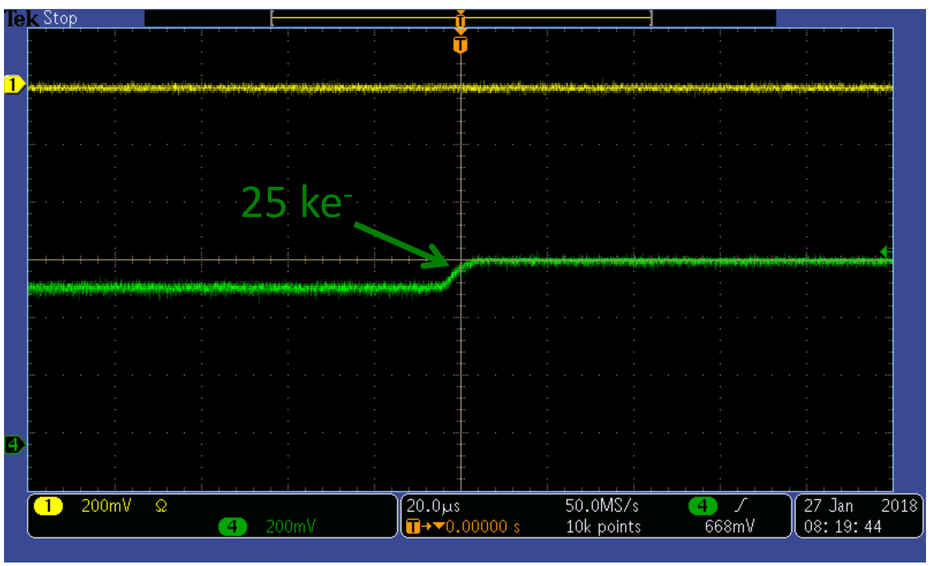
LArPix has no resistive feedback or shaping

→ Charge stays on pixel until you do something with it

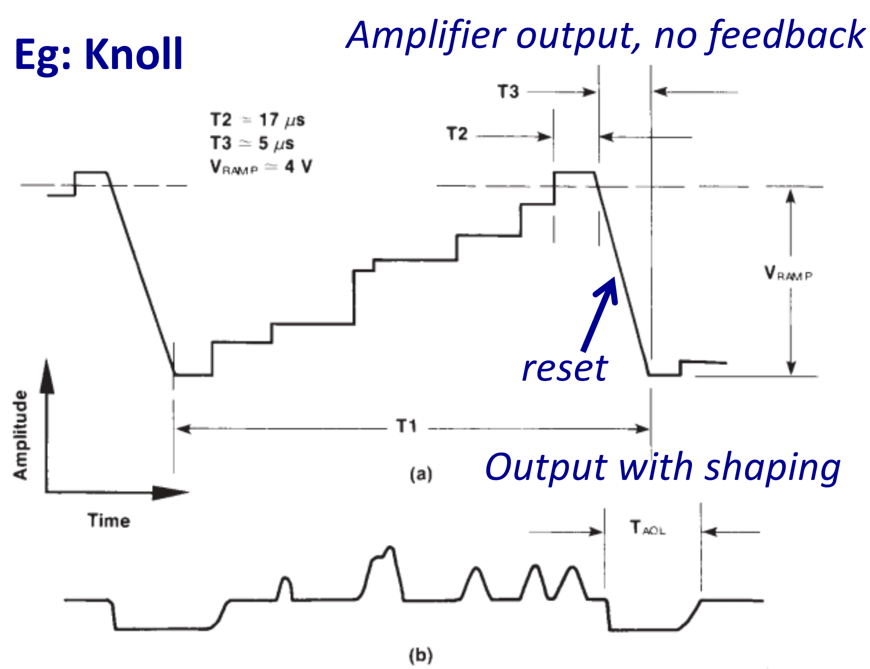
Your choices:

- Self-trigger reset: digitize and drain charge after threshold crossed
- External-trigger reset: digitize and drain sub-threshold charge based on external signal
- Cross-trigger reset: digitize and drain sub-threshold charge based on self-trigger of another pixel
- Periodic-trigger reset: periodically discard sub-threshold charge without digitization

Example MIP-scale signal, without reset



Eg: Knoll



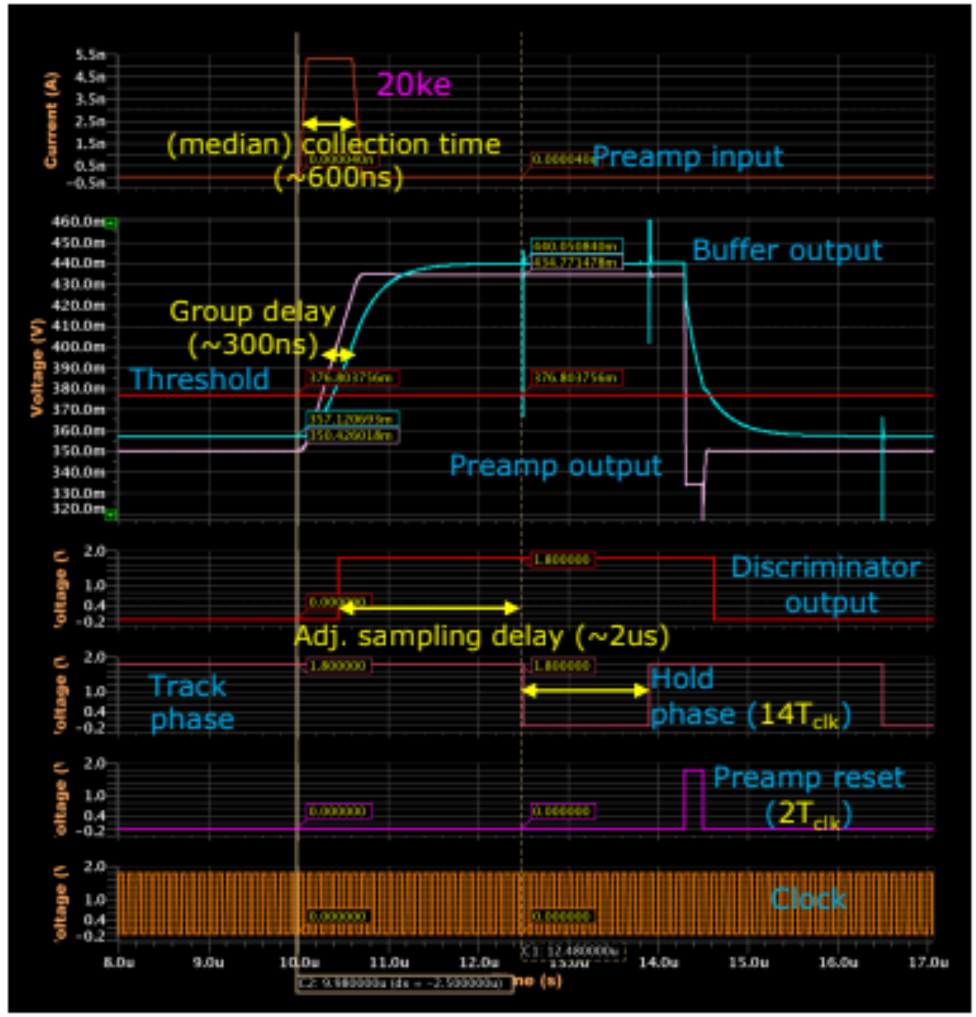
LArPix Channel Response

Detailed simulation of LArPix-v1 channel response

D. Gnani

'Typical' Timing

- Input collection current / track duration
  - 0-320us (600ns median)
- CSA preamp delay & settling time
  - 15ns & 80ns
- CSA preamp delay & (8-bit) settling time
  - T_{dly}=300ns; T_{stl}=1.8us
  - Settling time forces sampling delay ~2us
  - Min resampling time ~15.5us @T_{clk}=100ns
- Comparator delays
  - Prop. delay (signal dependent)
  - Clock capture delay ≤$1T_{clk}$
- ADC conversion time
  - $14T_{clk}$
  - $(4+2)T_{clk}$ recovery



Deadtime

CSA reset introduces 'deadtime'

- More accurately: signal charge loss during reset.

1) Direct reset loss:

Charge arriving between signal hold by ADC and recovery of CSA from reset is never seen by ADC.

2) Indirect reset loss:

Charge arriving shortly before signal hold by ADC, but insufficiently settled on ADC capacitors, is incompletely seen by ADC.

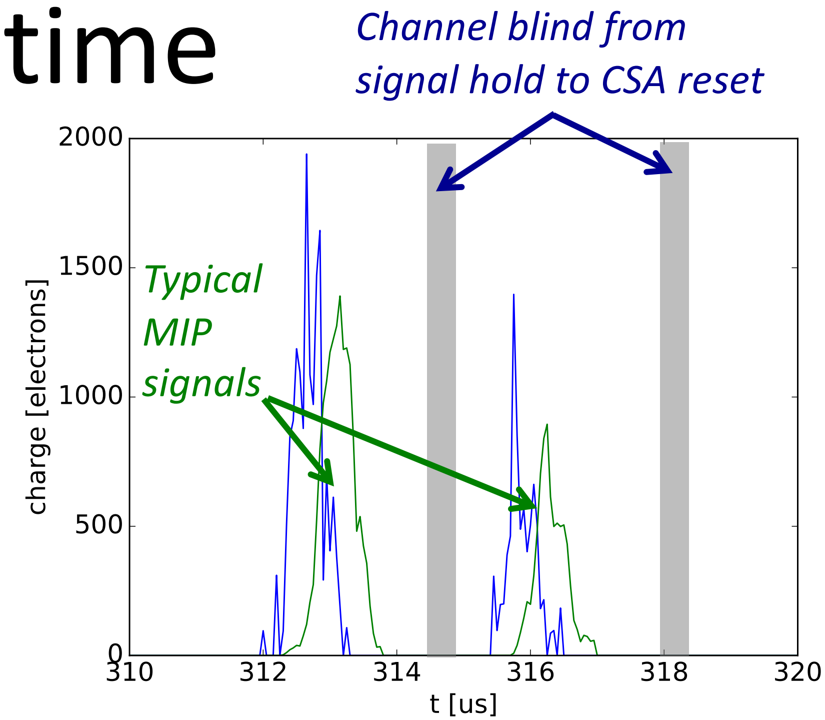
- Unlikely an issue for short MIP signals
- More concern for long signals

Requirements for LArPix-v2:

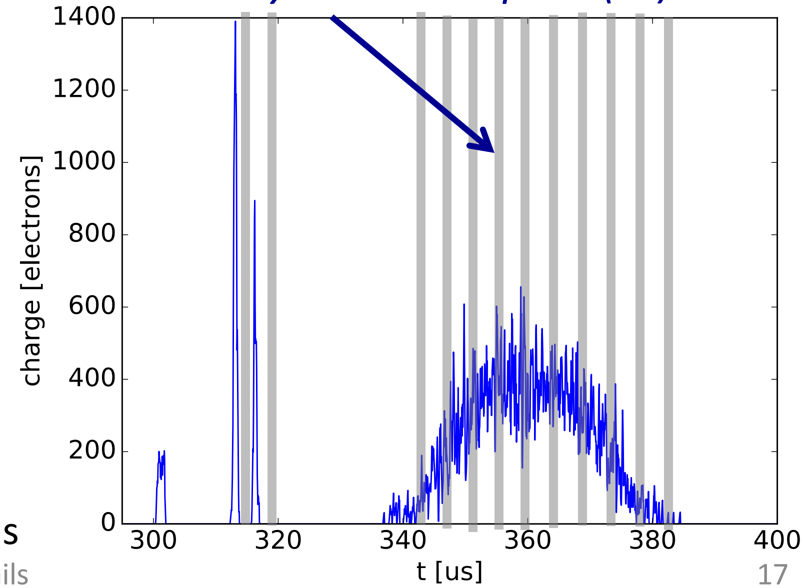
- Difficult to quantify with existing data. More simulations in progress.

Plan:

1) Reduce effect by decreasing time from signal hold to recovery from reset, and speed up buffer.
2) Add reset-suppressed (charge-integrating) modes to enable measurement of reset charge loss.
   fixed: ADC digitizes (dt=~2us) n-times before reset
   dynamic: ADC digitizes (dt=~2us) until ADC value settles



Multiple resets during long signal from track nearly normal to pixel (2^o).



Leakage Current

Leakage of charge onto front-end must be mitigated

Large leakage can lead to spurious triggers or increased uncertainty for charge measurement.

LArPix-v1 ASIC:

Observed leakage, no pixel attached

At room temp: ~80 fA (~500 e-/ms)

At LN/LAr temp: ~80 aA (~500 e-/s)

v1 Conclusion:

Enabling periodic resets at >50 Hz, leakage is negligible at LAr temp. (slightly annoying at room temp)

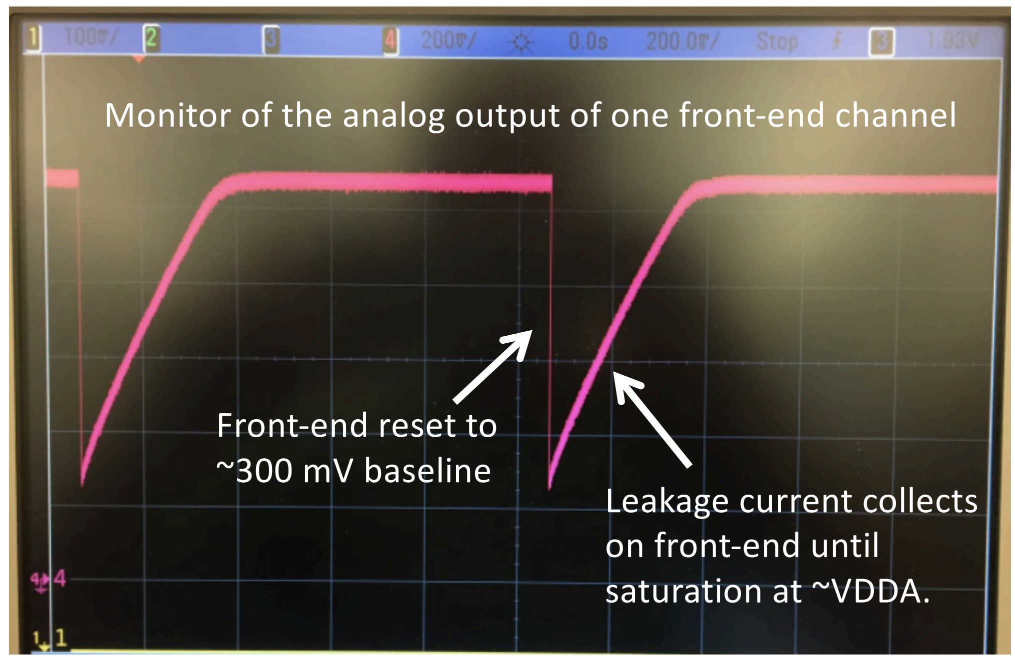
Also:

Occasional channels with high leakage after pixel PCB assembly.

Usually resolved by cleaning pixel PCB.

Example:

Channel with high leakage and 1 Hz periodic reset.



v2 Goal:

Don't substantially increase leakage from v1: ~80 aA in LAr.

Trigger Rate

LArPix concept relies on low trigger rate per pixel

Data rates:

- Data I/O for pixel tile saturates at ~10 kHz trigger rate per I/O link (MOSI/MISO pair).
- Assuming one I/O link per tile, 100 ASICs per pixel tile, 64 channels per ASIC:

  → *Physical Limit: ~1.5 Hz / channel*

- Expected data rates from true signals:

  Observed: LArPix-v1 @ Bern (on surface, 60cm-drift): *~0.3 Hz / channel*

  Expected: ArgonCube 2x2 Demonstrator:

  @ Bern (on surface, 30cm-drift): *~0.15 Hz / channel*

  @ FNAL (underground, 30cm-drift): *~0.01 Hz / channel*

Channel thresholds:

LArPix-v1:

Observed excess trigger rate (~1 Hz) at threshold of ~0.4 MIP. Insufficiently clean power?

Worse at Bern due to enhanced noise environment (lab above train station).

LArPix-v2:

Improving cleanliness of analog power with on-chip LDOs.

Improve ground plane on v2 pixel tile.

Power:

Data I/O a large part of digital power consumption. Hard to increase I/O link bandwidth at fixed power.

Some room to decrease digital voltage to reduce I/O power.

FIFO Depth

LArPix FIFO facilitates slow low-power off-chip data transmission

How large of a FIFO is required?

Lesson from LArPix-v1 @ Bern:

- FIFO depth: 2048 entries
- 32 channels per chip
- 16 chip daisy chain
- Average data rate, on surface, 60cm-drift: *~0.3 Hz / channel*

Observed:

FIFO half-full flags: 3 events over ~1 week of operation
FIFO full flags: 0

Estimate for LArPix-v2 in ArgonCube 2x2 Demonstrator:

- 64 channels per chip *→ x2 FIFO depth*
- Shorter drift length (~35cm instead of 60cm.) *→ x0.5 FIFO depth*
- Hydra I/O vs. Daisy Chain: *→ Signal-dependent. Simulation in progress.*

Rough Estimate:

Likely ok underground @ FNAL. Unclear about surface operation @ Bern.

v2: Implementing tunable I/O clock rate to allow trade-off in data rate vs. power

FIFO Depth

LArPix FIFO facilitates slow low-power off-chip data transmission

→ What about intense, long signal bursts on one channel, chip, pixel tile?

Scenario 1: Single channel fully active for one drift window

drift_velocity: 1.6 mm/us
drift_distance: 350 mm (for ArgonCube 2x2 Demonstrator)
drift_window = drift_distance / drift_velocity *→ ~220 us*
sample_time: 2.0 us
n_samples_per_channel = drift_window / sample_time *→ ~110 samples*

Scenario 2: All channels on chip maxed out during one drift window

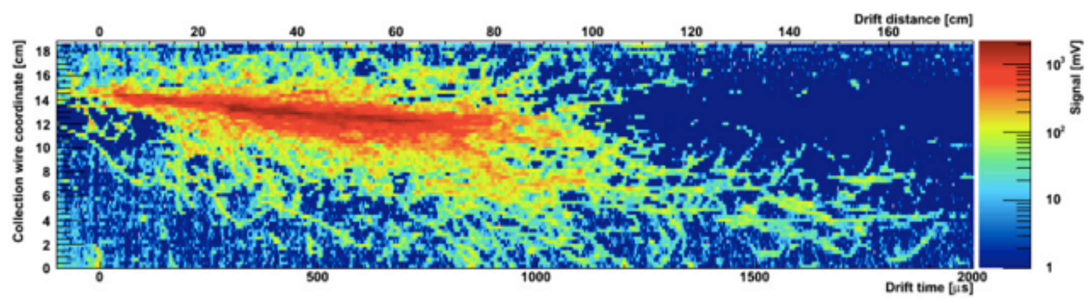
n_channels: 64 per chip
n_samples_per_chip = n_samples_per_channel * n_channels *→ 7,000 samples*

Neither scenario is very likely for MIP tracks.
More likely: MIP track is perpendicular to one chip region:
→ ~110 samples spread over a few (~8) of the channels on the chip.

Example intense cosmic shower from 5m ArgonTube LArTPC

Open question: Particle showers

- Simulation in progress
- v1 operation at Bern:
  No ‘FIFO full’ flags from cosmic showers.



Assembly and Operation

Many changes needed for assembly and operation of detector-scale system

Assembly:

→ Enable complete assembly of pixel tiles by commercial vendors

- Increase channel count: from 32 (v1) to 64 (v2)
- Increase default pixel spacing: from 3mm (v1) to 4mm (v2)
- Substantially reduce the number of SMT components: ~30/ASIC (v1) to ~few/ASIC (v2)
- Simplify chip attachment, rework: wirebond COB (v1) to QFP package (v2)
- Simplify PCB structure: two PCB sandwich (v1) to single PCB (v2)

Operation:

→ Pixel tile must continue to function, robust to arbitrary single-ASIC failures.

Example ASIC failure modes considered:

Chip D.O.A., excess current draw on power-up, excess noise generation on power-up, data I/O failure

Key v2 features:

- Hydra I/O
- ASIC subsection power disabled by default, manually enabled via digital control
- Extensive in-chip monitoring capabilities
- Enhanced test-pulse capabilities
- Protection against disabled pixel charge-up

Summary

Requirements for the LArPix-v2 ASIC design

Signal targets for the ArgonCube 2x2 Demonstrator:

- Cosmic Ray tracks and showers, operating on the surface in Bern
- NuMI neutrino beam interactions, operating underground at Fermilab

LArPix-v1 to v2 changes:

Primarily focused on aiding large-scale detector assembly and operation

- Robust I/O architecture
- Chip configurability to mitigate failure modes
- Increase channel count, use QFP packaging, minimize external circuitry and components

Maintain v1 physics performance, with some limited enhancements

- Reduce front-end deadtime, charge signal loss
- Enhance front-end test pulse system to improve channel characterization
- Larger timestamp to facilitate data synchronization