

**6th DUNE Near Detector Meeting.2019** DESY, Hamburg, October 22, 2019

Felix Sefkow **DESY** 















Calorimeter prototypes for future e+e- colliders

**Production procedures** 

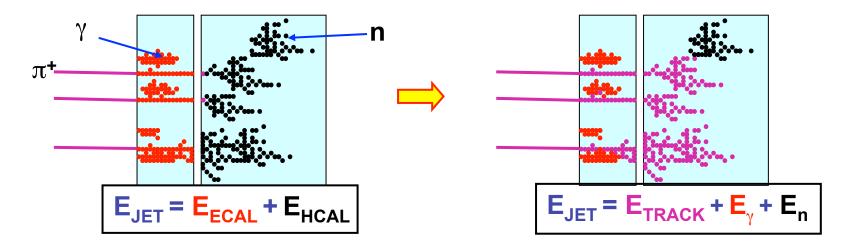
**Electronics directions** 

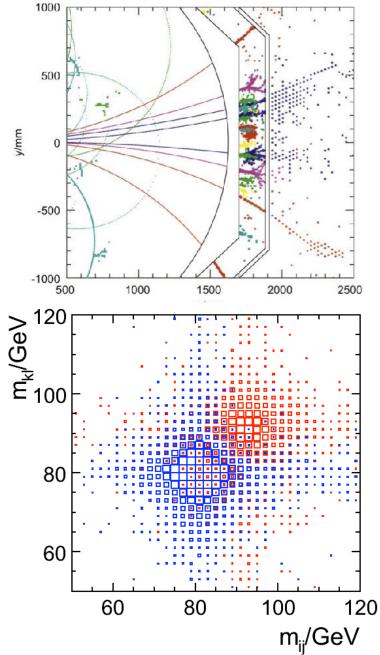
## Prototyping Experience for an e+e- Detector

## **Particle Flow Paradigm**

Tackle the jet energy challenge.

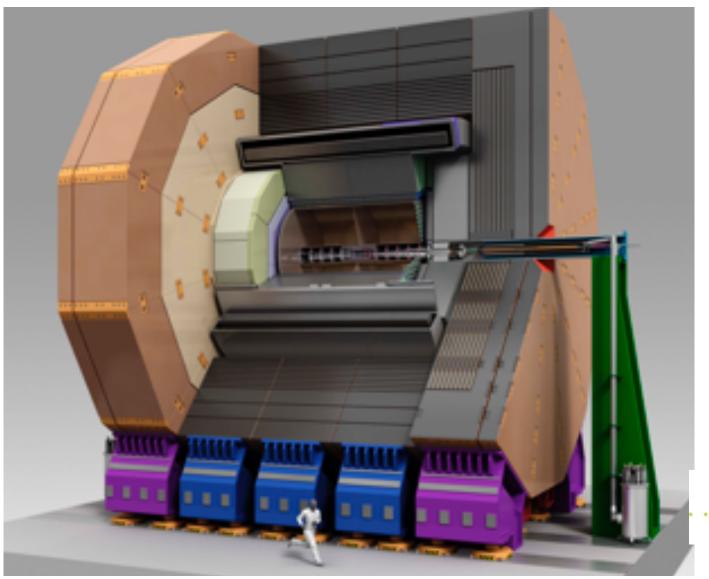
Reconstruct each particle individually and use optimal detector Requires fine 3D segmentation of and sophisticated software Today all linear collider detector concepts follow particle flow concept

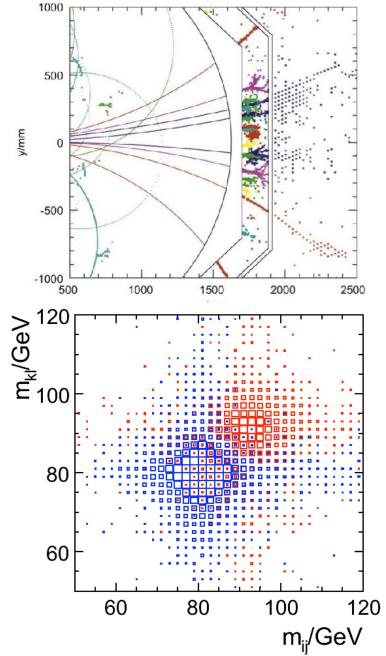




## **Particle Flow Paradigm**

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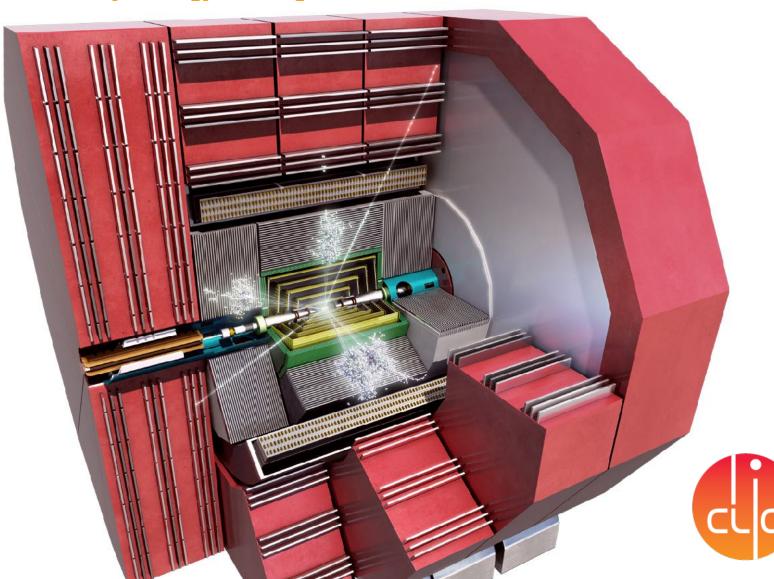


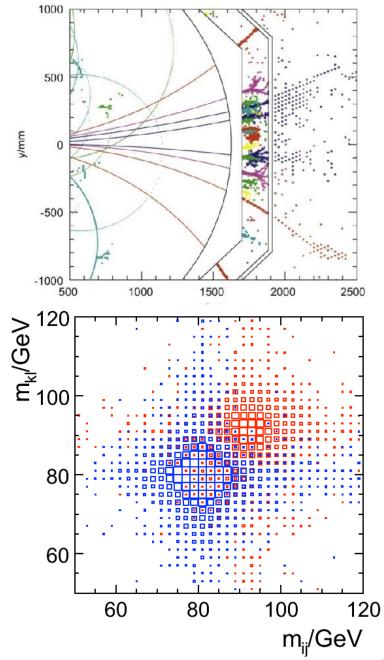


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## **Particle Flow Paradigm**

Tackle the jet energy challenge.





## **Technologies for Highly Granular Calorimeters**

Because we can.

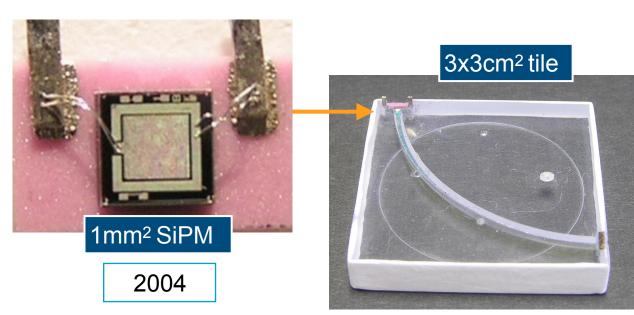
#### Large area silicon arrays

silicon calorimetry grows out of the domain of small plug devices

New segmented gas amplification structures (RPC, GEM,  $\mu$ Ms) Silicon photomultipliers on scintillator tiles or strips



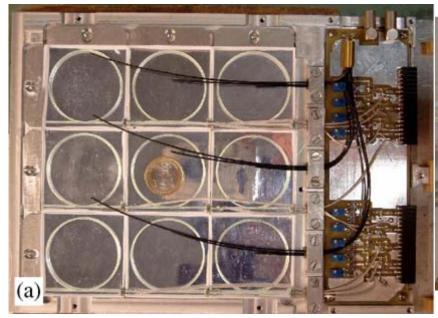




small, B-insensitive, cheap, robust

## **SiPM-on-Tile Evolution**

A long way

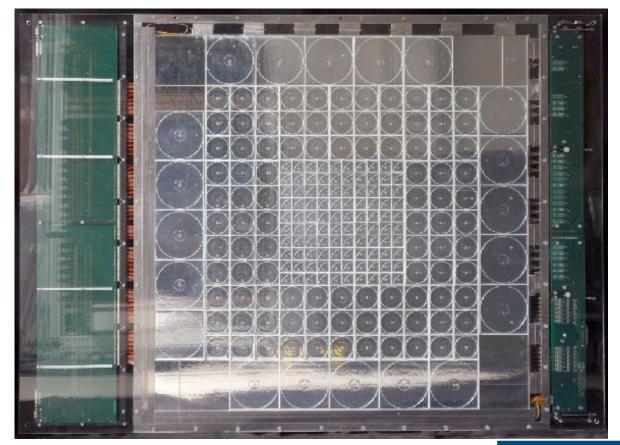


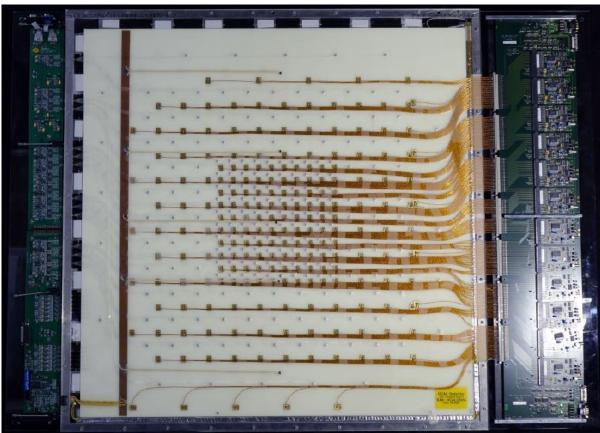


2003: MiniCal

## **SiPM-on-Tile Evolution**

A long way

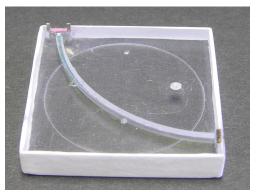


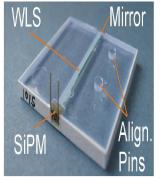


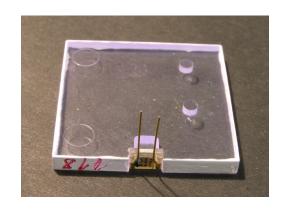
2006: Physics Prototype

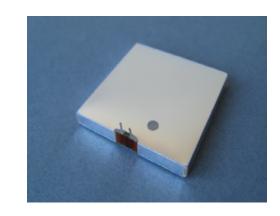
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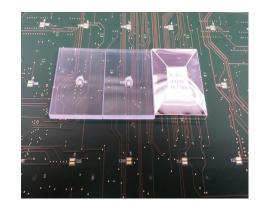
A long way





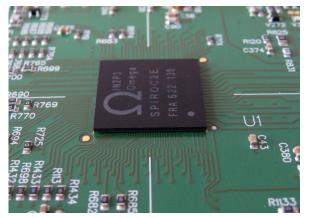


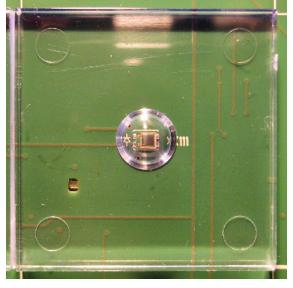




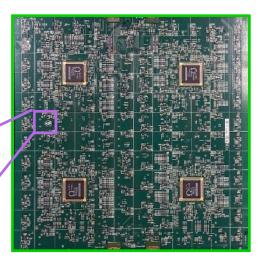
## The Next Step: Scalability

**Technological prototypes.** 

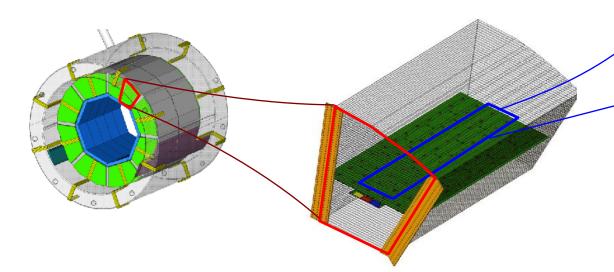








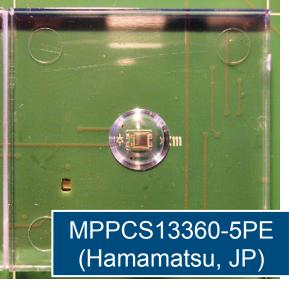
- 1000's of channels per m<sup>2</sup>
- 1000's of m<sup>2</sup>
- must embed electronics and go digital as early as possible; power pulsing
- Integrate SiPMs in read-out board, too



## The Next Step: Scalability

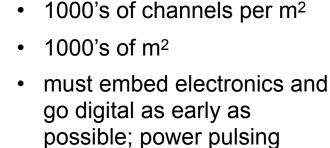
Technological prototypes.



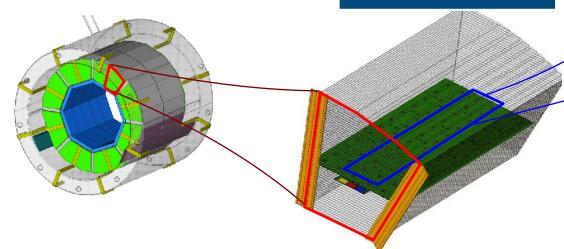


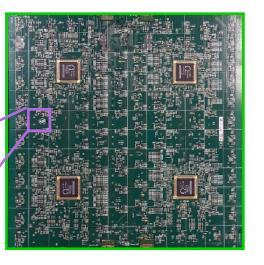


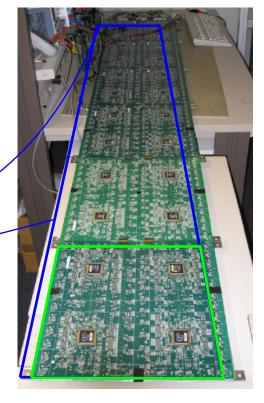
polystyrene tiles (Uniplast, RU) with ESR film



 Integrate SiPMs in read-out board, too





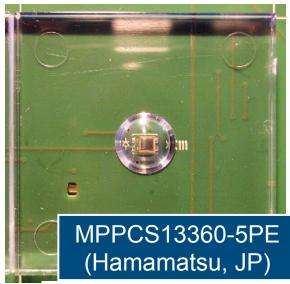


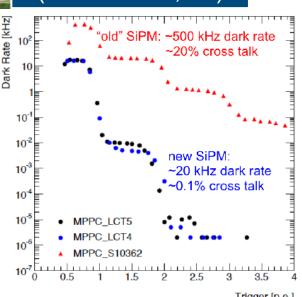
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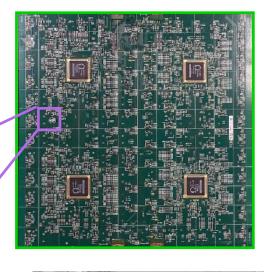
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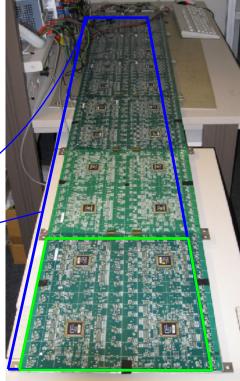






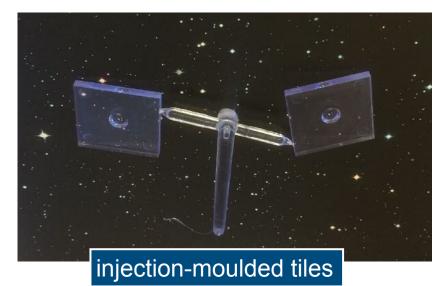
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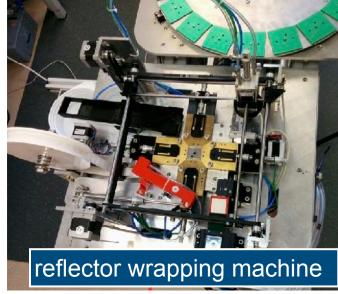


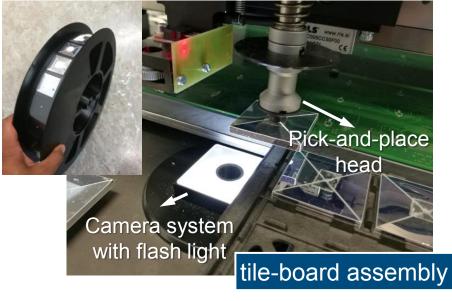


## **Automated Production and Quality Assurance**

**Establishing the concept.** 





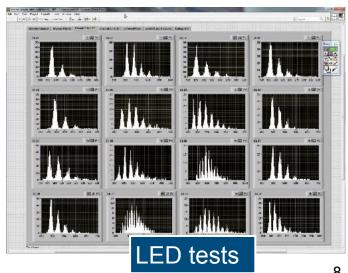


#### In addition test infrastructures:

- Multi-channel SiPM tests
- Automated ASIC tests
- PCB tests using LEDs
- Coscmic tests after tile assembly



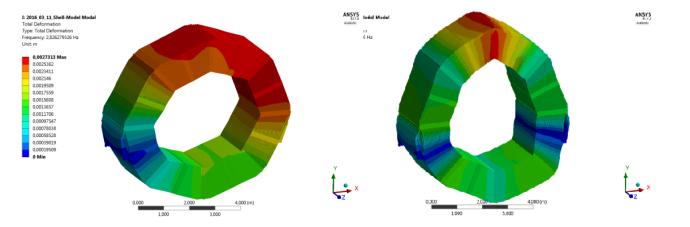




Prototyped.

#### Stack services dimensioned for full collider detector

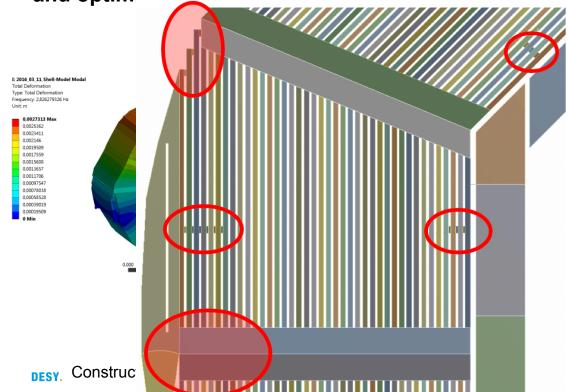
- Data concentration
- Power distribution
- Cooling



Prototyped.

#### Stack services dimensioned for full collider detector

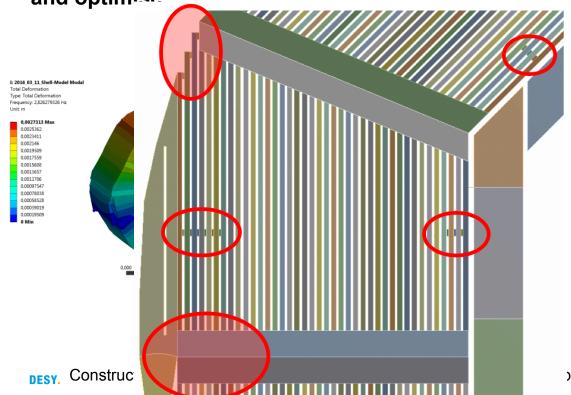
- Data concentration
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- Cooling

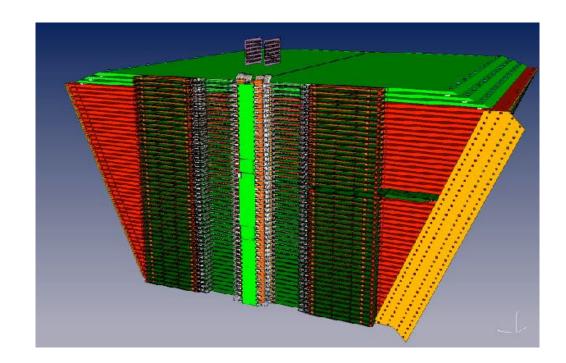


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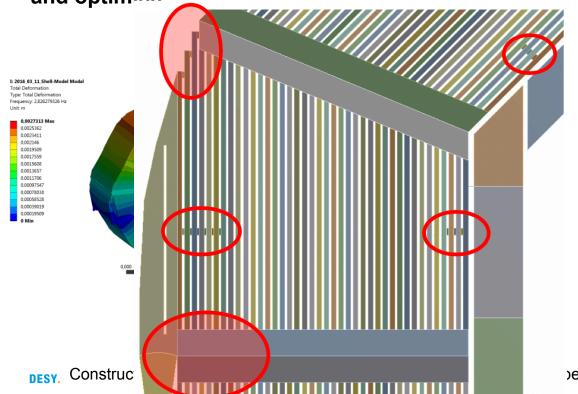


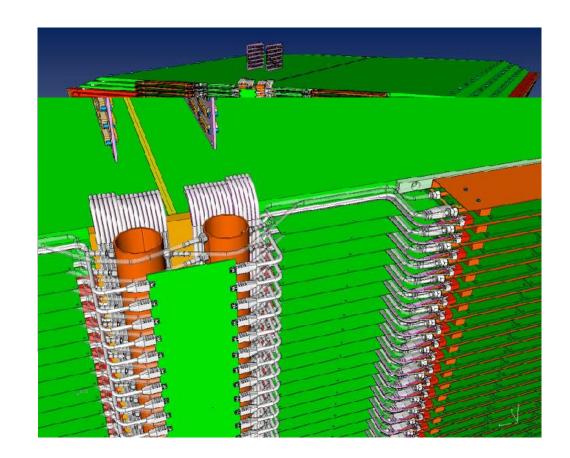


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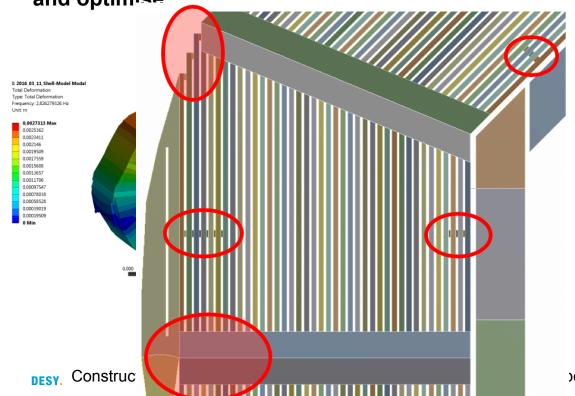




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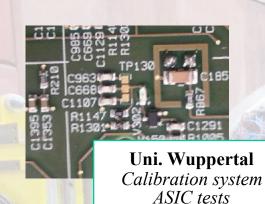
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## **AHCAL** technological prototype



Uni. Mainz
DAQ, assembly
Cosmic test stand

MPI Munich
Mechanics (cassettes),
SiPM tests

**Prague** DAQ

Strong contribution from different international & German institutes

#### **DESY**

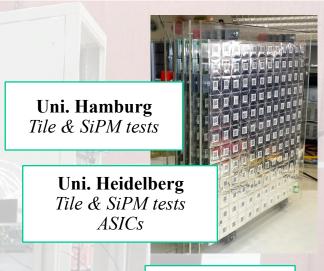
Electronics & mechanics design Commissioning Testbeam software Testbeam coordination

All institutes

Analysis of data

**R&D contribution from additional partners** 

Shinshu Uni, Tokyo Uni (Japan) JINR, Dubna, MEPHI (Moscow) UT Arlington, Northern Illinois Uni (USA)



Uni. Sussex
Monitoring

**Lebedev I** *Tile production* 

Omega (IN2P3)

ASICs

#### **CERN**

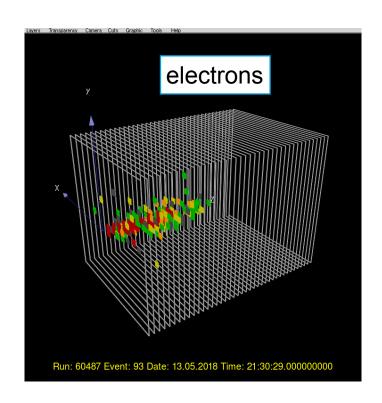
Tungsten structure, test beam, logistics

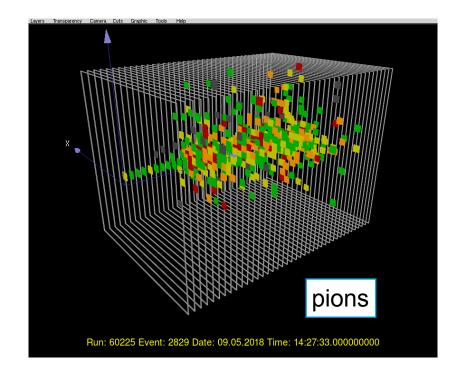


## **Electrons and Hadrons**

#### **Mixed Beams**

- Electron data 10 100 GeV
- Hadron data 10 160 GeV

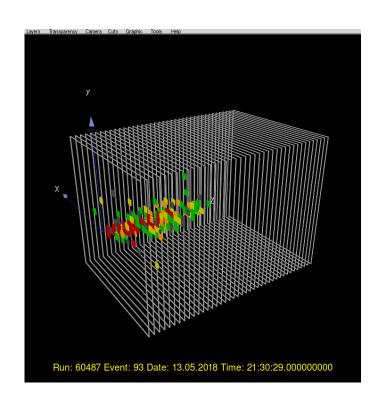


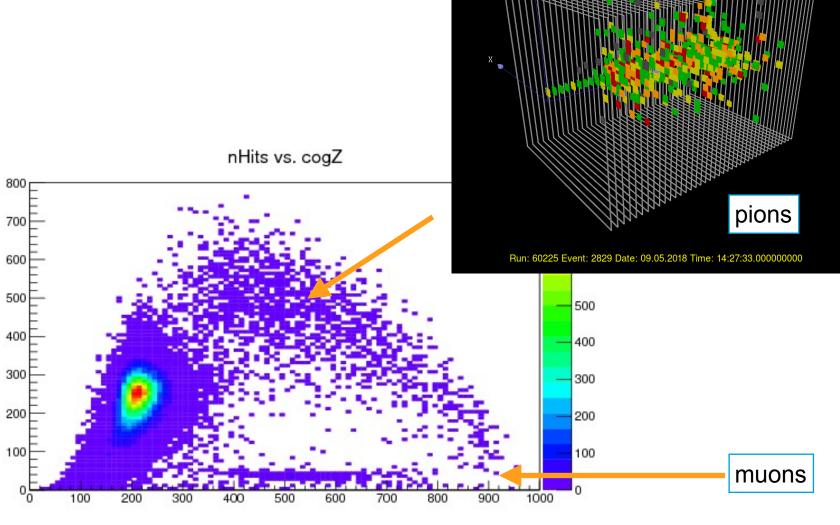


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#### **Mixed Beams**

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## **Temperature compensation**

Online - Used routinely throughout 2018

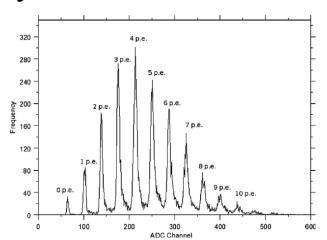
## SiPM parameters (almost all) depend on over-voltage

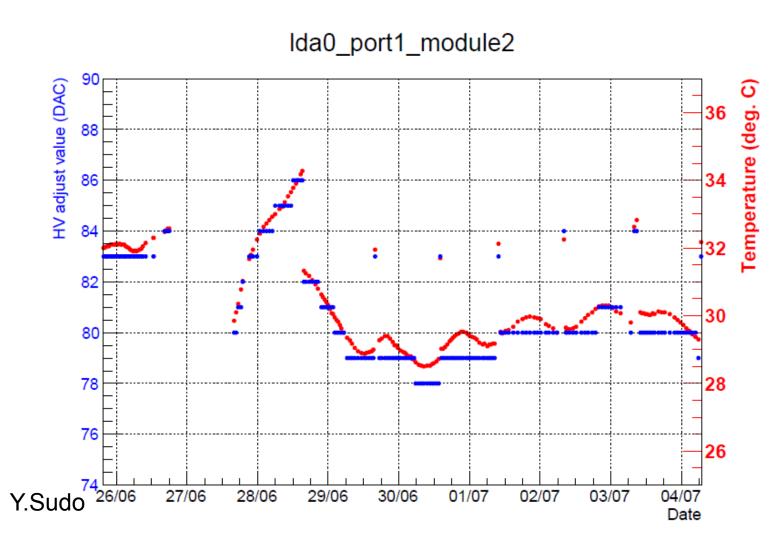
 $\Delta V = V_{\text{bias}} - V_{\text{breakdown}}(T)$ 

V<sub>breaddown</sub> depends on temperature, very uniformly

Adjust  $V_{bias}(T)$  to stabilise  $\Delta V$ 

Use gain (from single photoelectron peak spacing to monitor stability





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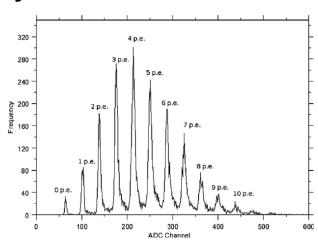
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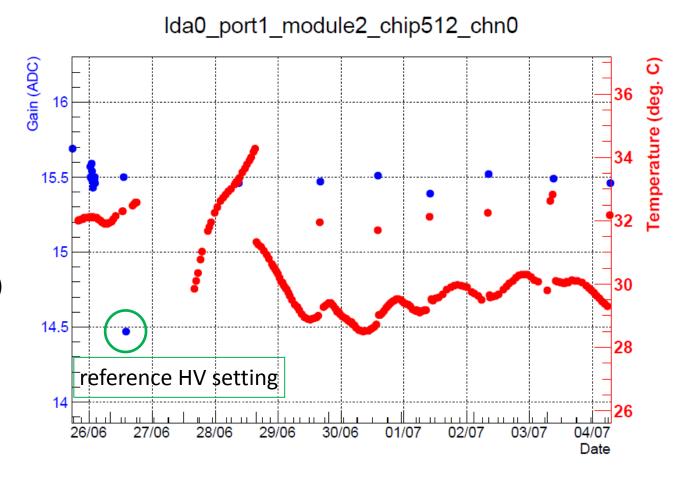
V<sub>breaddown</sub> depends on temperature, very uniformly

Adjust  $V_{bias}(T)$  to stabilise  $\Delta V$ 

Use gain (from single photoelectron peak spacing to monitor stability



no HV adjust (same setting as the last configuration)



Y.Sudo

# Construction Techniques for the CMS Upgrade



## **HGCAL** Overview

#### **Key Parameters (updated from the TDR):**

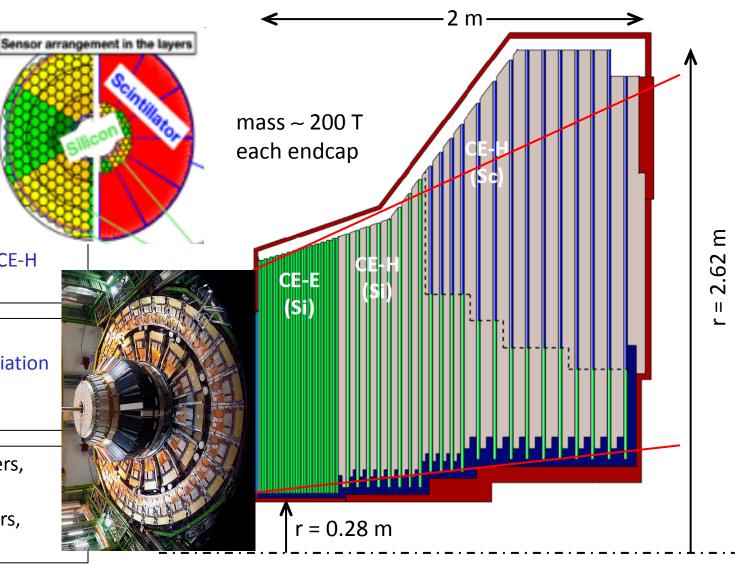
- HGCAL covers  $1.5 < \eta < 3.0$
- Full system maintained at -30°C
- ~640 m² of silicon sensors
- ~370 m<sup>2</sup> of scintillators
- 6.1M Si channels, 0.5 or 1.1 cm<sup>2</sup> cell size (6M) 240k scint-tile channels  $(\eta \phi)$ 
  - Data readout from all layers
  - Trigger readout from alternate layers in CE-E and all in CE-H
- ~31000 Si modules (incl. spares)

#### **Active Elements:**

- Si sensors (full and partial hexagons) in CE-E and high-radiation region of CE-H.
- SiPM-on-Scintillating tiles in low-radiation region of CE-H

Electromagnetic calorimeter (**CE-E**): **Si**, Cu/CuW/Pb absorbers, 28 layers, 25.5  $X_0$  & ~1.7 $\lambda$ 

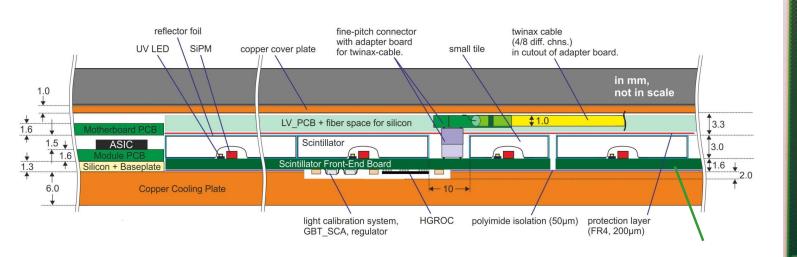
Hadronic calorimeter (**CE-H**): **Si** & **scintillator**, steel absorbers, 22 layers,  $\sim$ 9.5 $\lambda$  (including CE-E)

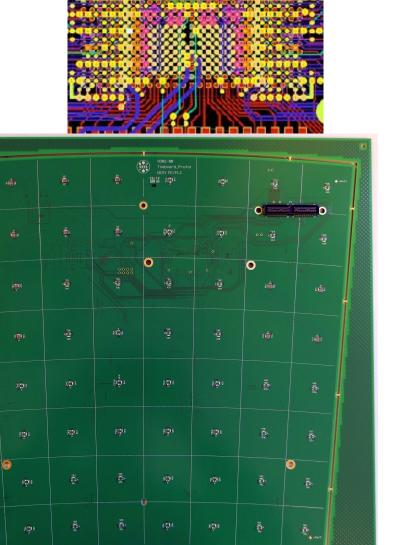


### **Tileboard**

#### **Prototyping**

Prototype TB-1 produced last week
64 SiPMs, HGCROC ASIC, DCDC converters, LEDs
Complex layout, HGCROC in 0.6mm pitch BGA package
Thermal vias for SiPM cooling
Test environment in preparation

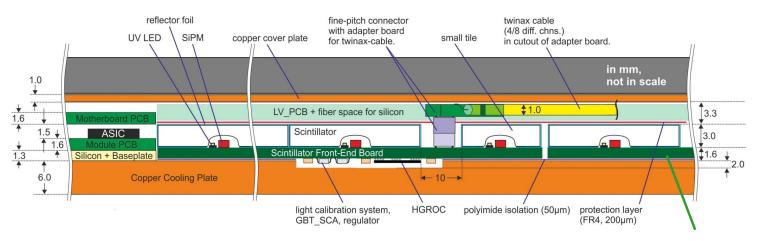


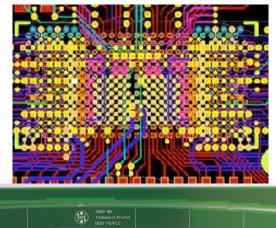


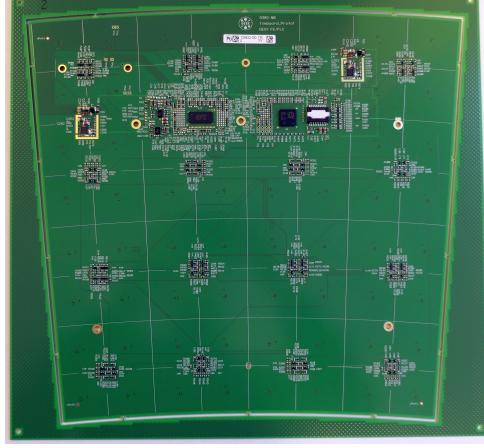
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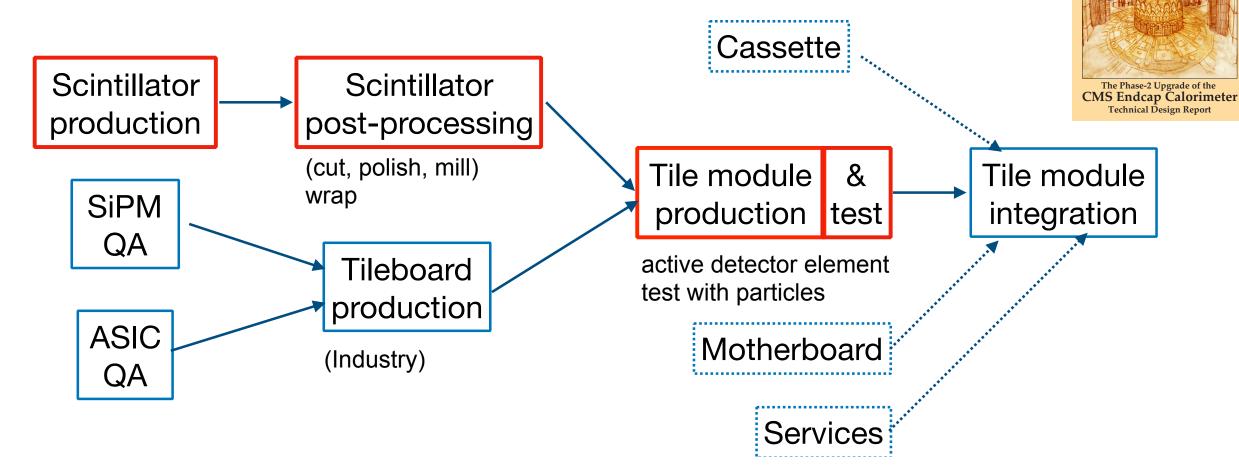






## Tile Module Assembly Flow Diagram

**Production and QC** 



Quality assurance and quality control after each step

## **Foil Cutting Alternative**

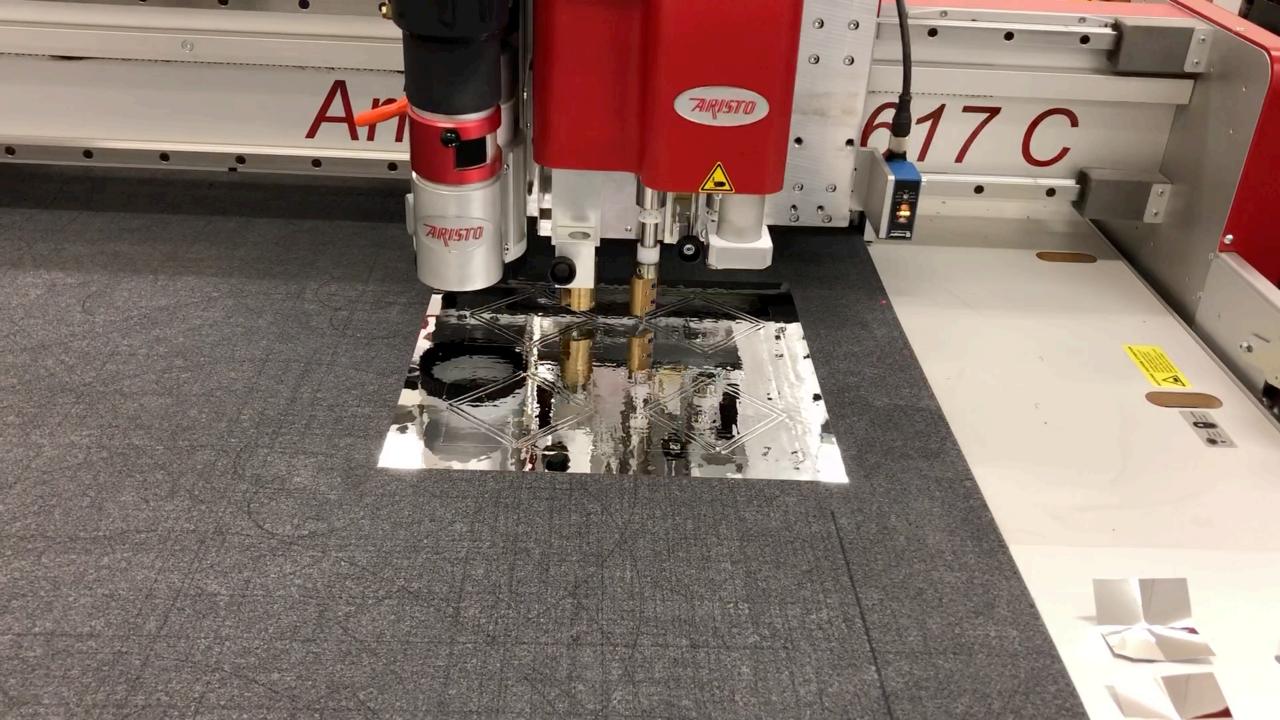
To replace laser cutter

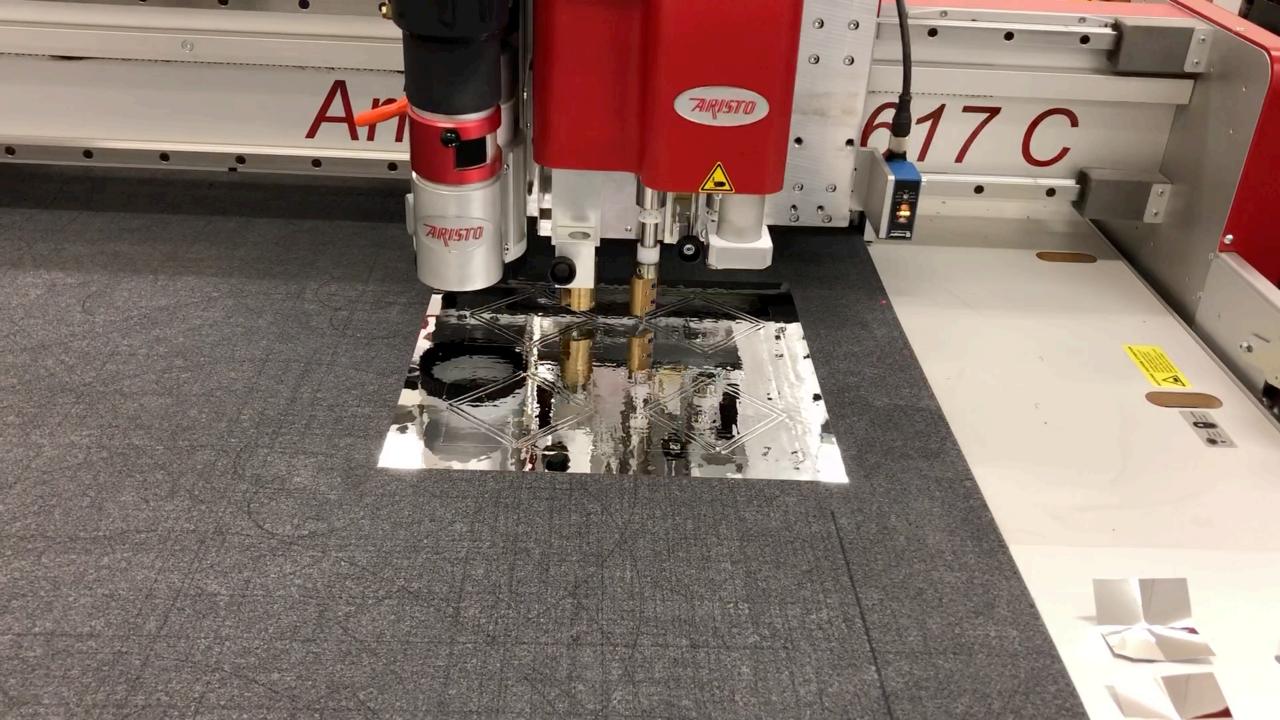


## Computer-controlled creasing wheel and knife easy to program: reads drawings in dxf format Reproducibility (spec) 0.02 mm



O. Bach, DESY



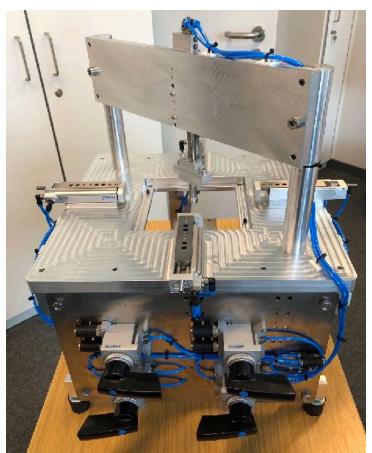


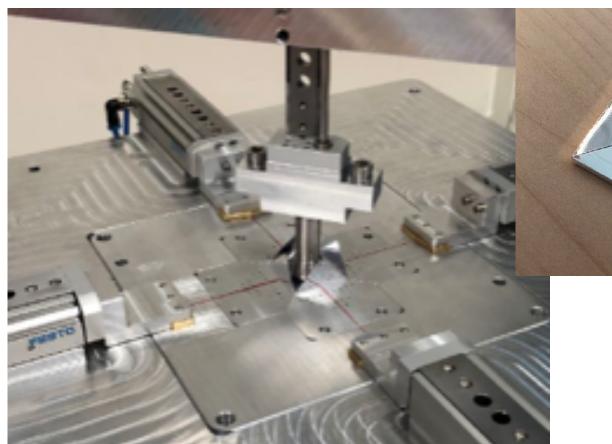
## **Tile Wrapping Tool**

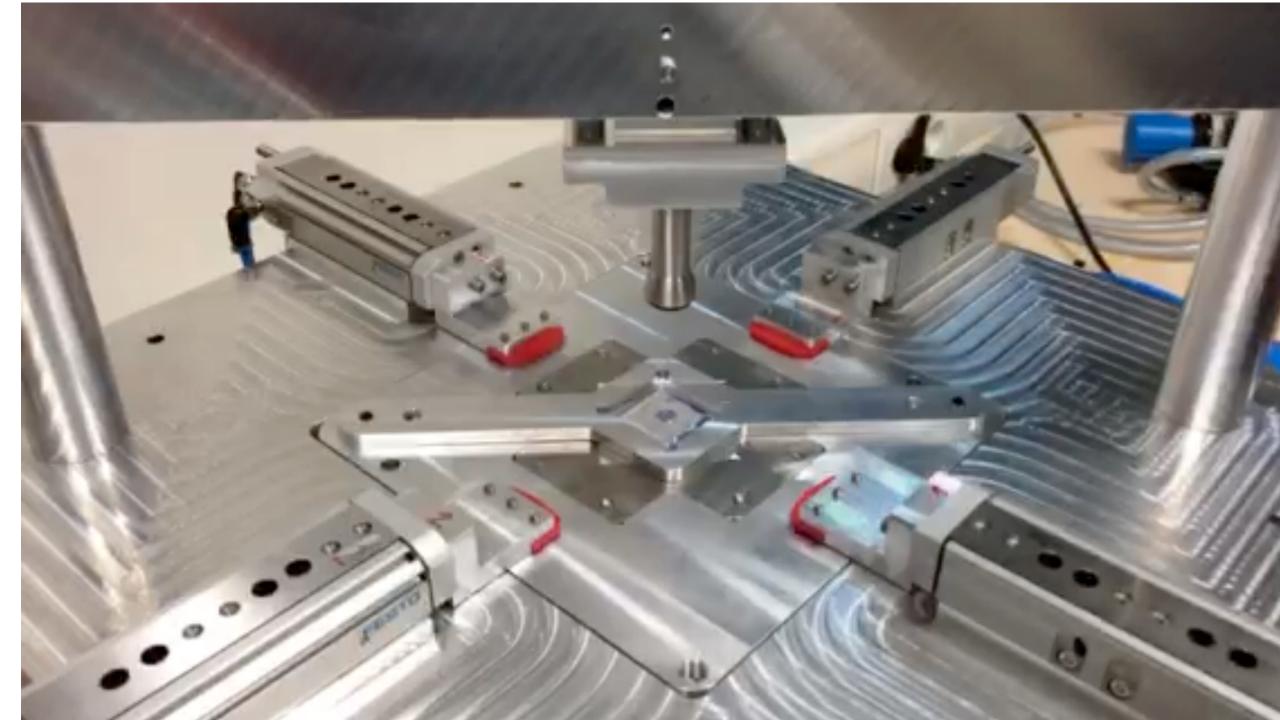
**Ongoing work: DESY** 

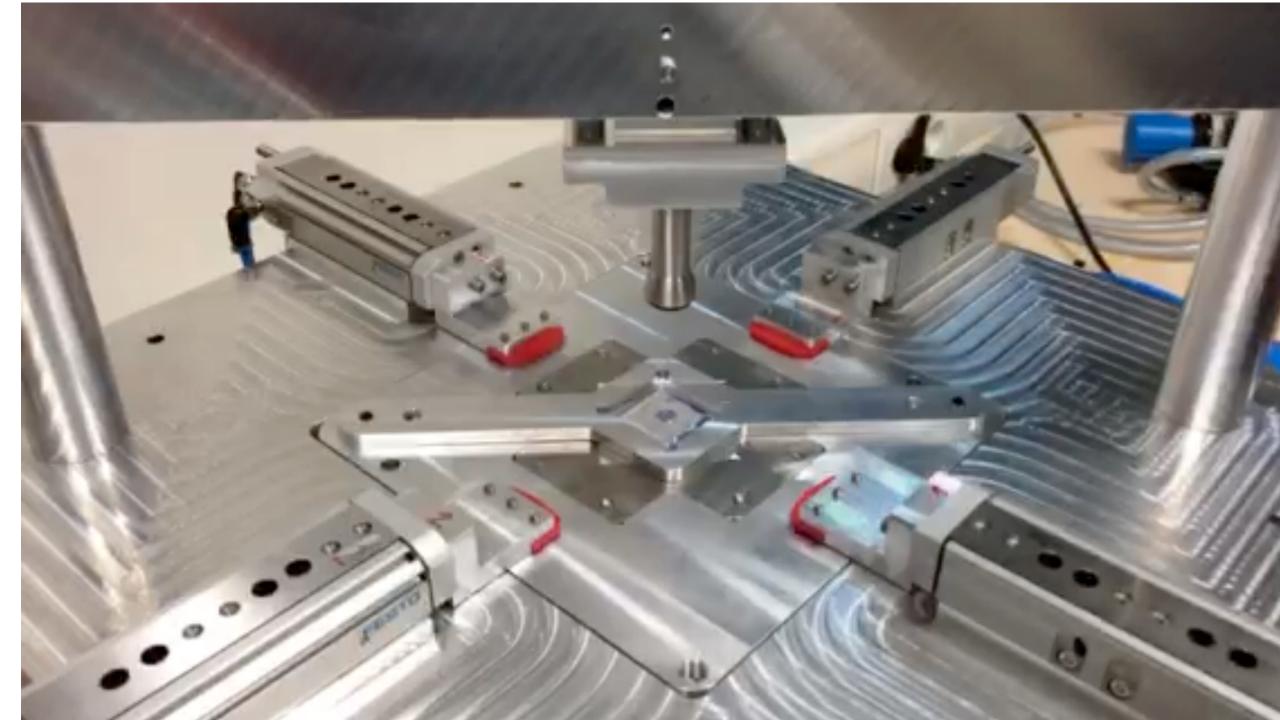
#### Machine built, first tests done

Commercial pneumatic actuators, rest built in-house









## **Wrapping Machine Status**

As of Today

Folienvorrat

# Central part ready, feeders in production

expected for mid October

#### **Size-dependent parts**

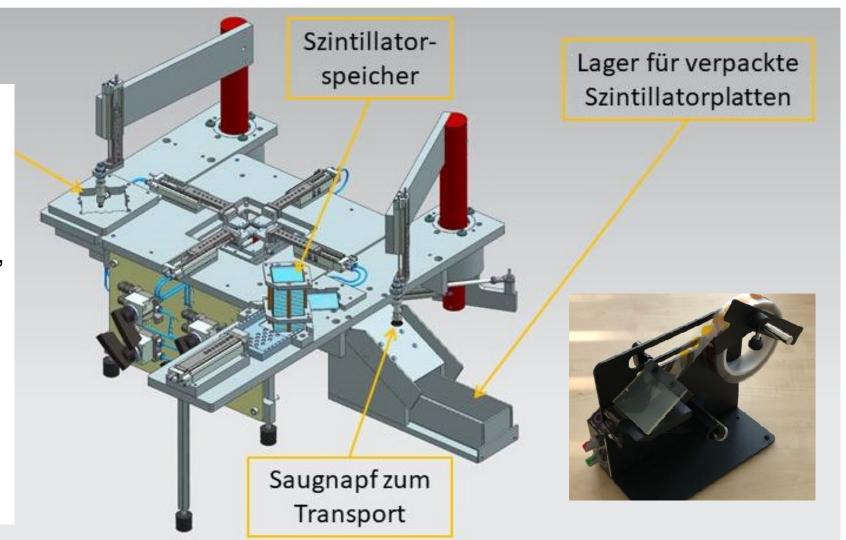
existing for square CALICE tiles, used for assembly tests

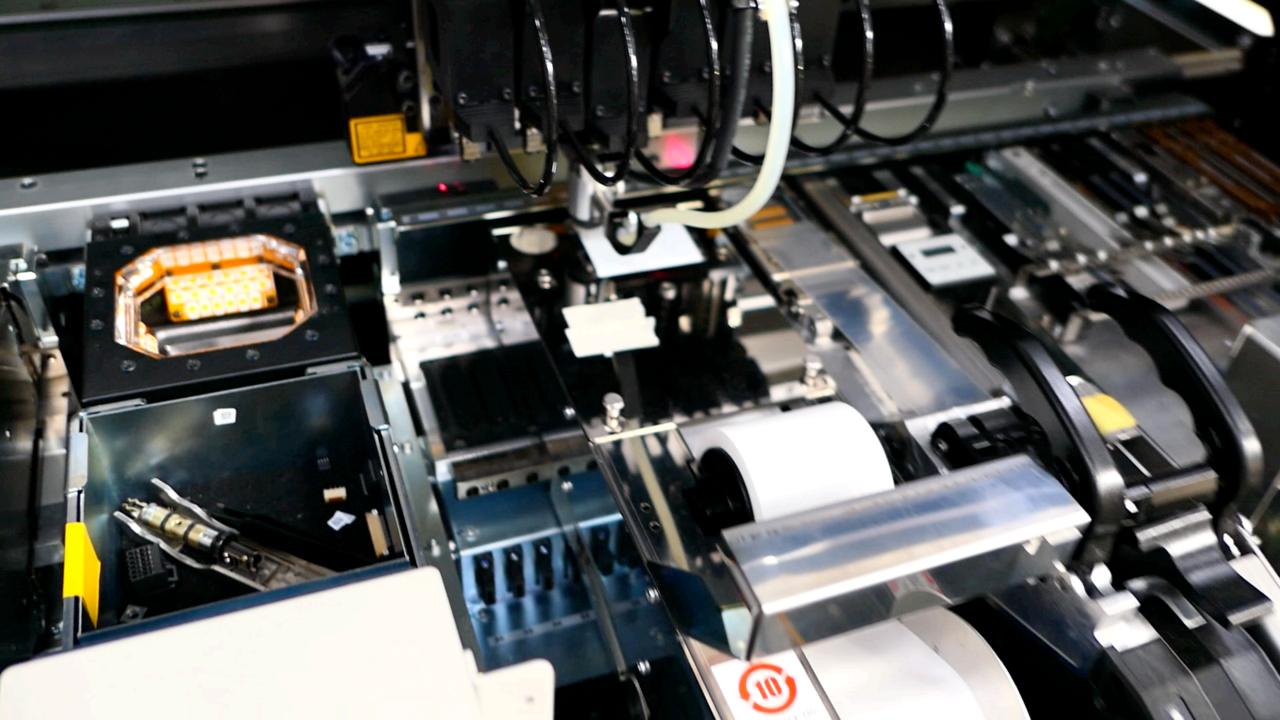
ready for the 4 sizes of Tileboard-1

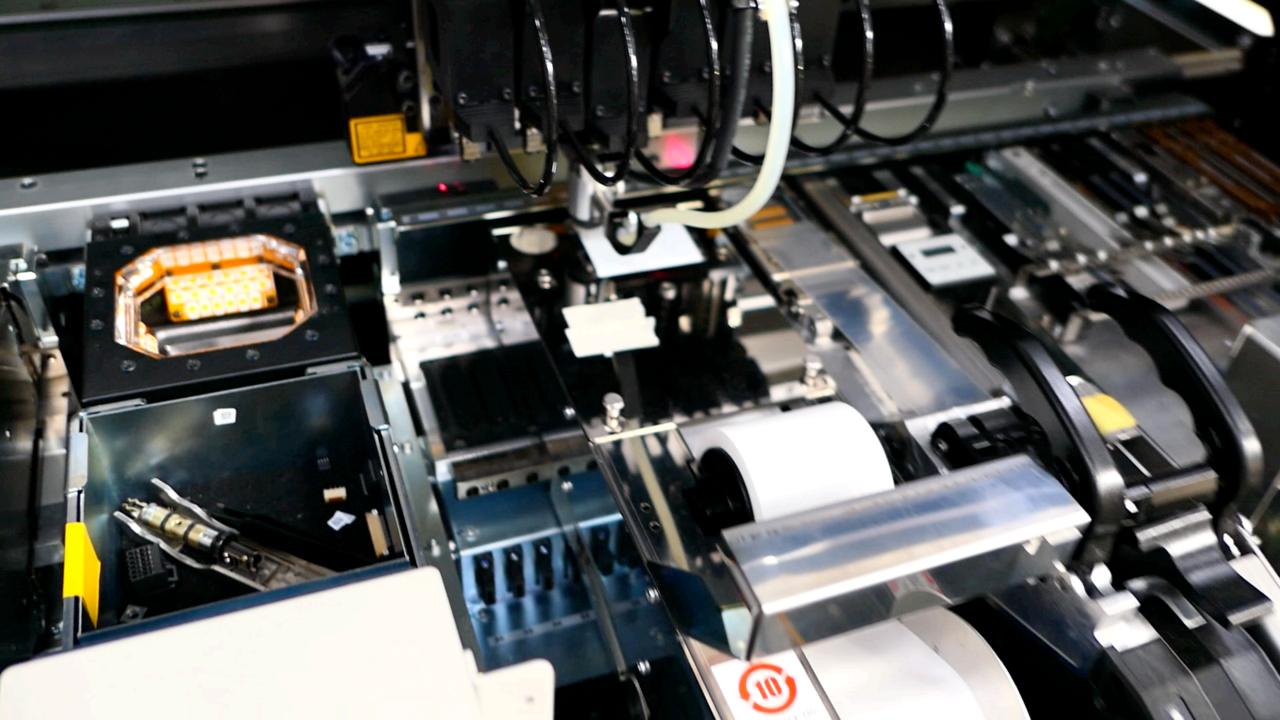
#### Figures:

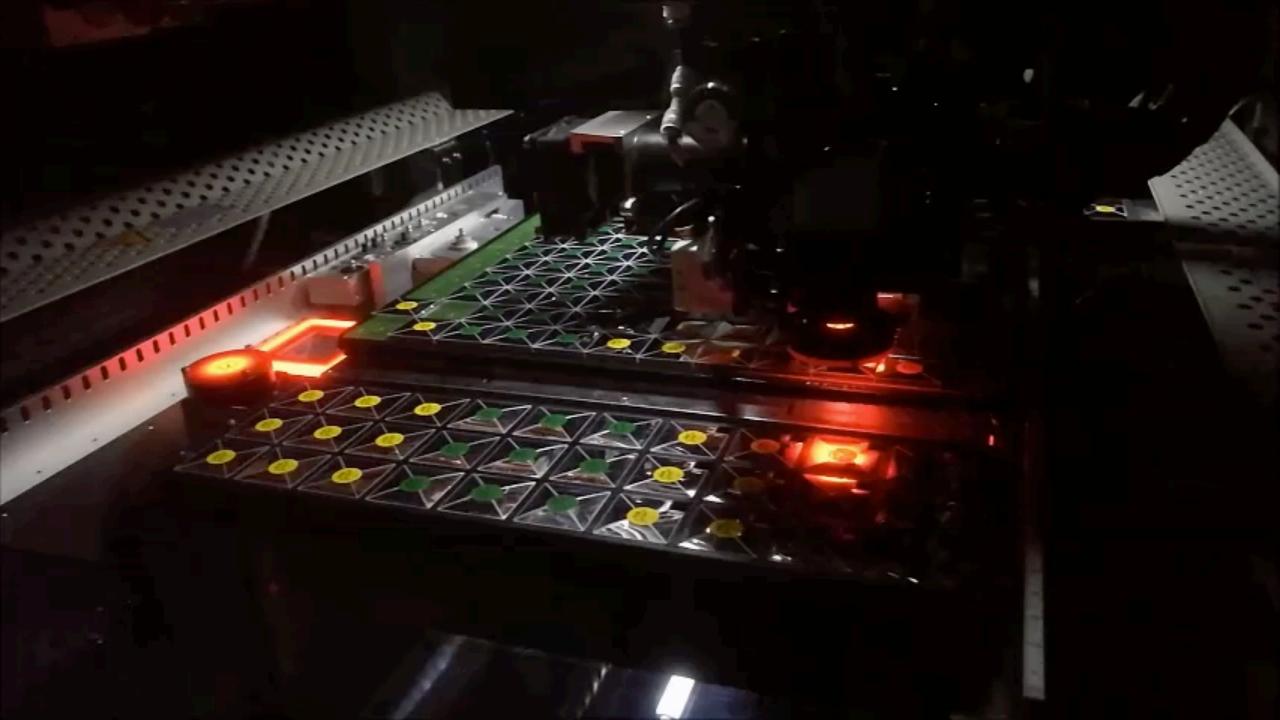
Cost: 8k + 160 hrs w/s time

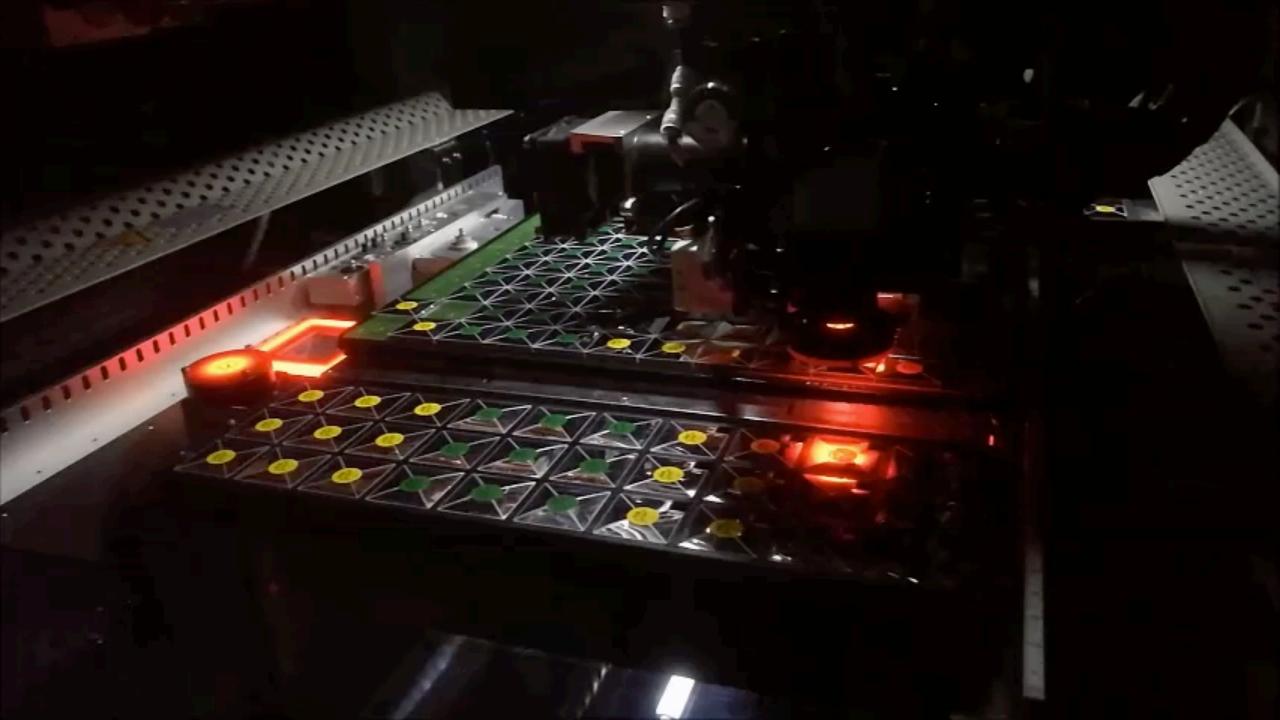
Speed: 3-4 tiles / min







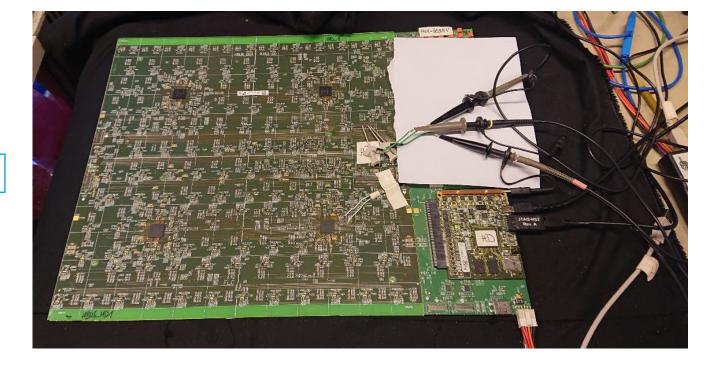




# **Electronics Developments**

### Status Commissioning HBU6\_HD

- New child in HBU family: HBU6\_HD with KLauS ASICs (cooperation Uni-Heidelberg, DESY)
- > Two HBU6\_HDs with KLauS5 ASICs, 4 new POWER4 boards completed.
- > First commissioning at DESY Sept. 2019: Zhenxiong, Mathias.



KLAUS ASIC:
optimised input stage
for SiPMs with smaller
gain, larger dynamic
range
continued read-out
timing

see Wei Shen's talk





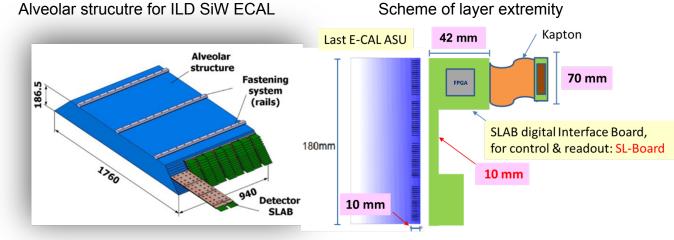


#### **CALICE SiW ECAL- Rationalisation/Miniaturisation of components**



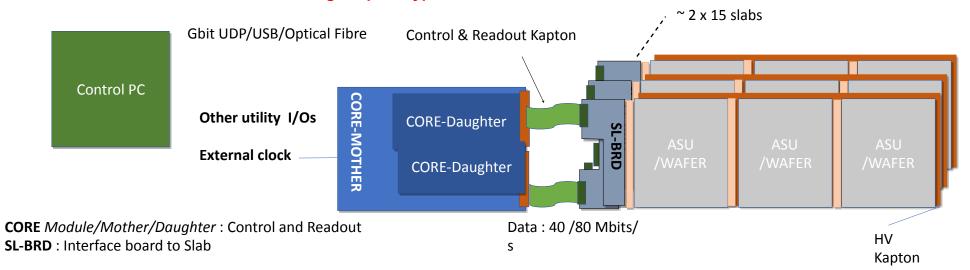
#### Constraints for the Slab Interface Board (SL-Board)

- The SI-board will be installed between ECAL and HCAL, separated by only 67 mm
- L-shape because of the cooling system
- Maximum Height : 6 to 12 mm depending on the location
- Control & Readout electronics at the extremity of the Slab
- Signal Integrity over a Slab : up to 15 interconnected ASUs
- Very low Power consumption (~ 150 mA/ Slab): needs to run in power pulsing mode



... similar to DUNE Structure

#### Readout scheme of CALICE SiW ECAL technological prototype



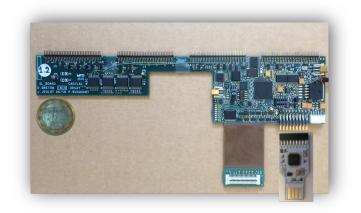
Maalmi/Jeglot/Breton

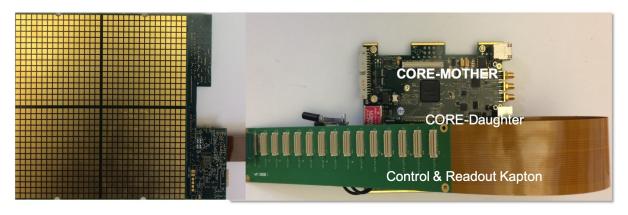


#### **CALICE SiW ECAL-** Rationalisation/Miniaturisation of components



#### SL-Board for up to 10000 cells and connection to concentrator unit via flat kapton cable





Service for up to 15 layers

#### Elegant space economic solution

Seamless operation in DESY beam test 2019

2019: One flat cable leaving the detector



< 2019: "Jungle" of bulky cables



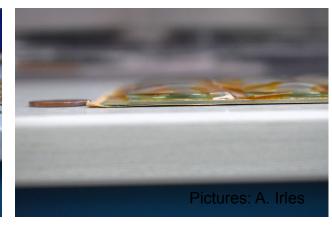
### Rationalisation/Miniaturisation of components



#### Thin PCB for compact detector solutions

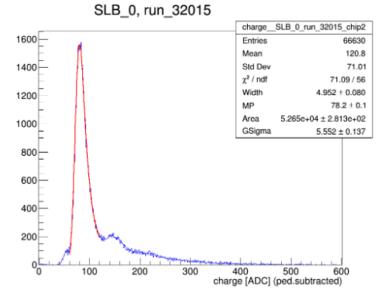








- Height 1.2mm (for a 9 layer board!!!)
- Challenges in terms of planarity
- · were overcome in
- · close collaboration with Korean Company
- First beam test 2019 at DESY



VCI 2019



#### **Rationalisation/Miniaturisation of components - Conclusions**



- "Dead space free" granular calorimeters put tight demands on compactness
- Current developments within CALICE for SiECAL meet these requirements
- Can be applied/adapted wherever compactness is mandatory
- Components will/did already go through scrutiny phase in beam tests

#### Summary no Outlook

SiPMs are a mature technology meanwhile

SiPM-tile integration concepts suitable for large systems developed for e+e- colliders

Now being applied to CMS: production techniques for 240'000 channels

Electronics for compact ECAL designs and continuous readout under development

Established network of institutes and task sharing

# Back-up