The research leading to these results has received funding from the European Union Seventh Framework Programme [FP7/2007-2013] under Grant Agreement n256984 (EndoTOFPET-US) and n289355 (PicoSEC)

SiPM readout ASIC @KIP Heidelberg

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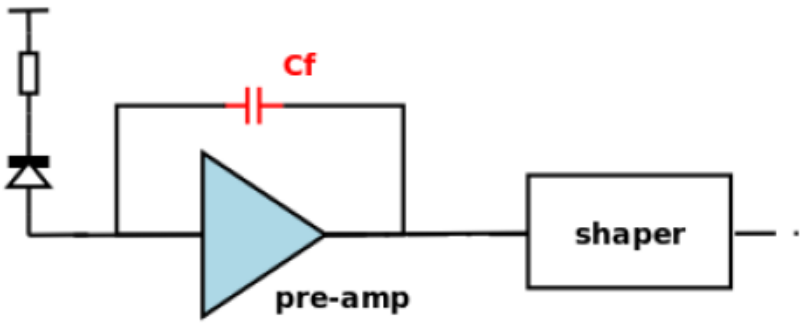
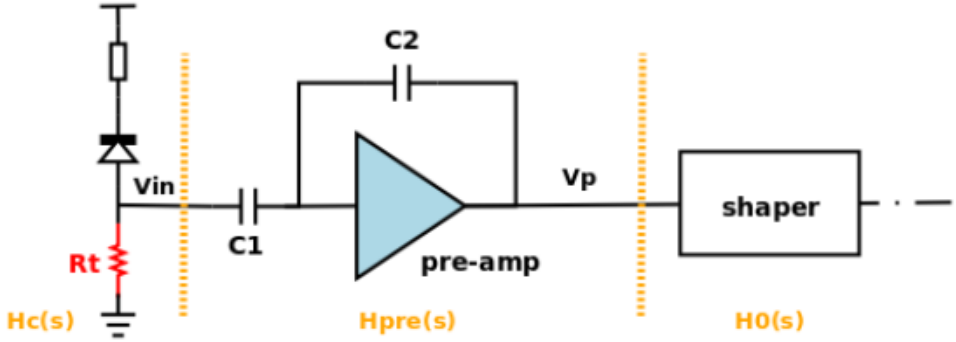
Outline

- SiPM readout Topologies
- SiPM readout ASICs developed in HD

Topologies for SiPM readout

- the traditional readout structure for PiN or APD detectors do not fit for SiPM, reasons:





1. much too high gain of SiPMs
2. the reruested SNR of SiPM is effectively higher (suprise!!)
3. due to the large gain and high detector capacitance, the bandwith request from SiPM is much higher

CHIPs using this structure : VATA series (IDEAS) , SPIROC (WeeROC)

the existing topologies for SiPM readout

- current based

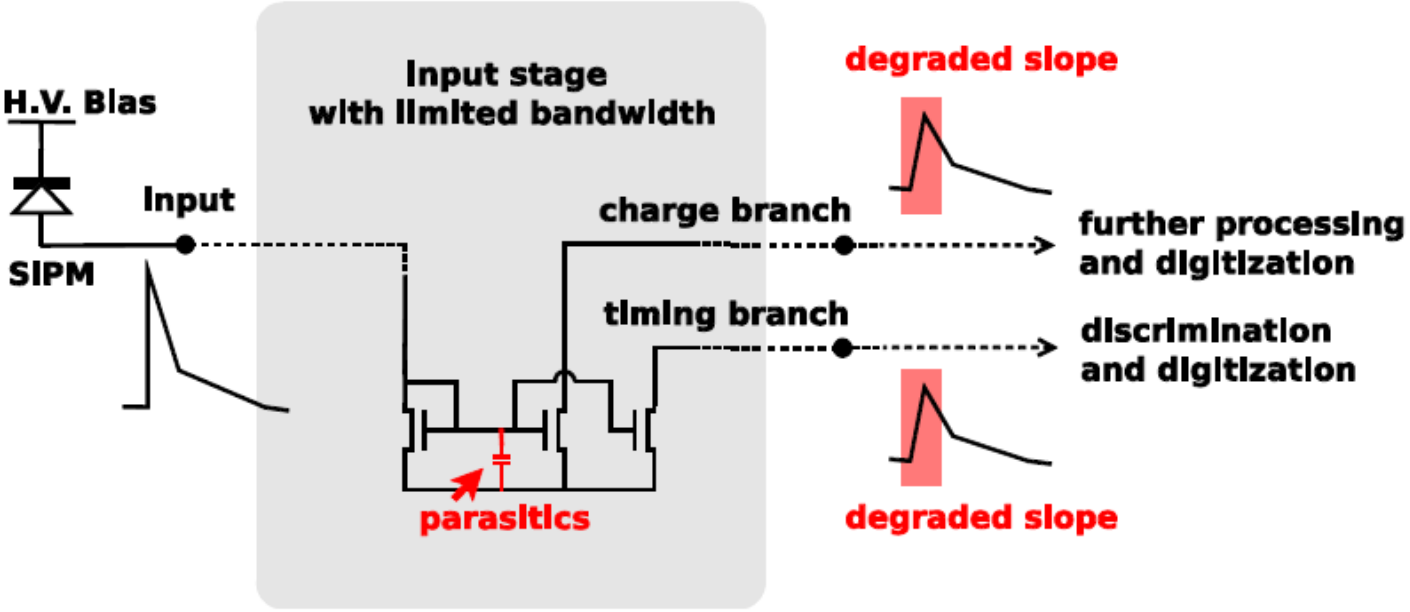
ToFPET ASIC (PETsys), PETIROC (WeeROC),
BASIC (INFN), FlexToT (Barcelona), PASIFIC (LHCb),
KLauS (KIP, HD), PETA (ZITI, HD), EXYT(清华), ……

- Time based

NINO (CERN), STiC (KIP, HD)

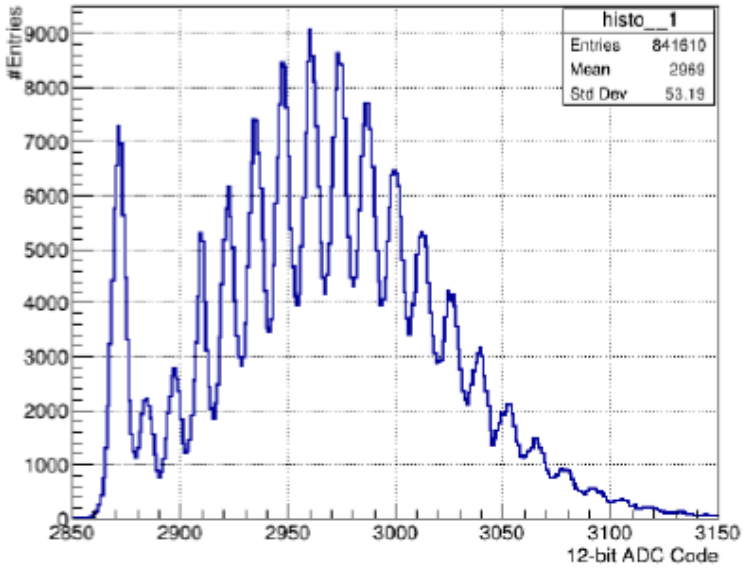
Current based topology

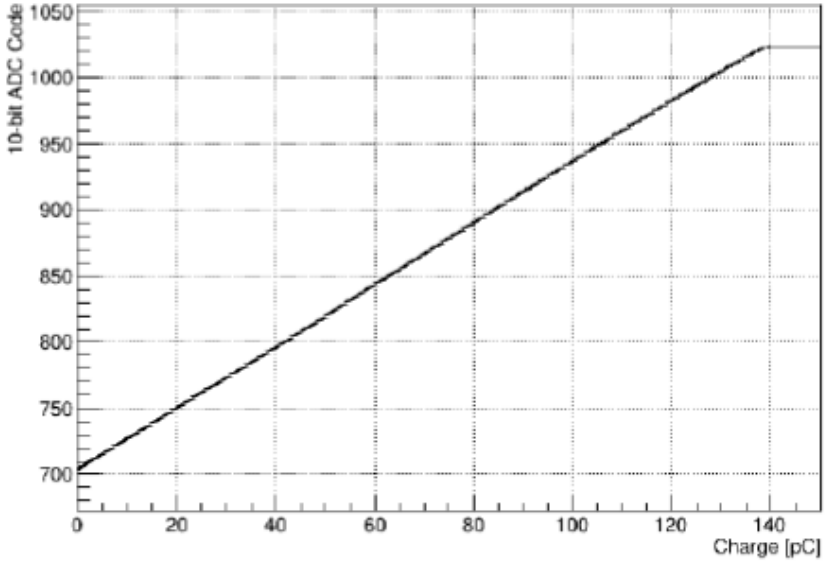
- Characteristics of current based topology
  1. input stages with low impedance but low or medium BW
  2. the impedance realized by feedbacks
  3. capable of hosting the full current/charge range (by large mirrors)
  4. a few (claimed) time based chips are actually current based (FlexToT, EXYT)



Pros and Cons of Current Based Topology

- high Signal to Noise Ratio for charge measurement, nice single photon spectrum, good energy resolution, linear charge response





- medium (not best) timing performance, but still ToF capable (< FWHM 500ps for LYSO systems)
- low power consumption (< 5mW), event based triggering, power gating ……

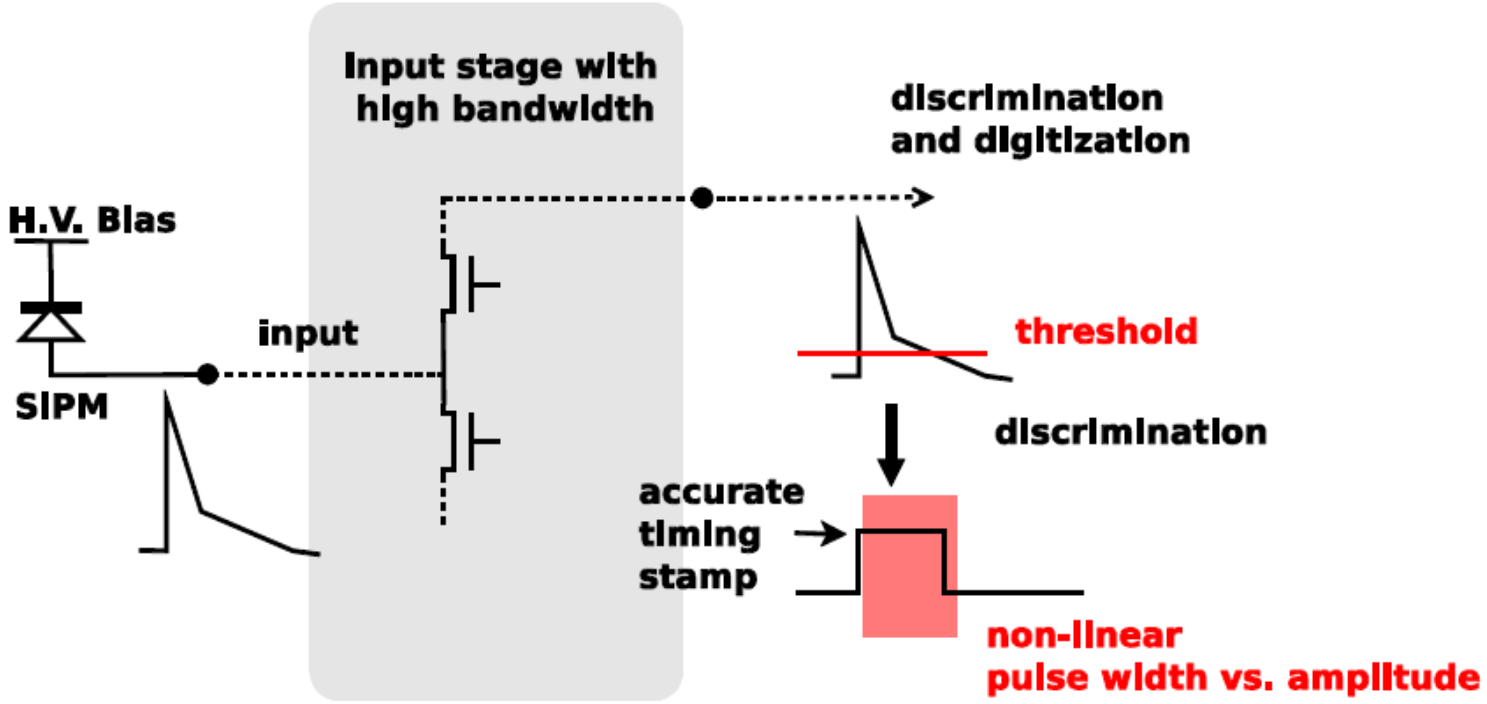
Pros and Cons of Current Based Topology

- System Coincidence Timing Resolution (300ps – 500ps) with realistic LYSO crystal size, systematic resolution energy resolution , preserving intrinsic resolution 9 – 12 %

- different designs focus on the power-timing trade-offs, better timing with more power
- BUT! the timing performance has its lower limit, ToF ~ 200ps with ordinary LYSOs not possible
- very suitable for a cooling free ToF system (~1mW/ch, < 500ps FWHM)

Time based topology

- Characteristics of current based topology
  1. everything optimized for timing
  2. input transistor selection, polarity fixed (NMOS favoured)
  3. no full range current/charge collection unit
  4. often non-linear charge response (but not always)
  5. often high power



Pros and Cons of time based topology

- Pros :

  high performance timing (physical limit)

  fast signal processing, less pile-ups

- Cons :

  high power consumption (cooling needed)

  limited charge processing capabilities,
  (photoelectric event selection still OK!)

ASICs developed for SiPMs in HD

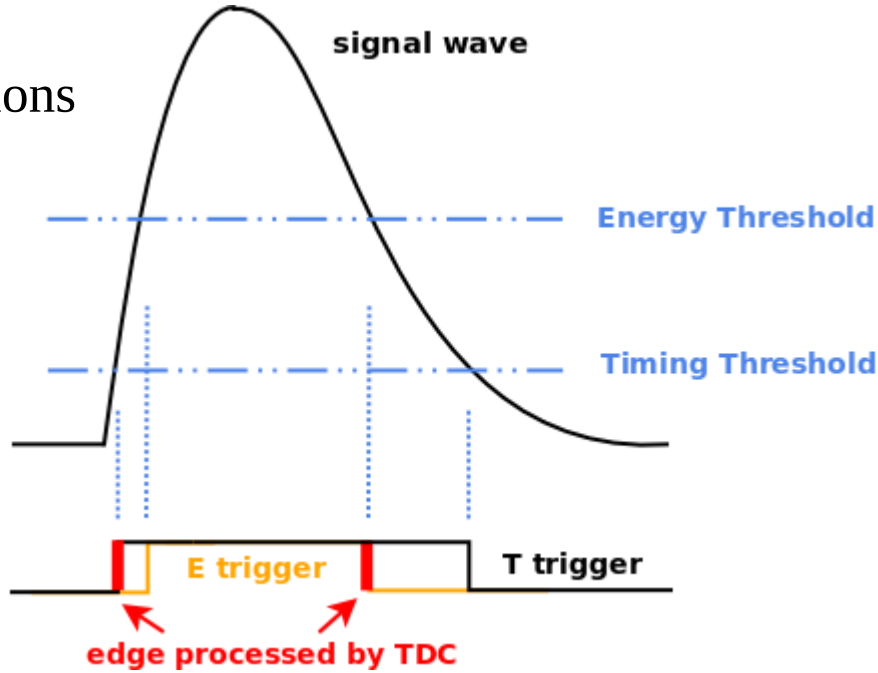
Overview: SiPM readout Chips in HD

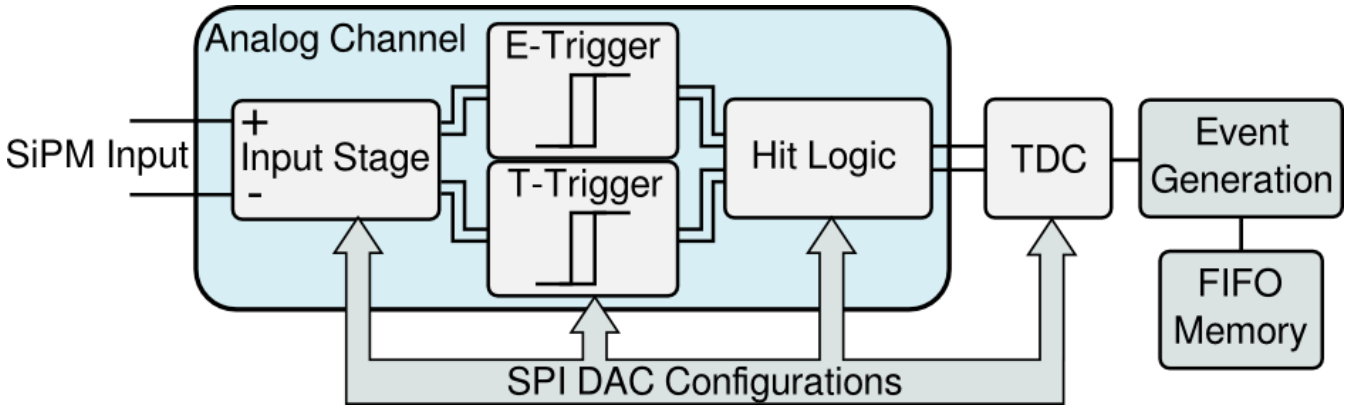
- STiC : SiPM high resolution Timing chip (SoC)
- uTRiG : SiPM high rate readout with high resolution timing performance (SoC)
- KLauS : SiPM frondend for high resolution charge/energy measurement (SoC)

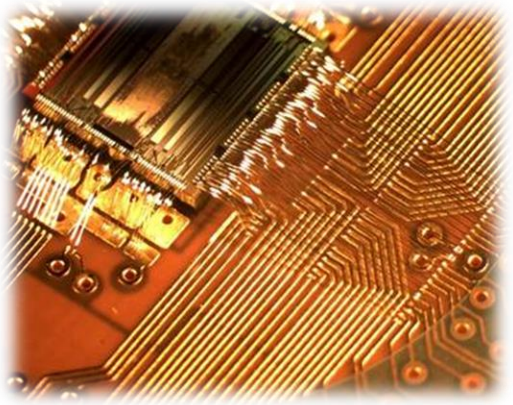
STiC : SiPM timing chip

STiC : basic readout principle

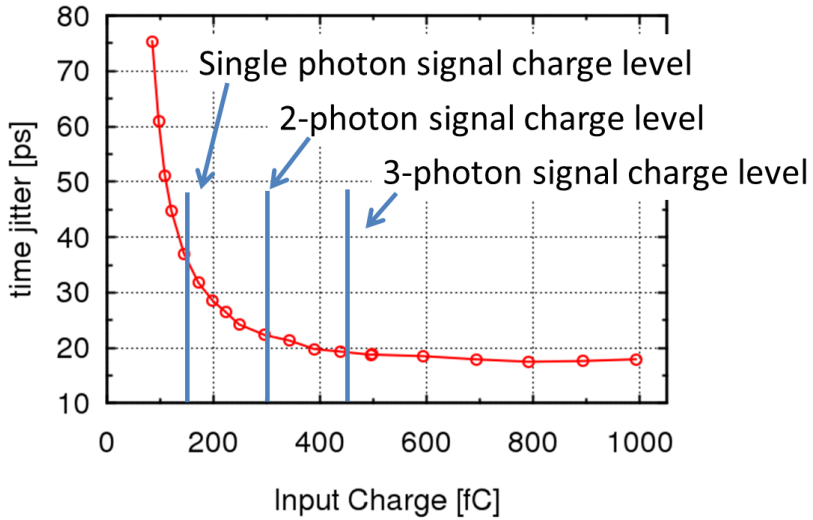
- 64-ch SiPM readout ASIC for ToF applications
- UMC 0.18 µm CMOS
- Time + (linearized) Energy based on TDCs
- Analog Frontend + TDC + Digital(8/10b)
- SiPM bias tuning (~500mV)
- jitter < 20 ps
- SiPM Dark Counts pile-up suppression

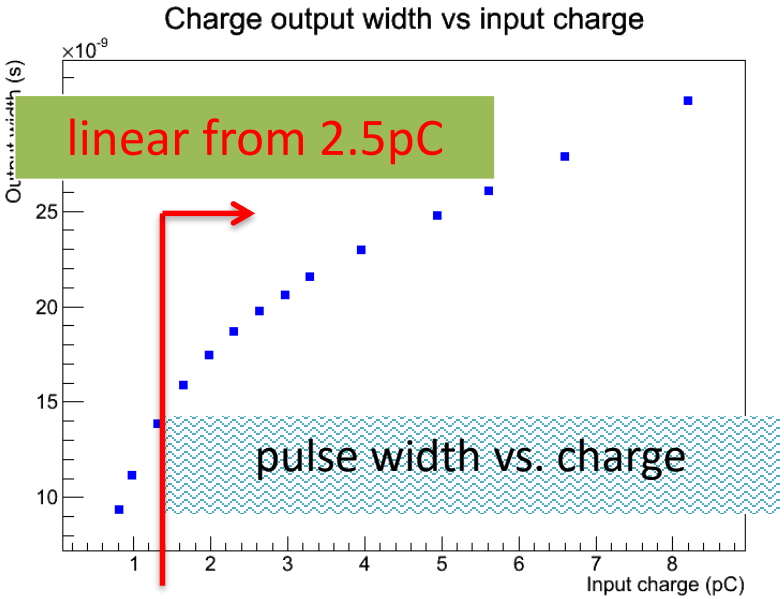


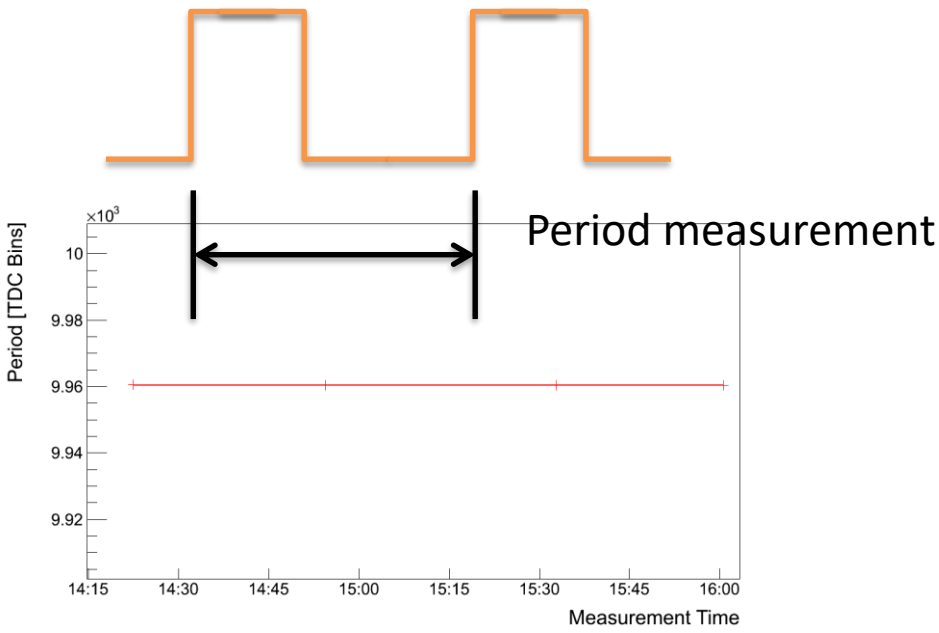


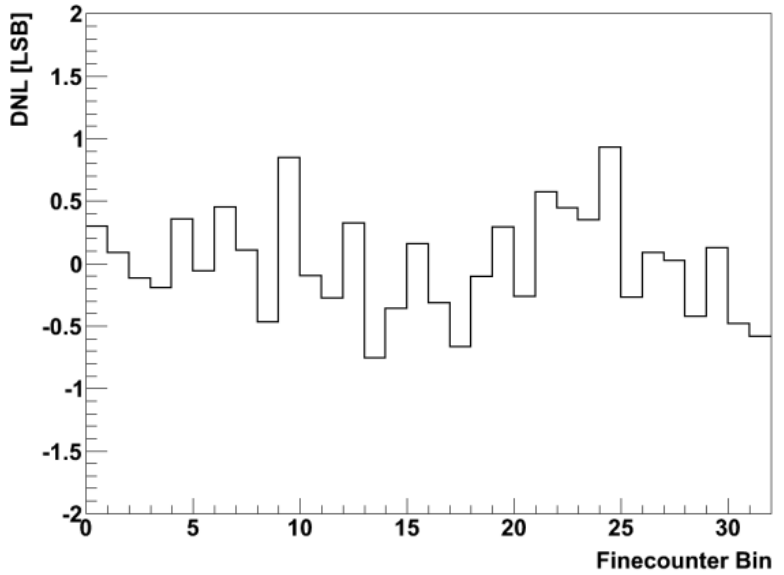


Measured Performance

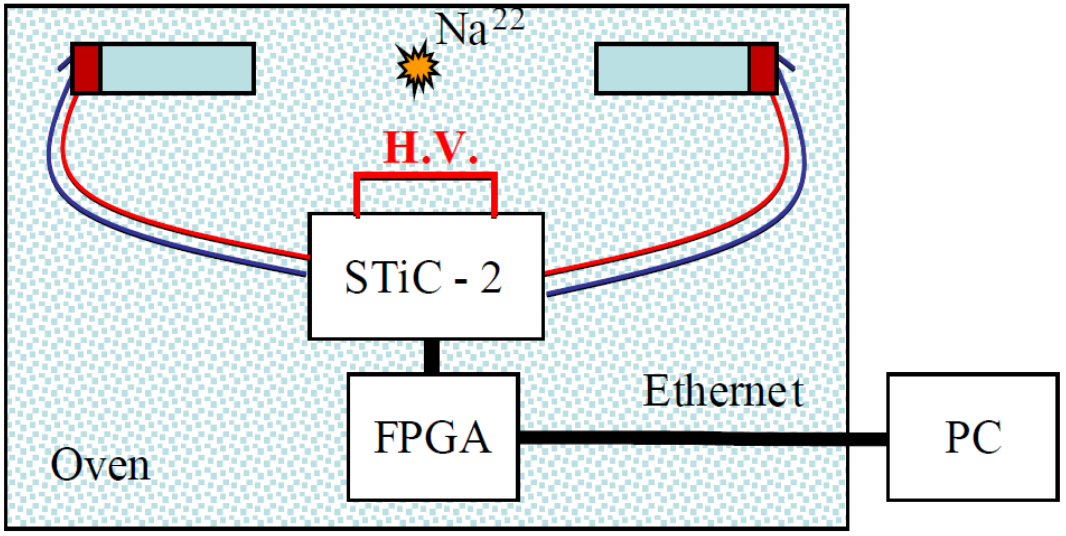




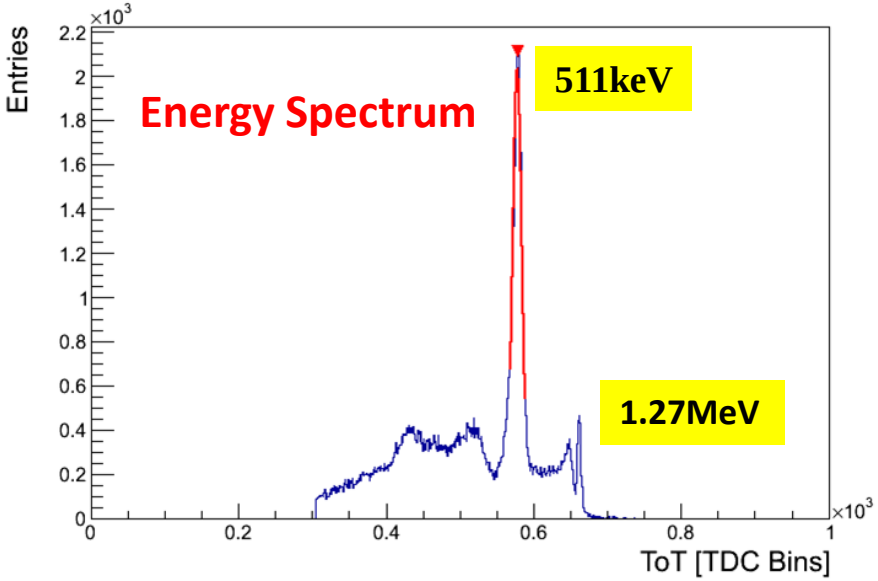


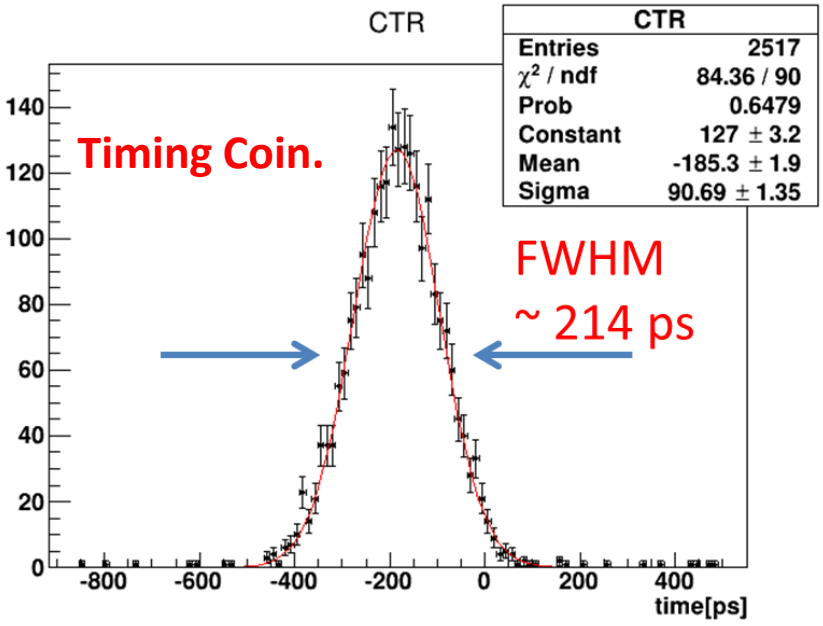


PET coincidence



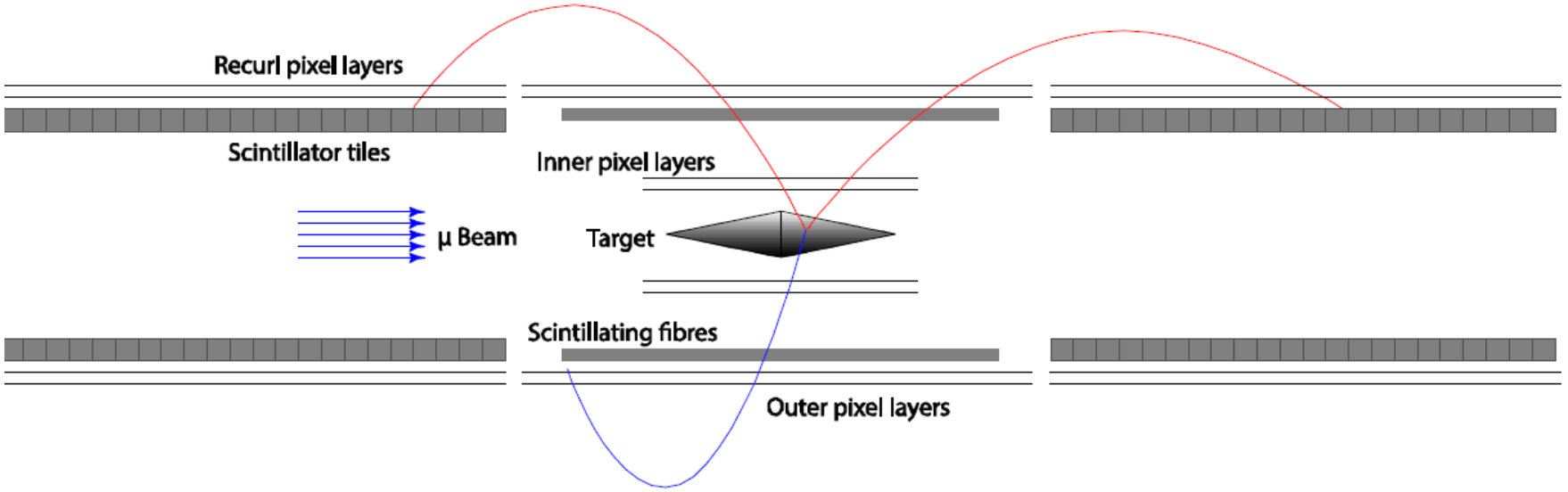
Na^{22} β^+ decay → coincidence with LSO 3.1x3.1x15 mm^3 +MPPC-S10625-33-50





Mu3e Tile detectors

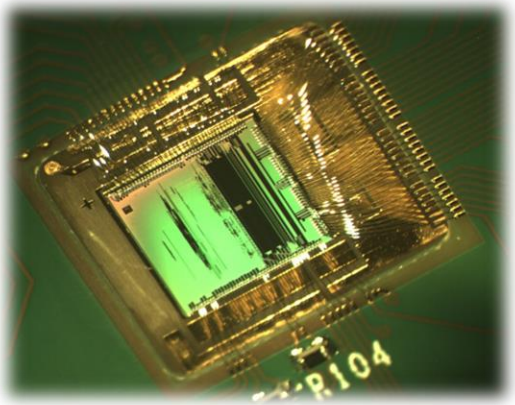
- To be installed in Phase I-b
- Plastic scintillator + SiPM
- Reduce combinatorial background
- **Goals:**
  - Time resolution ≈ 100 ps
  - Maximum efficiency → good pile-up separation



MuTRiG chip ver. 1.0

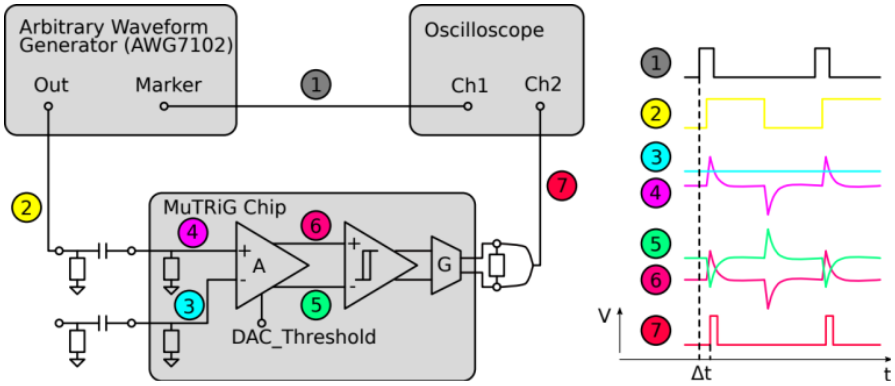
- Mixed-signal SiPM readout ASIC for precise timing applications
  - 32 channels
  - Individual SiPM bias tuning
  - 50 ps time binning TDC
  - Gigabit serial data link (1.25 Gbps)
  - Switchable event length (48/27 bits)
  - Analog channel inherited from STiC ASIC
- Digital functionality
  - External trigger
  - Cyclic Redundancy Check (CRC) for transmission error detectiaon
  - Channel event counter

Version 1.0 in 2017

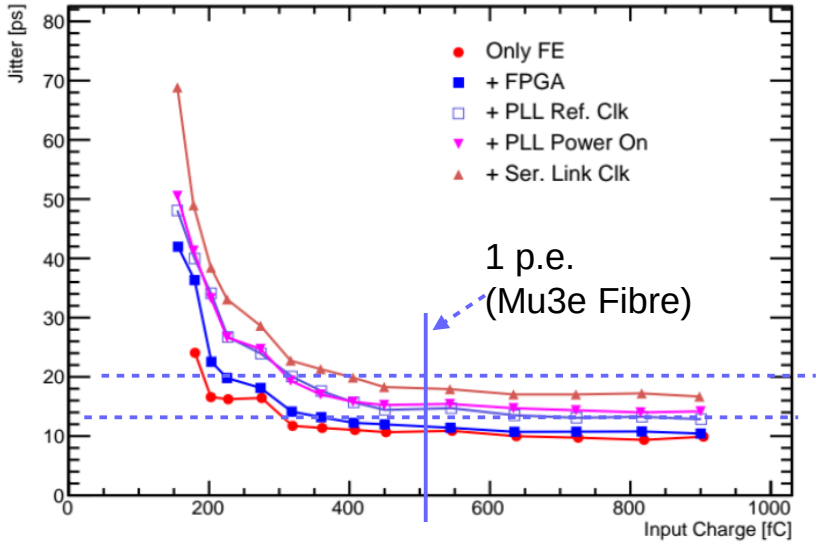


5 x 5 mm^2

Front-End jitter measurements



[Measurement setup, Capacitor = 15pF]



For charges > 480 fC (1p.e. Mu3e Fiber)

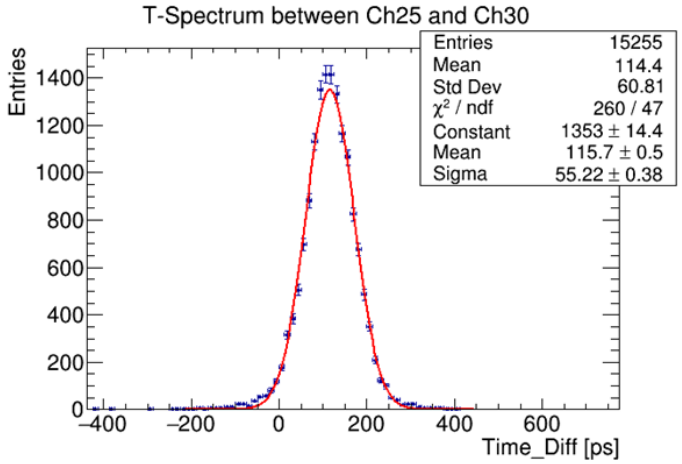
FE Jitter **< 12 ps**

FE jitter **< 18 ps,** when FPGA, clocks and PLL are all on.

Test beam results

At DESY, February 2018 with positron beam at 2.4 GeV

Coincidence time resolution



Scintillator:

- type: EJ228
- size: 6.5 x 6.5 x 5 mm^3

SiPM:

- Hamamatsu 50μm pitch
- Size: 3 x 3 mm^2

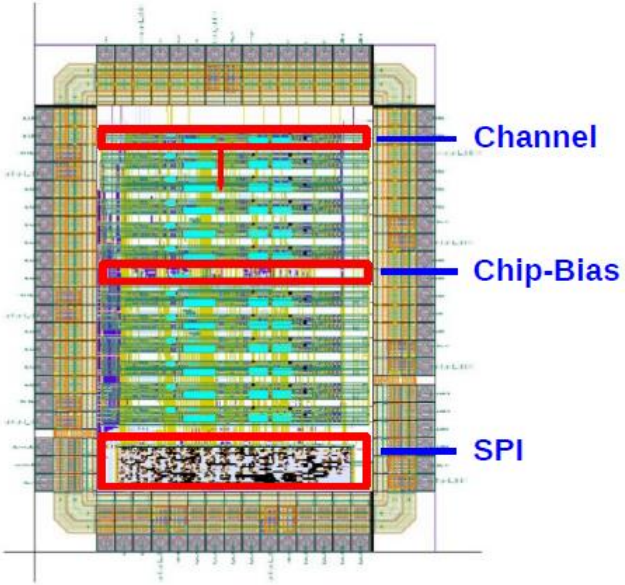
Channel N	σ
17	39.3 ps
23	45.6 ps
25	43.0 ps
30	34.7 ps

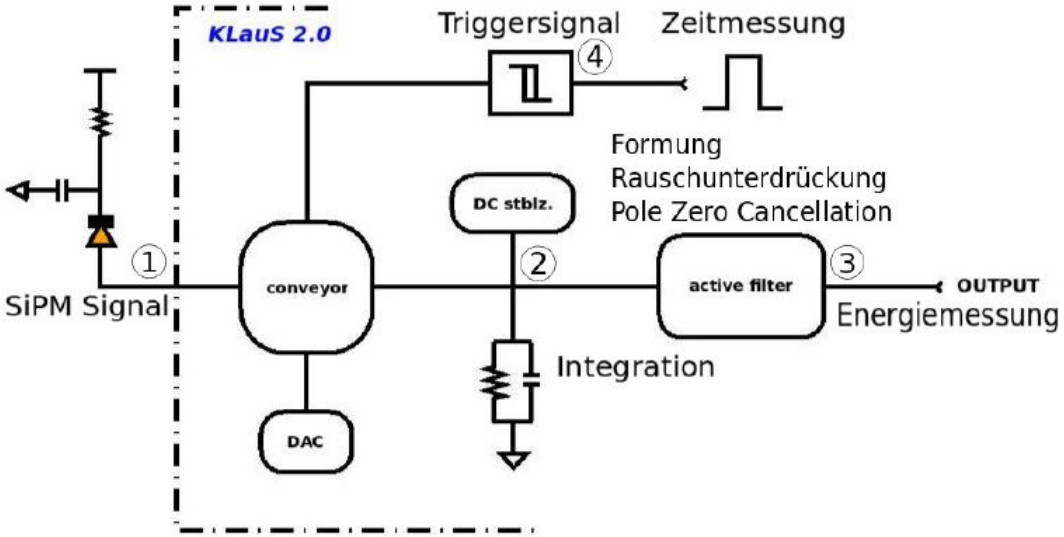
Achieved timing resolution for the tested channels

σ = 40.6 ps << 100 ps!

KLauS : frondend for charge measurement

KLauS overview

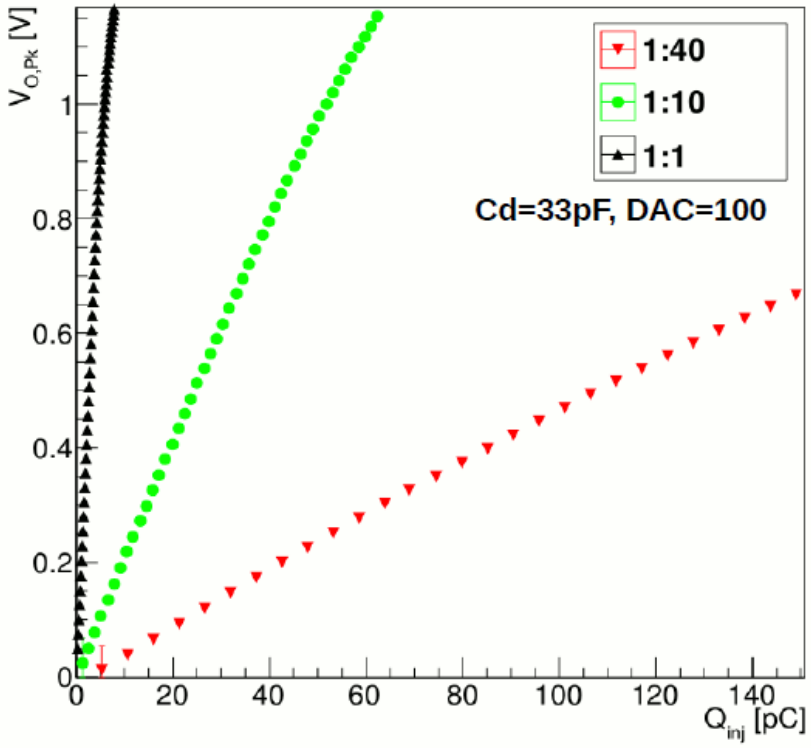




- 12 Channels
- SiPM bias tuning with a 8bit DAC
- Trigger with low time-jtter

- Analog output for charge measurement
- SPI configuration
- Powergating Capability

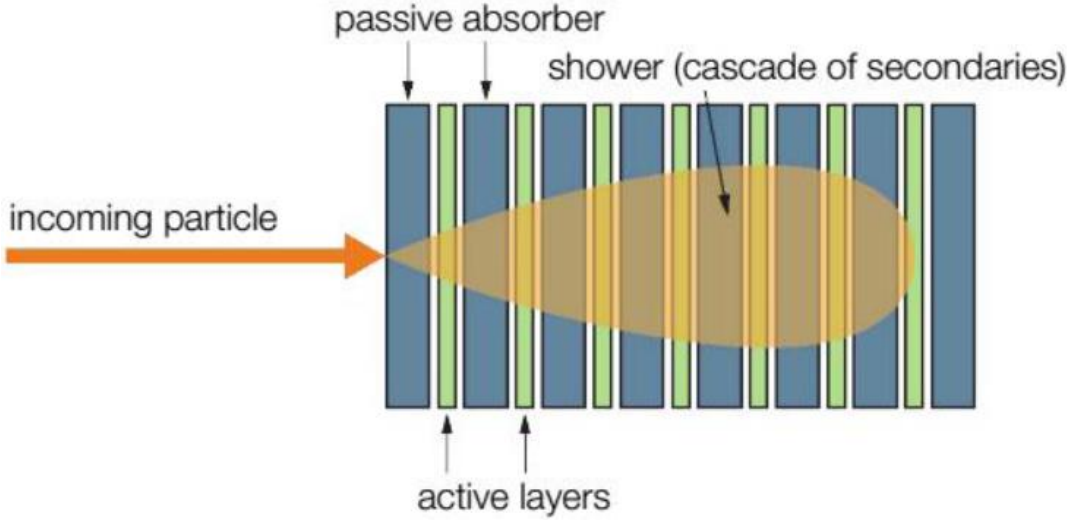
Charge measurement



- Input signal scalable in discrete steps (1:1, 1:10,1:40)
- Dynamic range depending on detector capacitance, 220pC @ Cd = 440pF
- For Cd = 33pC

Scaling	Conversion factor	FSR
1:1	187 mV/pC	4.4pC
1:10	19.6 mV/pC	49.2pC
1:40	4.4 mV/pC	138.4pC

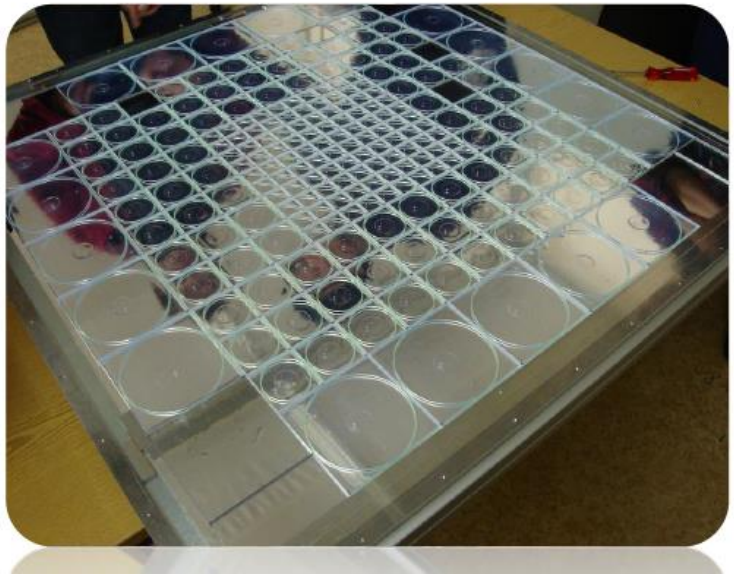
CALICE Analog Hadron Calorimeter



- sandwich calorimeter

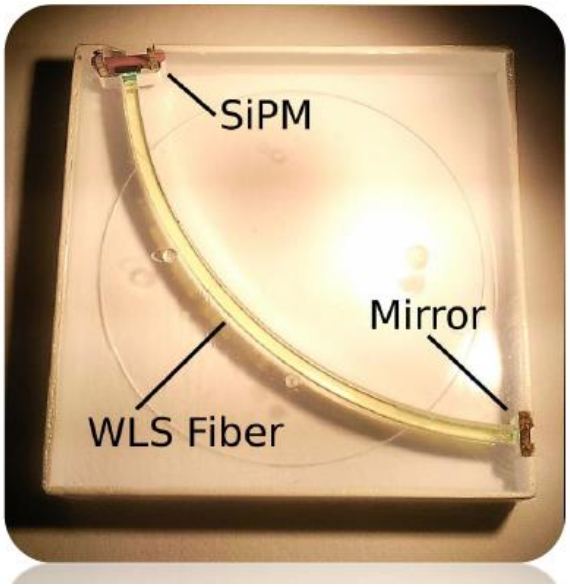
Absorber : Fe, Pb, U

Active : plastic scintillator
silicon
liquid & gas detector



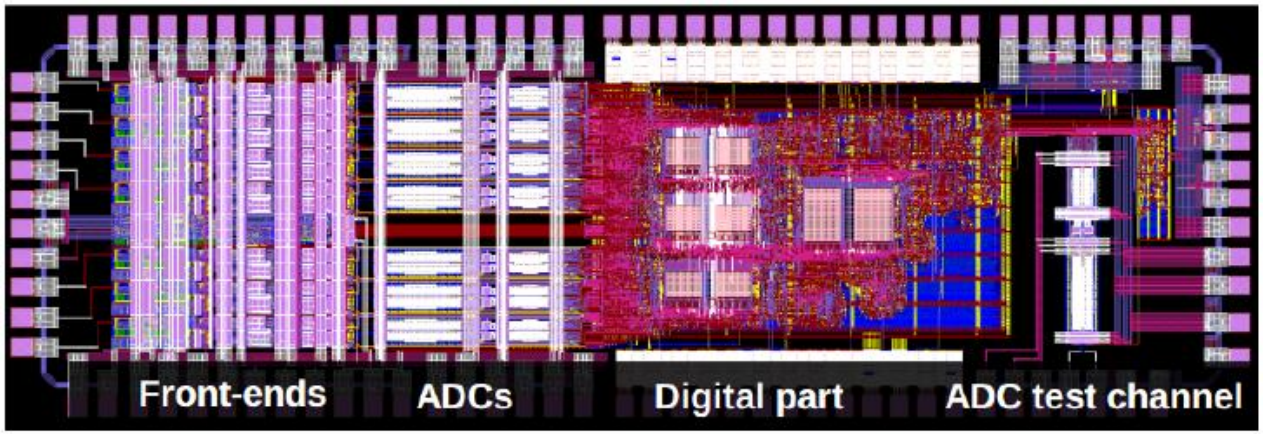
← active scintillator layer

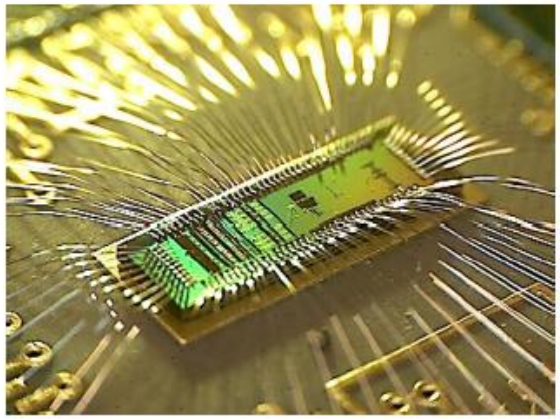
Silicon detector used to readout scintillators →



Towards a SoC SiPM charge Readout LoKas

KLauS - Kanäle zur Ladungsauslese für Silicon Photomultiplier

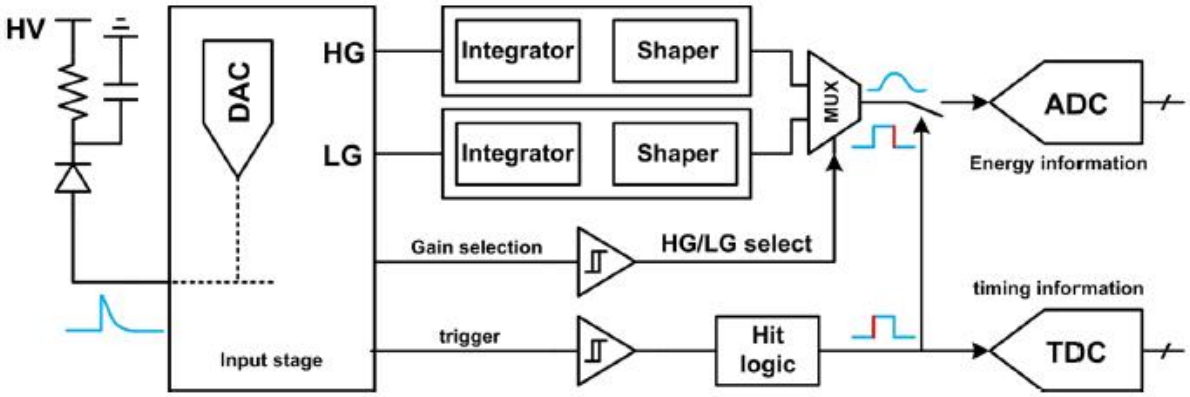


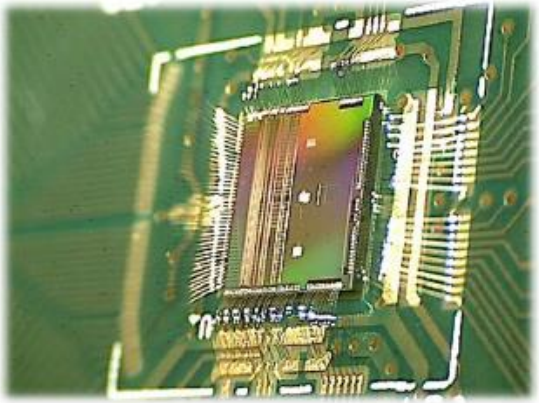


Submitted in May 2016

- **Mixed-mode** prototype
- UMC 180nm CMOS, 1.5 x 4.5 mm^2 mini-ASIC
- **7 channels** (Front-end + ADC + Digital control block)
- TDC with 25ns binning
- Fast LVDS (160 Mbit/s) or I2C link for data transfer
- SPI for slow control

KLauS chip and test setup





Low power, precise charge readout of SiPM

KLauS5

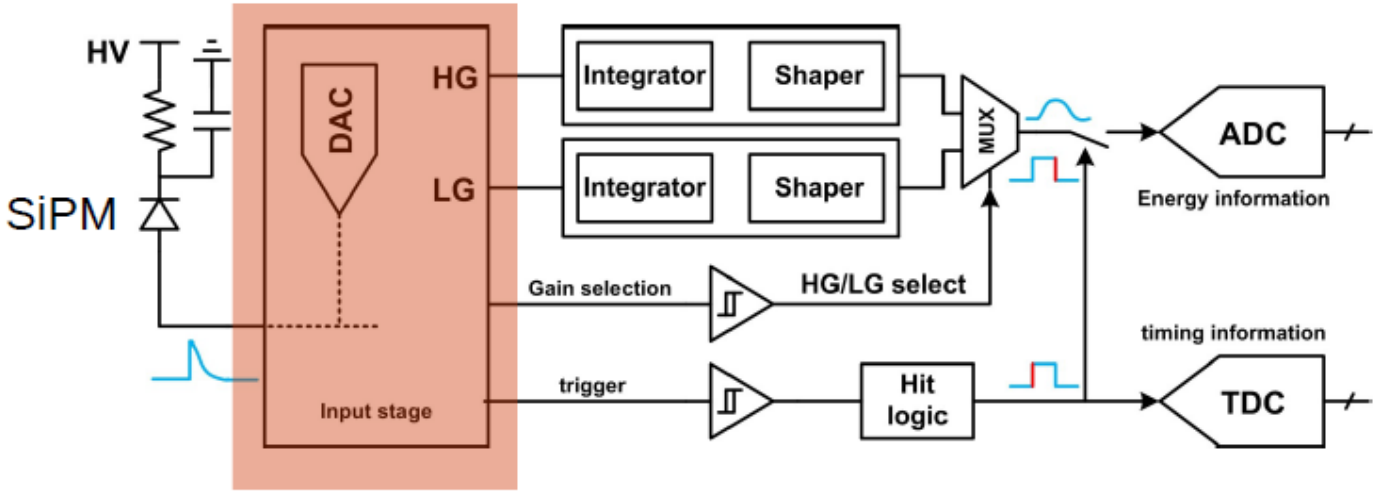
Received in Nov. 2017

Measurement setup:

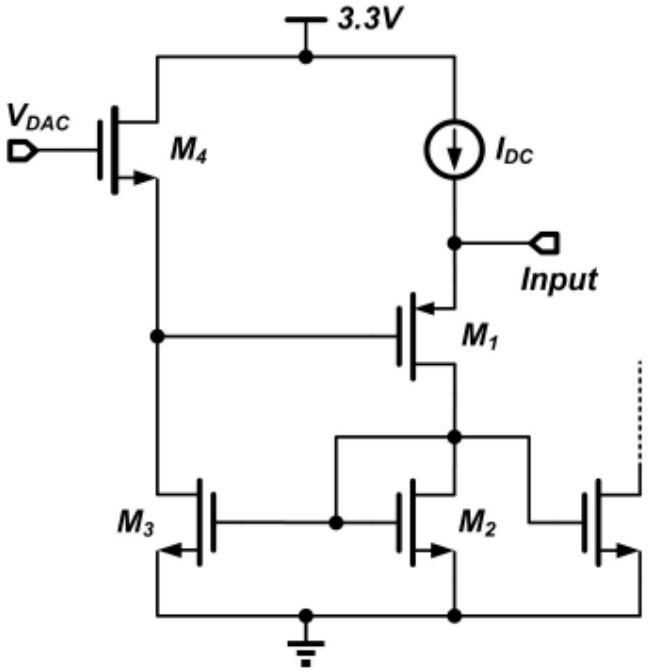
- **Raspberry Pi**
- **Interface board**
- **Testboard**

I2C/LVDS for data-taking

Inside structure: Front-end



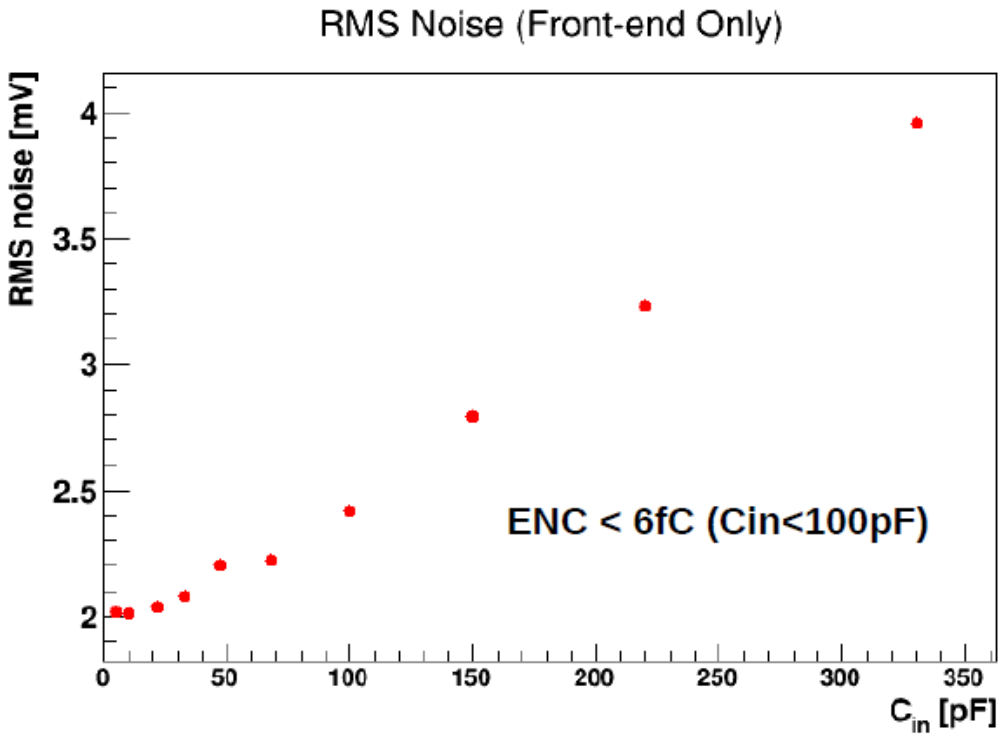
Channel block diagram



- **Front-end**: *Input stage, 2 integration branches, 2 comparator, ADC and TDC*
- **low input impedance:** *Common-gate structure + current feedback*
- **8b-DAC** - SiPM bias voltage tuning
- **Power-gating** functionality

Full chain : noise performance

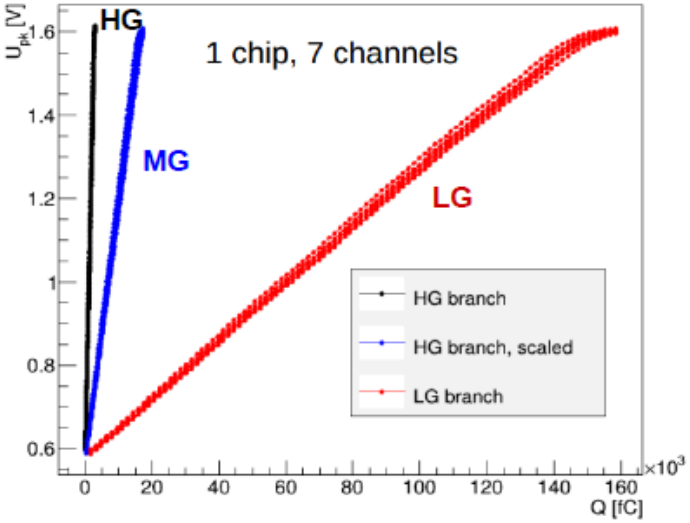
- *Measurement : The Root-Mean-Square of the pedestal voltage for different capacitance connected to the input terminal.*
- *Fixed charge input*
- *For capacitance < 100pF, the equivalent noise charge (ENC) < than 6fC*
- *Code spans from 3~5 ADC codes*
- *Stddev is around 0.6~0.8 bins (LSB=3.2mV)*
- *The front-end noise is the dominant*



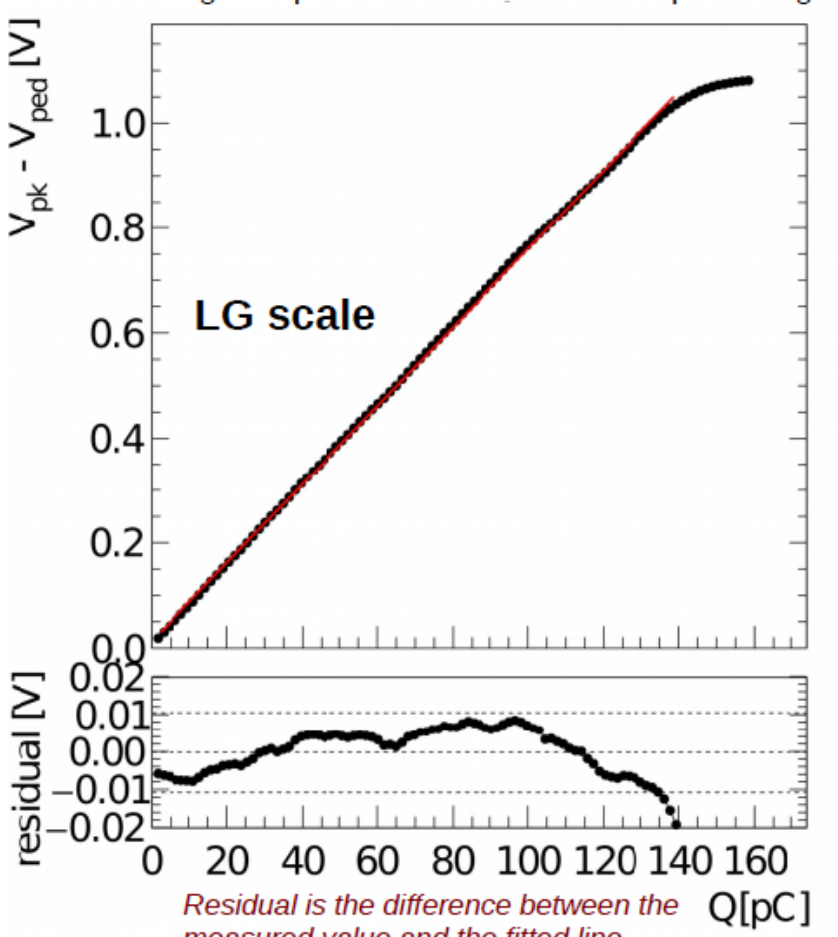
Front-end characterization

Charge injection pulse pass trough 33pF capacitor and is connected to the FE.
The FE output is measured with scope.

- **3 possible gain scale setting**
  - HG branch → 1:1(HG) or 1:7(MG) exclusive
  - LG branch → 1:48
- **Dynamic range** (1% Full Scale Range):
  - High Gain scale → 2.7pC
  - Middle Gain scale → 16pC
  - Low Gain scale → 136pC



Voltage amplitude as a function of input charge



Residual is the difference between the measured value and the fitted line.

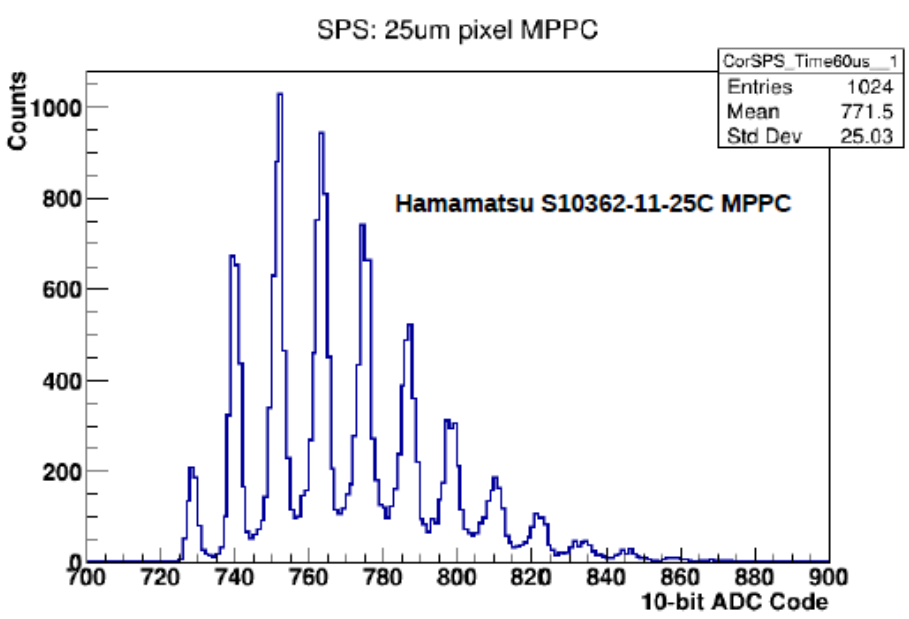
Measurements of the SPS

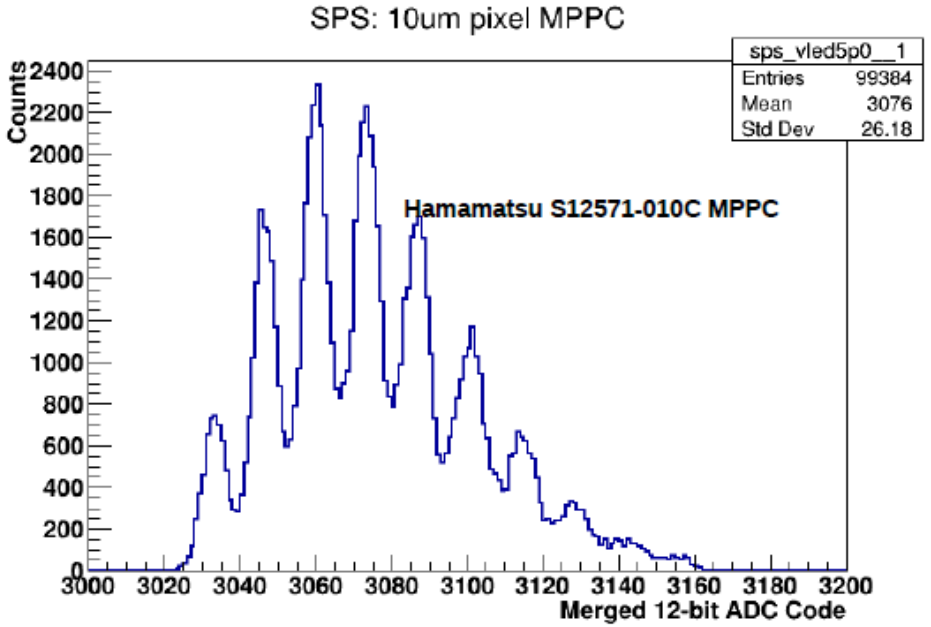
Single Photon Spectra (SPS): SiPM with different pixel sizes.
Sensor illuminated by a pulsed LED

- **SPS with 25µm MPPC**
  - Spectra recorded in self-triggered mode
  - Large gain: 10b ADC sufficient
  - ADC DNL correction performed

- **SPS with 10 µm MPPC**
  - External triggered mode
  - Small gain: 12b ADC used
  - SiPM operated at nominal bias voltage

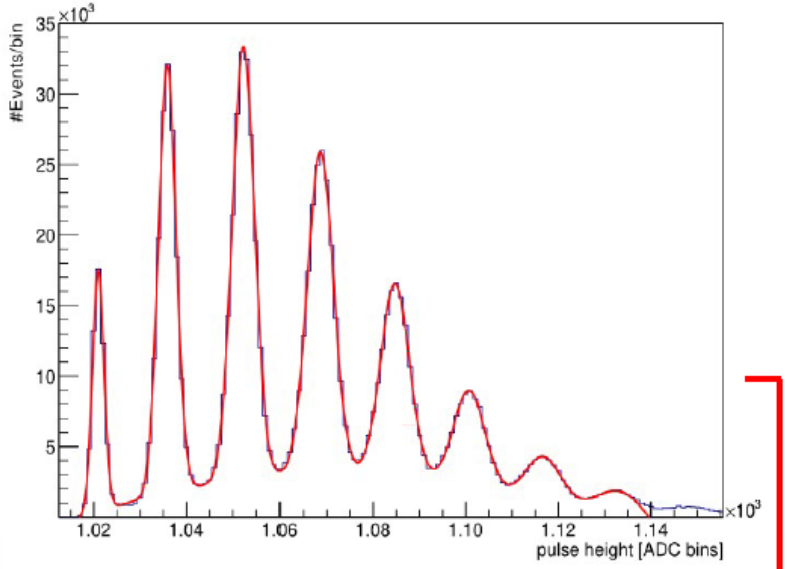
Gain = 1.35e5 (data-sheet)

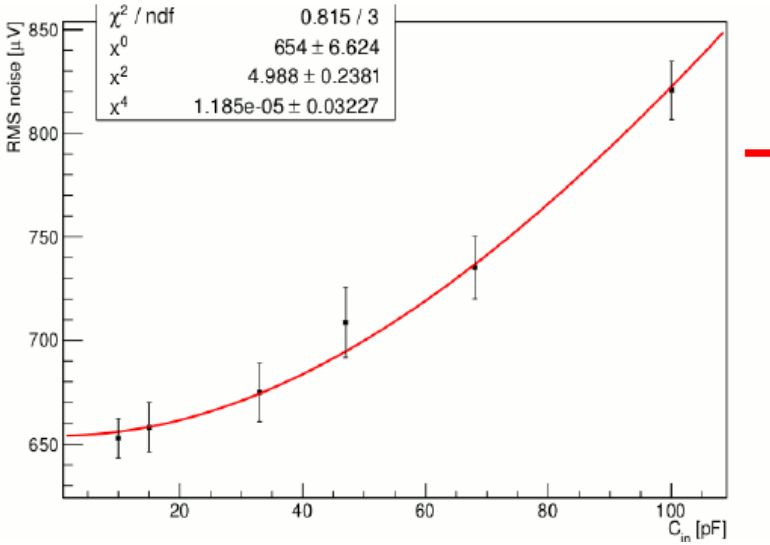




- For both cases a nice spectrum is obtained with clear peak separation.

Noise sources for high gain mode





Typical contributions to peak widths for a 1mm², 50µm-Pitch SiPM (Hamamatsu)

Source	Value (Abs.)	(Rel.) 1P.E.
SiPM-Leakage Current	50µV	$<10^{-3}$
Dark rate (Pileup)	≈ 1mV@500kHz	≈ 25%
Pixel gain uniformity	1.04mV@ 1P.E.	27.7%
Quenching fluctuations	1.14mV@ 1P.E.	33.3%
Electronic noise	700µV@50pF	12.5%
ADC (1mV/LSB)	290µV	2.2%

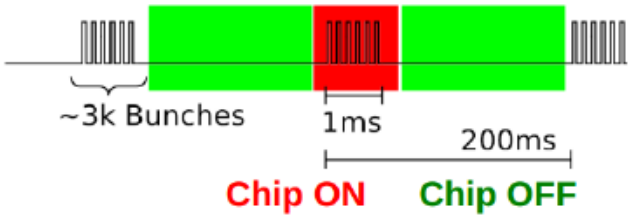
Signal to noise ratio for 1P.E. > 8

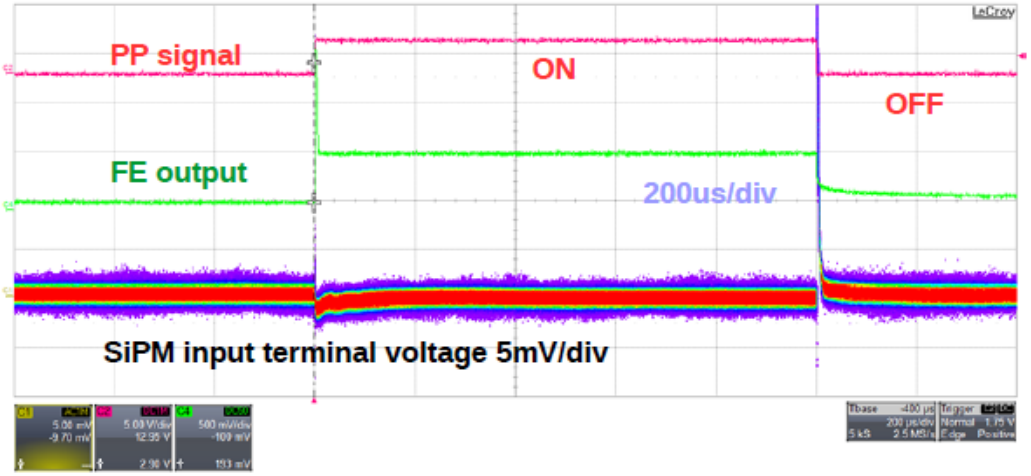
Power-pulsing features

Power pulsing scheme:

- Turn off ASIC when no events
- 25uW/Ch(>= 0.5%)

Beam structure





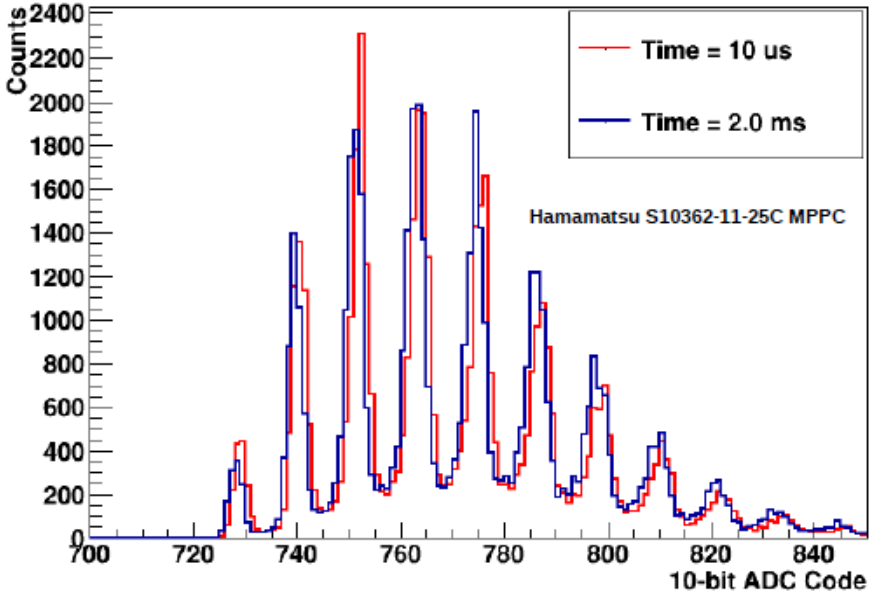
Key points:

- Stable bias voltage at the input
- Fast front-end setup < 10us

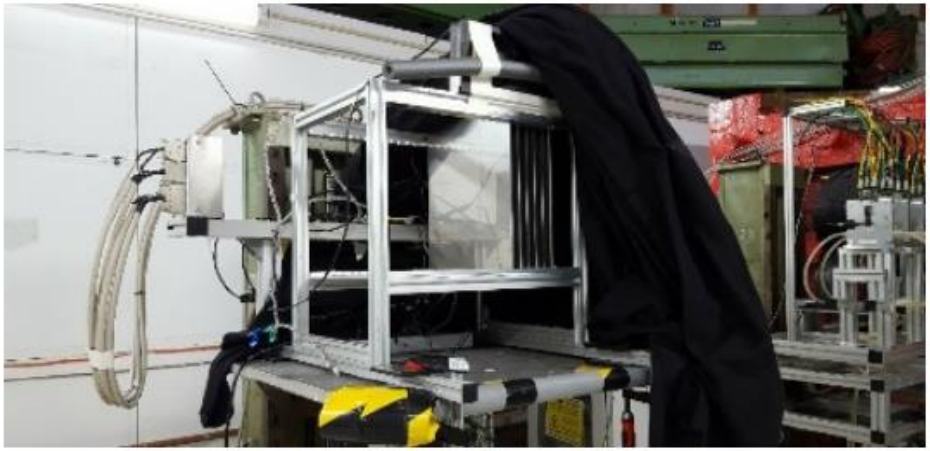
SPS at different illumination time respect to the ASIC ON time

- Almost no observable displacement

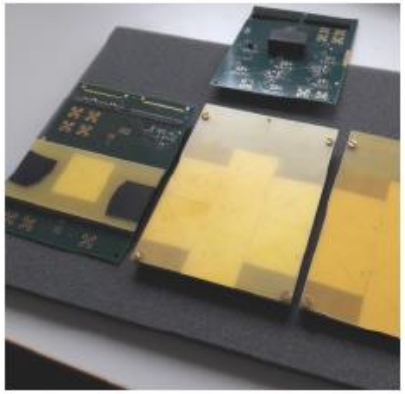
KLauS4 can work well with 10 µs after turn on during power pulsing

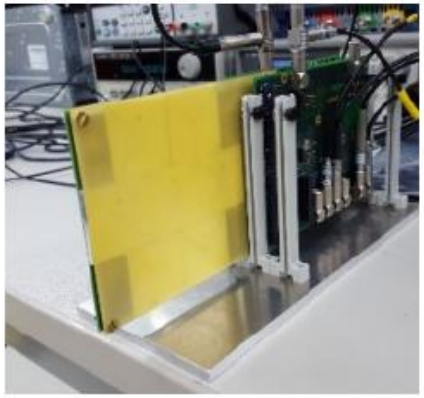


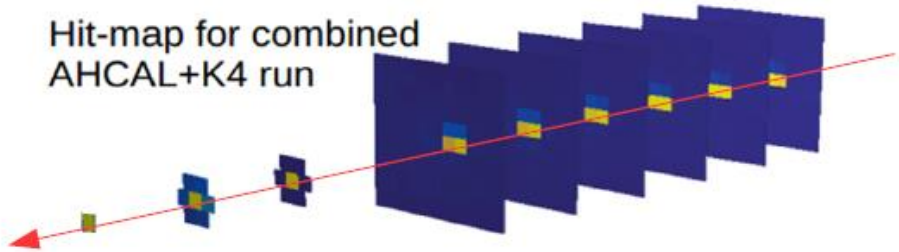
KLauS4 in DESY test-beam



- One week of beam in February
  - Parasitic to AHCAL DAQ tests
- 3 ASICs used
  - 1 board: single tile + SiPM in center
  - 2 boards: fully equipped (7 channels)

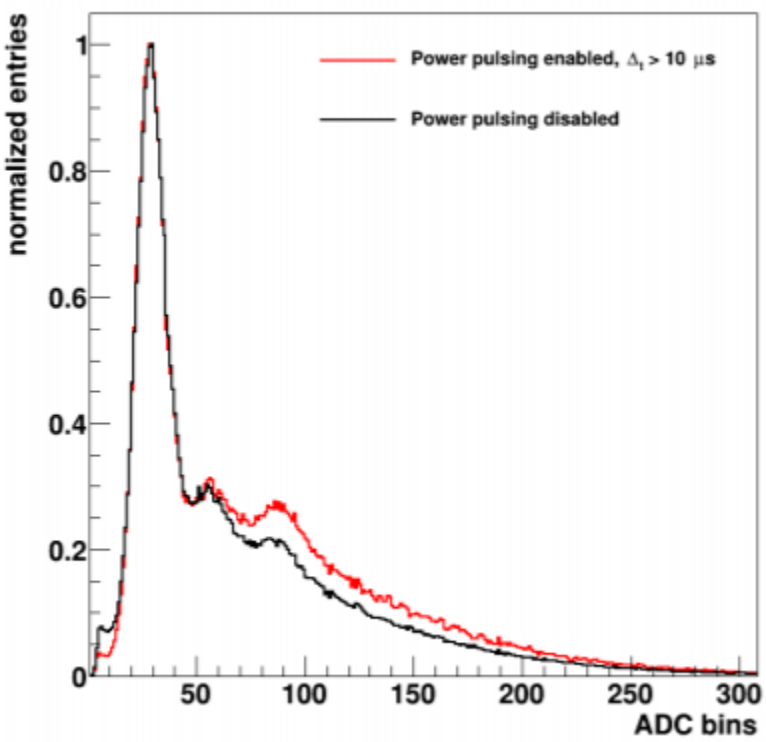


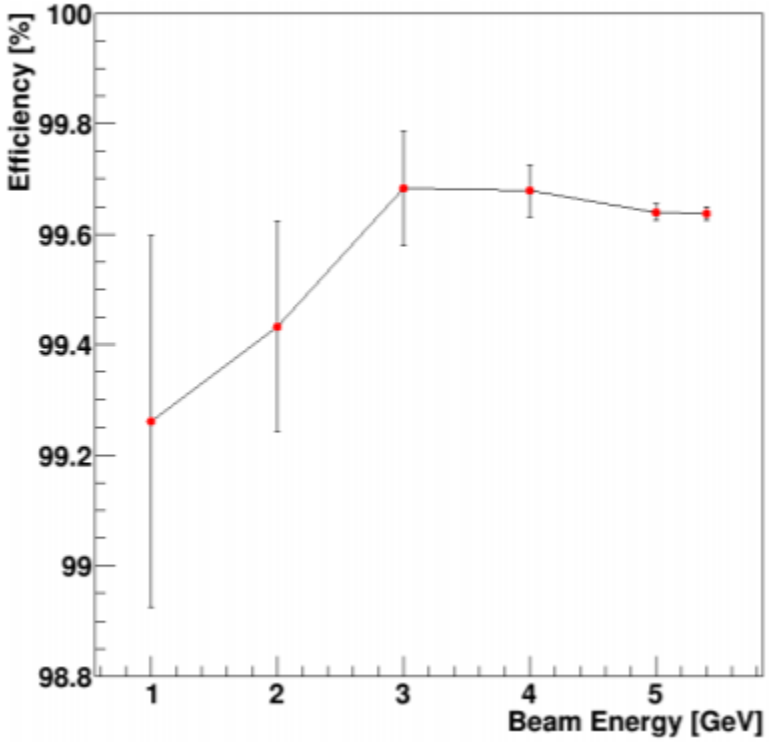




3 layers with KLauS4 6 AHCAL layers

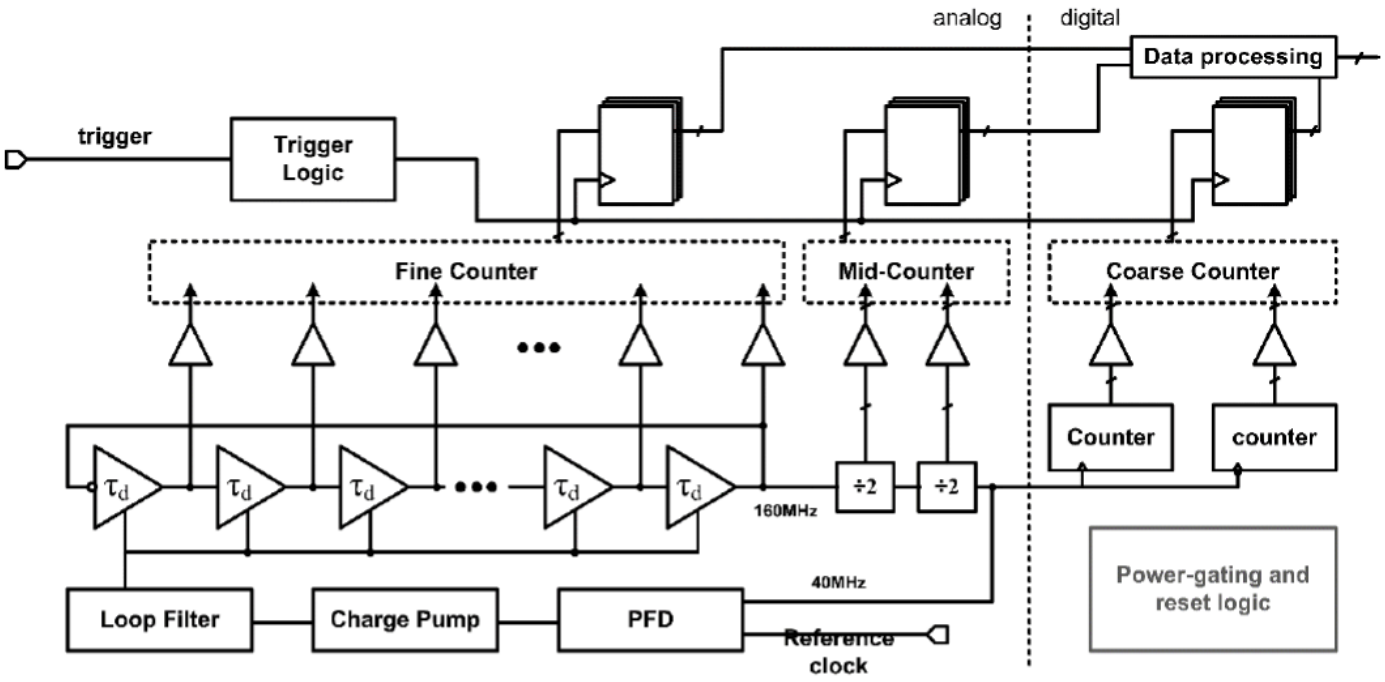
TestBeam Results





KLauS 6 , with 100/200ps TDC

KLauS PLL-based TDC Strucutre



- **Stable**
- **Fast lock < 5us**
- Power consumption:
  - VCO: 2.3mA
  - Buffers: 3.6mA
  - Latches: no DC power
  - Others: 0.6mA
  - Total: 6.5mA
  - 0.35mW/Ch
- **< 2µW/Ch (0.5%PP)**

- To be submitted @ July 29, design already finished