HPgTPC Readout

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Introduction

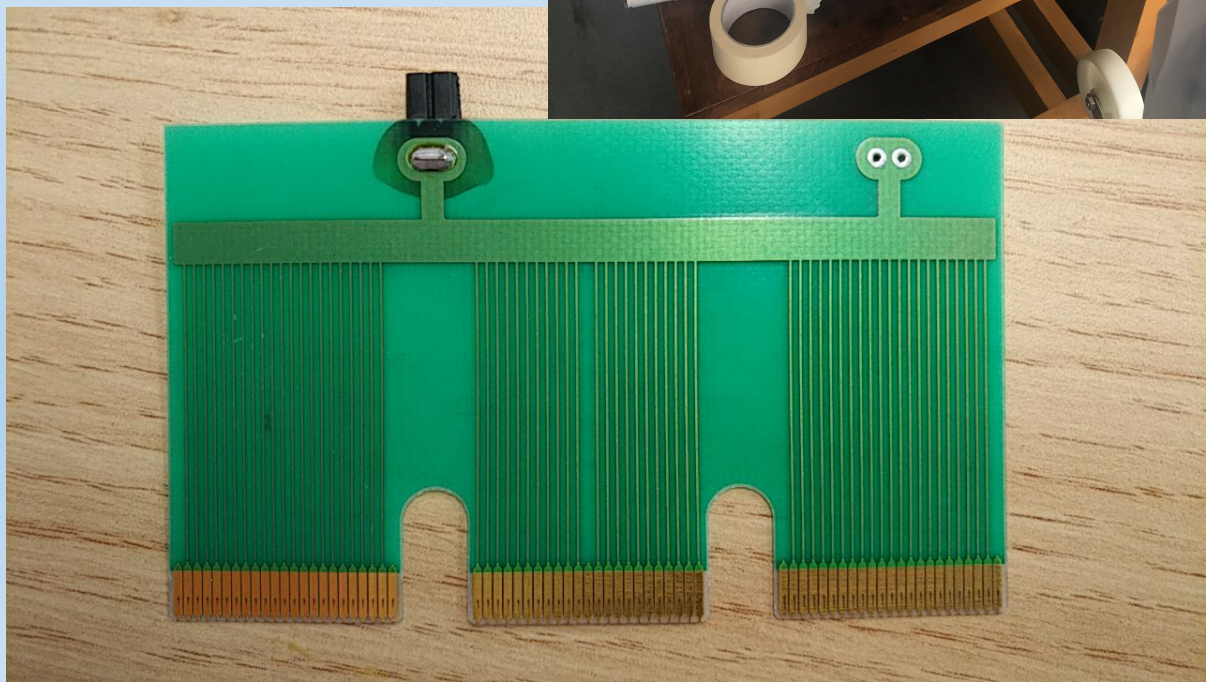
- HPgTPC is a gaseous TPC so drift speed is faster than LAr
- ALICE readout chambers that are being repurposed have about 570k channels. Will need to instrument new central region as well ~130k channels
- Intention is to design an HPgTPC DAQ that leverages work done for other DUNE subsystems DAQ
  - See Asher's talk for global ND DAQ discussion

Requirements

- Single hit resolution in z direction: aiming for at worst 1cm
- Number of channels: ~700,000 (ALICE ROCs + central region)
- Internal buffering must be sufficient for a trigger decision to be made
  - Exact value for this depends on other aspects of readout system so no hard number
- Dynamic range must be sufficient for signals from both protons and MIPs in 10 bar of Argon
- Heat output into the detector volume should not affect temperature stability of TPC active region

Interfaces, constraints: upstream

- Readout will connect to repurposed ALICE readout chambers (ROCs)
- Interface consists of pads arranged in lines of 23 pads/grounds (21-2 or 22-1) per connector slot
  - Blocks of 3 connector slots always contain 64 signal channels and 5 grounds
- Looking to build stiff PCBs that attach to blocks of three existing connectors with one copper trace per channel
- Easier to install than current fiddly connectors and constant number of channels per connector simplifies DAQ



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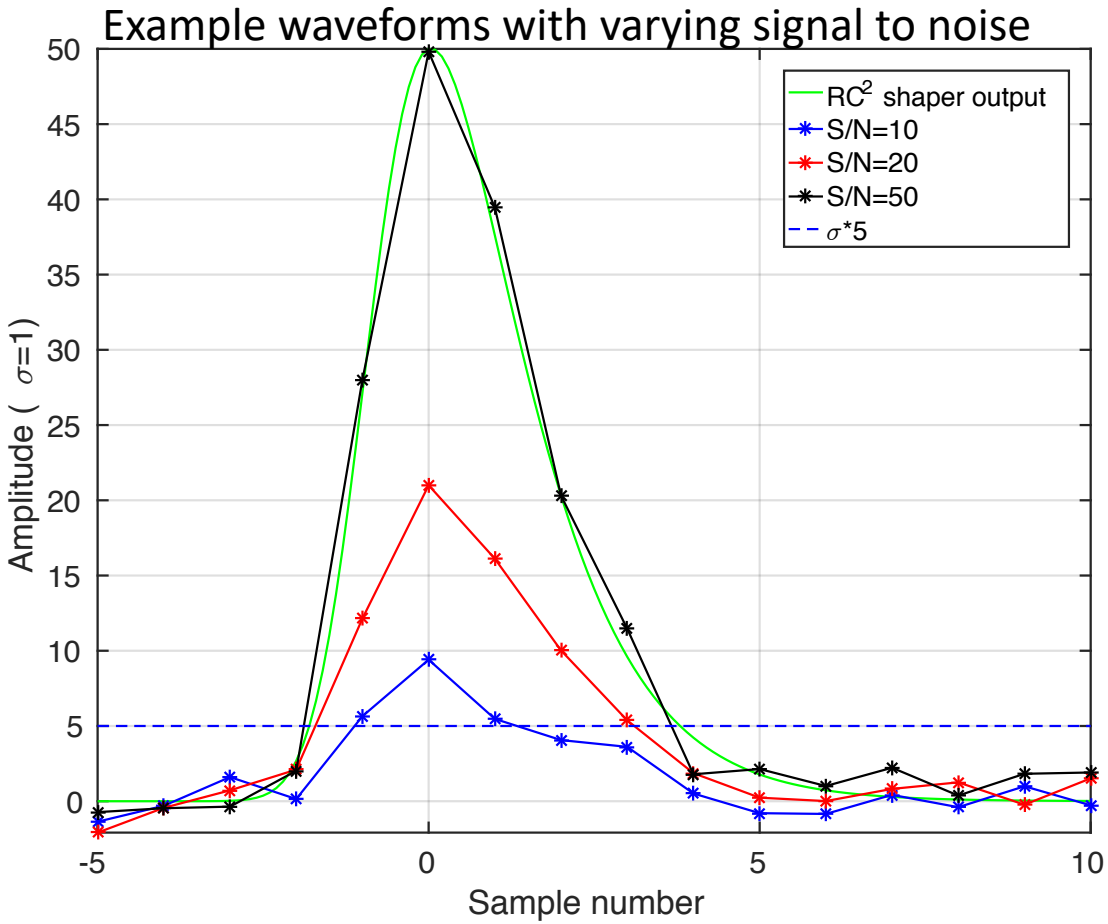
Interfaces, constraints: upstream

- Hardware level zero suppression will be needed to reduce data rate to an acceptable level
- Common industry standards are to zero suppress at ~5xRMS of noise and aim for signal to noise of at least 20
  - ALICE's design goal was a S/N of 30 for MIPs so this should be achievable



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Interfaces, constraints: downstream

- System will interface with Fermilab computing so final step must go into conventional computer
- Goal will be to keep rack space used as low as possible
- Number of fibers out will directly correspond to number of FELIX's that are needed and hence amount of servers

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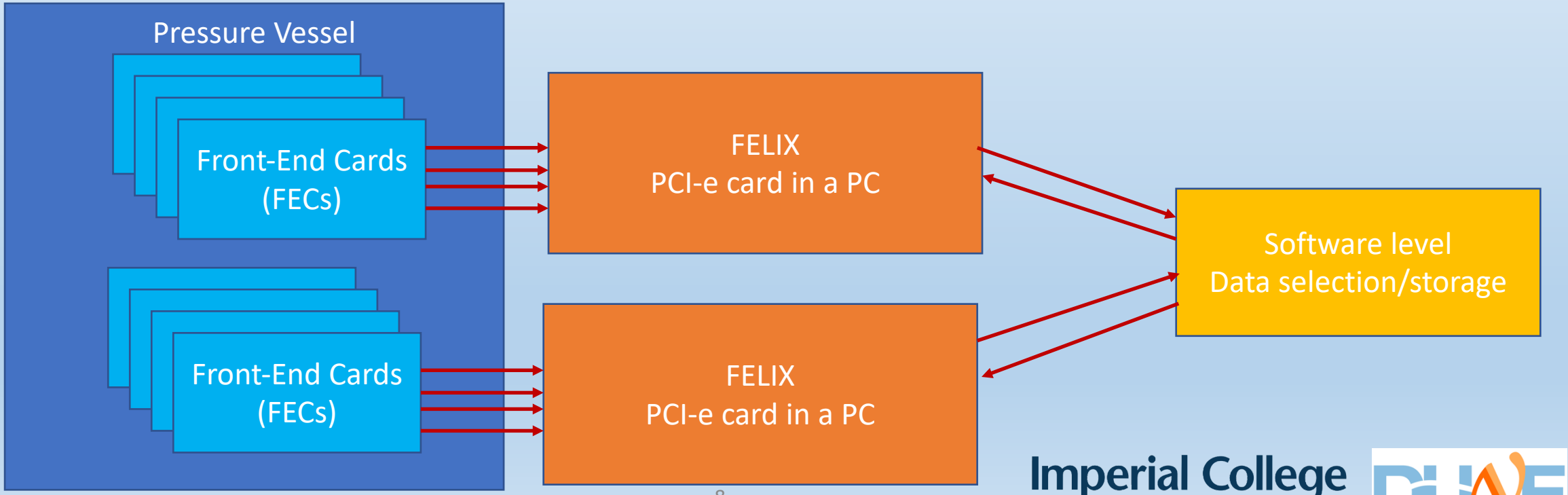
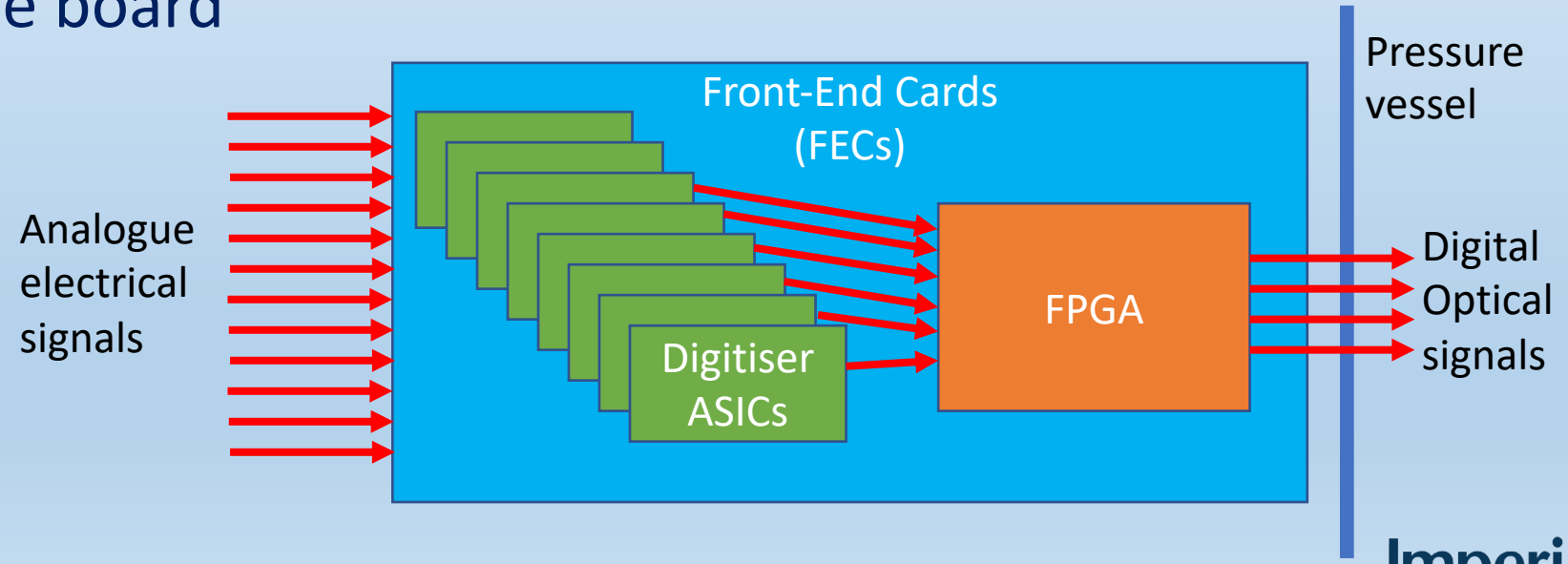
System design

- Number of feedthroughs on pressure vessel is limited and we want to limit the analogue signal path length
  - Therefore must digitize and zero-suppress on FECs before sending out of vessel
- FECs will be designed in UK, FELIX is an existing board



Front-end cards (FECs)

- Input is analogue electrical signals from detector
- Primary role is digitization of signals and zero-suppression
- Data then aggregated and converted to optical signal in an FPGA
- Possibility for buffering/low-level processing as will have an FPGA on the board



Longitudinal single sample resolution

- Choice of digitizer ASIC must have sufficient sampling frequency
- Argon gas has drift velocities O(10cm/us)

Required resolution	Implied Sampling Frequency
1cm	10 MHz
1mm	100 MHz
100um	1 GHz

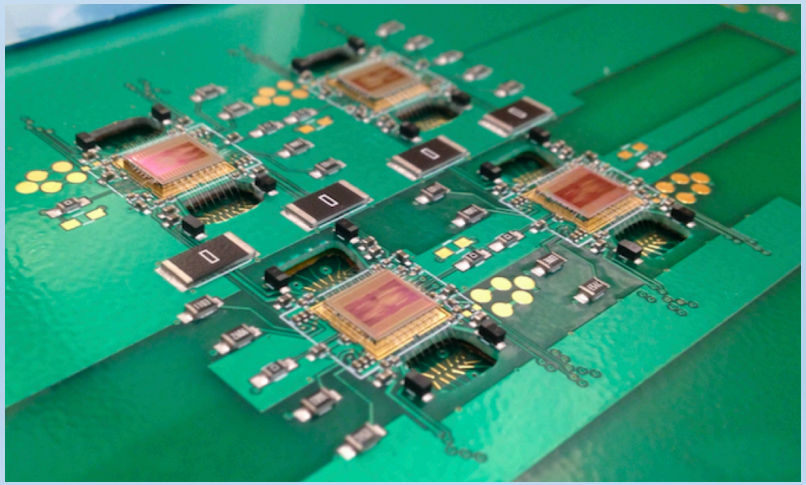
- Does not take into account longitudinal diffusion
- However, these are single sample resolutions so significant improvement from fitting multiple adjacent pixels
  - ALICE achieve 1300um precision with 5-10 MHz sampling

Digitiser ASIC options

- Investigating several options for digitizer ASIC on FECs
- FPGA also contributes to thermal budget (~50W for ~2000 channels)

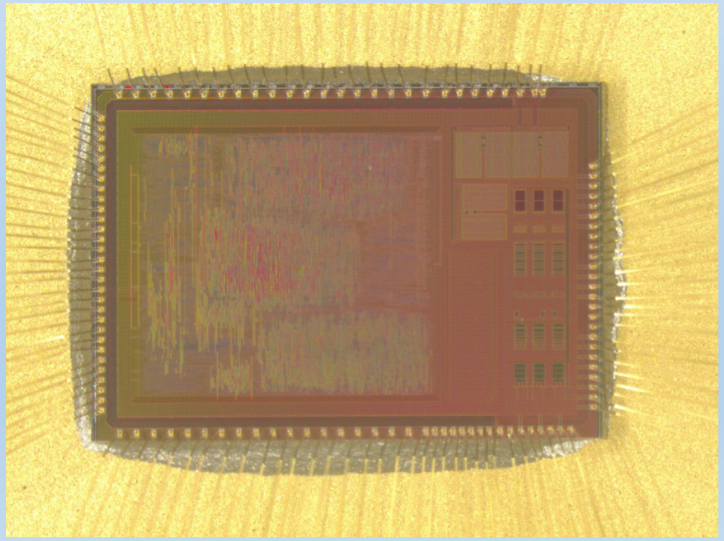
LArPix v2 chip

- 64 channels at 500kHz (but can be upgraded
- ~100 uW/channel (will go up with speed increase)



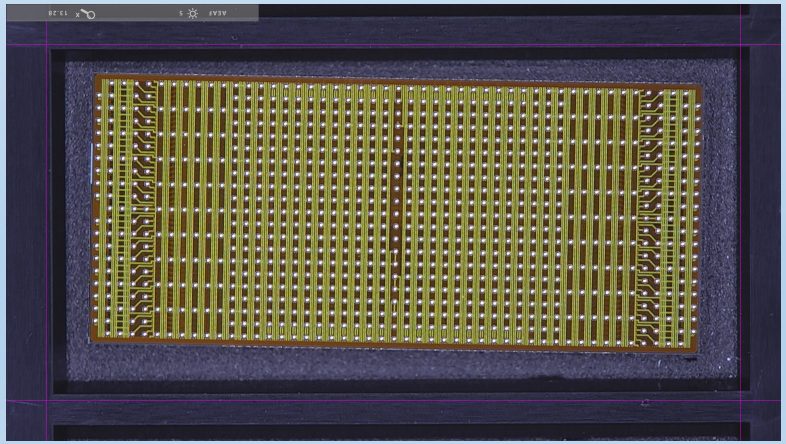
SAMPA chip develop for ALICE TPC upgrade

- 32 channels at 5 or 10 MHz
- ~35 mW/channel



HGROC chip developed for CMS HGCAL

- 72 channels at 40 MHz
- ~15 mW/channel



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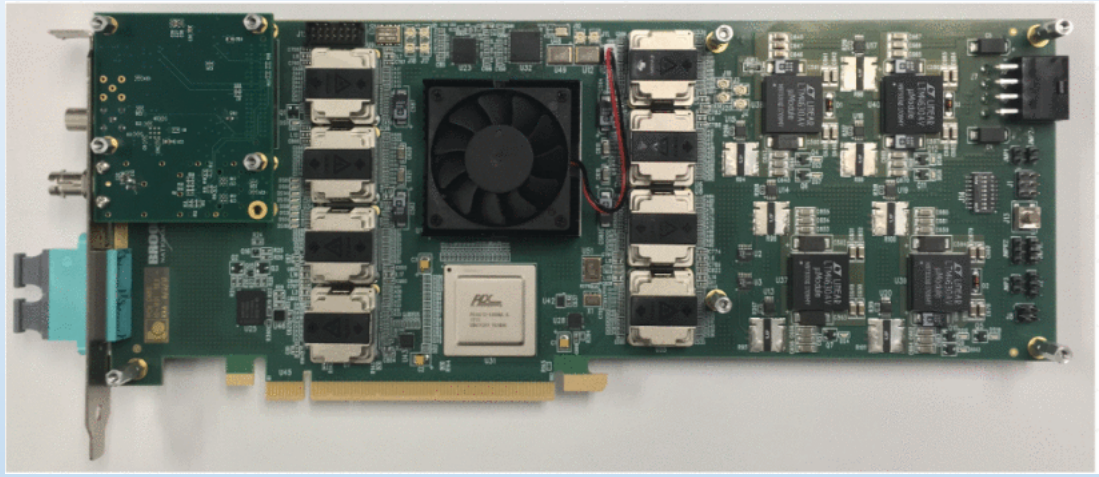
FELIX



- PCI-e board developed for ATLAS designed to be hosted in conventional off the shelf server unit
- Takes in 48 bi-directional optical links
- FPGA based electronics provides configurable interface to front-end electronics
  - Also capable of timing, triggering, data buffering, control, calibration and monitoring
- Already in use for DUNE FD DAQ

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Summary and Roadmap

- At the moment we're working towards a conceptual design for the system and choosing a digitiser ASIC for the FECs
- Soon will start technical design of the FEC which is the hardware component that needs the most work
- Felix part of system onwards is generalisable to other MPD subsystems

Task	202X				202X				202X				202X			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Intial design of FEC prototype																
Production and testing of 1st and 2nd FEC prototypes																
Larger pre-production runs and integration testing of																

Task	202X				202X				202X			
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
Production of HPgTPC DAQ system												
Installation of HPgTPC DAQ system												
HPgTPC commissioning												

FEC development roadmap worked through with Imperial College engineers

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Summary

- We are producing a conceptual design for HPgTPC readout
- Work is underway to choose an appropriate digitiser ASIC for the front-end cards (FECs) and we also hope to start the technical design of the FECs soon
- Felix part of system onwards is generalisable to other MPD subsystems and already in use for FD DAQ
- Simulation efforts are necessary to firm up details of occupancy that will be essential for system design

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