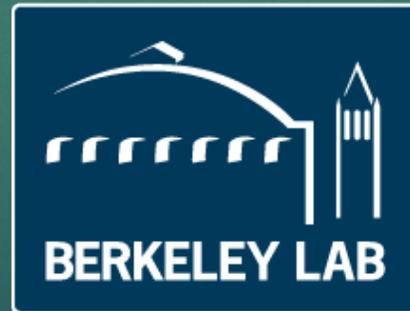


The Qpix Consortium

Organized to Design, Develop & Test A Novel Readout Concept for a Kiloton Scale Large TPC

Mitch Newcomer for the Qpix collaboration



Thanks to Jonathan Asaadi for authorized re-cycling of many of the Qpix introductory slides here

Important Readout Requirements for DUNE scale LAr TPC neutrino detectors

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Interesting Neutrino Events are rare. Each is precious!

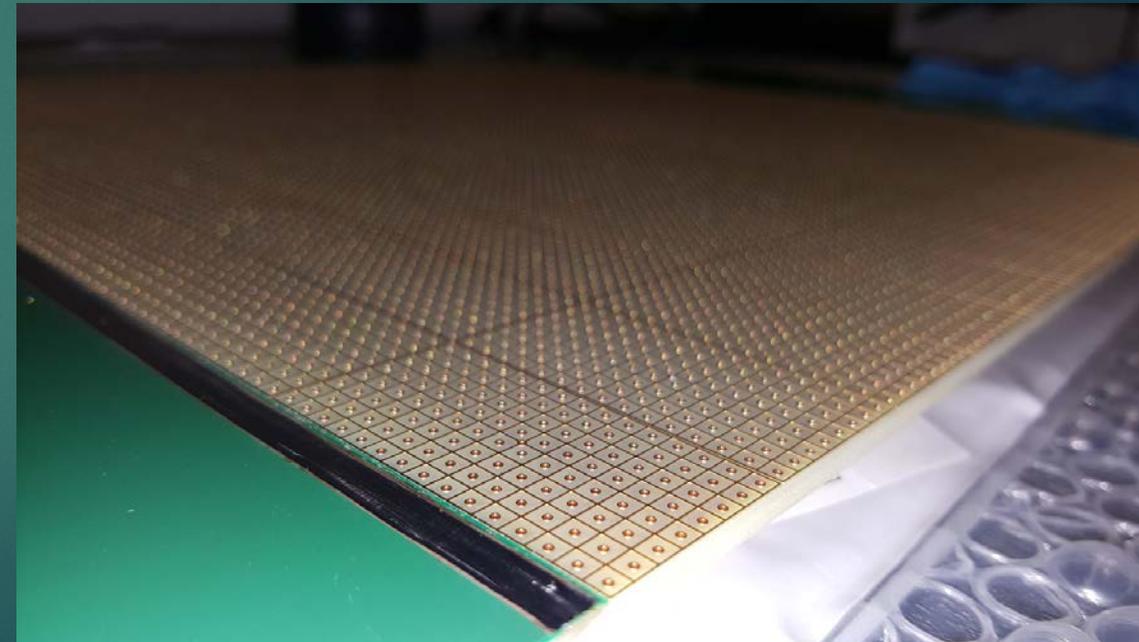
- ▶ Resolution should be determined by the intrinsic limits of the target medium (LAr) ... not the limits of the instrumentation.
- ▶ Optimum size for a pixel detector would be set by the ionization diffusion resulting in $\frac{1}{4}$ to $\frac{1}{2}$ cm pixel geometries. ~100M pixel ch. per DUNE size module.
- ▶ TPC data should contain enough granular correlated @, time and charge information to accurately reconstruct the path of tracks and their interactions along the way.

Electronics Noise needs to be significantly lower than signal

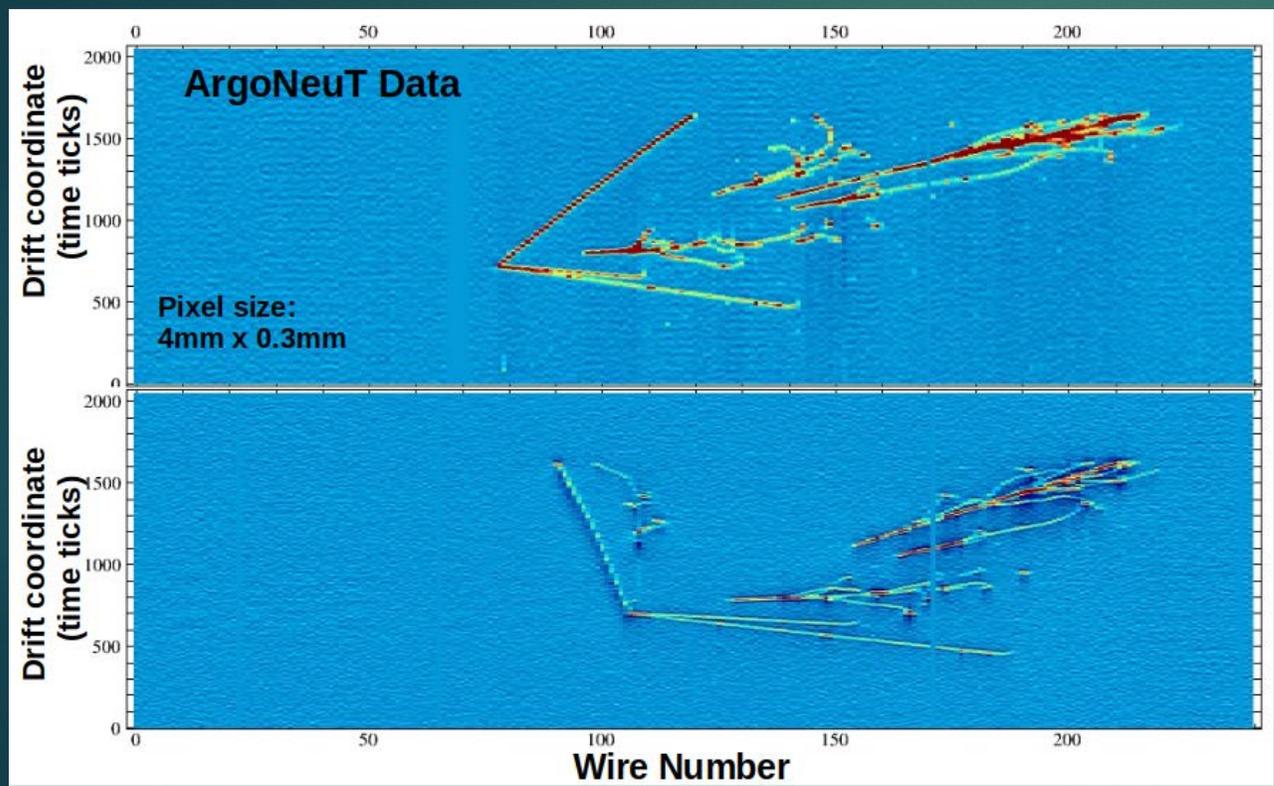
- ▶ Pixel FE readout must be in the cold, near the pixel sensors.
- ▶ Electronics heat load must not cause LAr boiling

LAr pixel readout .vs. wires

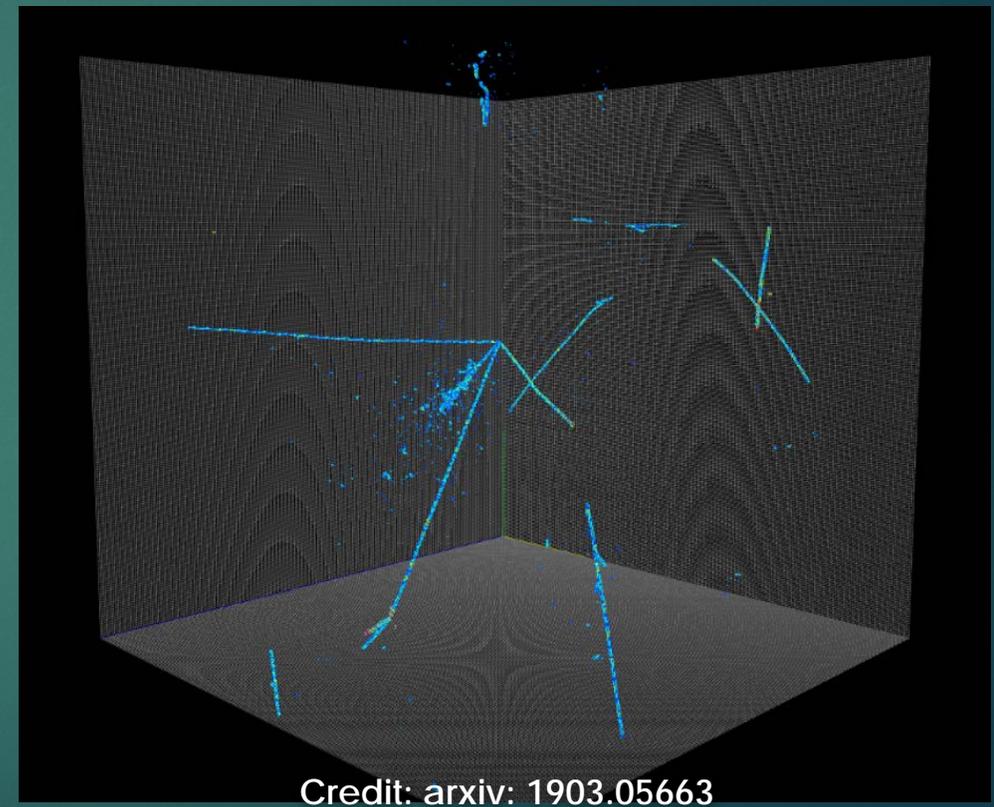
- Pixels come at a “cost” of higher channel count
 - Example: 2 meter x 2 meter readout
 - 3mm wire pitch w/three planes = 2450 channels
 - 3mm pixel pitch = 422,000 channels (4mm pixels 250K ch.)
- A pixel solution requires innovation in the readout electronics:
It needs to be motivated by increased physics reach and must meet heatload restrictions inherent in a 100X higher channel count.
- **Requires an “unorthodox” solution**



Capturing data w/o compromise and maintaining the intrinsic 3-D quality is an essential component of all Lar TPC readouts!



2D-Projective
Readout



3D-Pixel Readout

Dave Nygren's "unorthodox" solution

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- The Q-Pix electronics concept follows the "principle of least action"
 - **Don't do anything unless there is something to do**
 - Offers a solution to the immense data rates
 - Quiescent data rate (1 to 50 Mb/s/Mod TBD)
 - Allows for the pixelization of massive detectors
- Q-Pix offers an innovation in signal capture with a new approach and measures **time-to-charge:(ΔQ)**
 - Preserves the detailed waveforms of the LArTPC
 - Attempts to exploit ^{39}Ar to provide an automatic charge calibration
- **"Novelty does not automatically confer benefit"**
 - Much for a Consortium to explore.

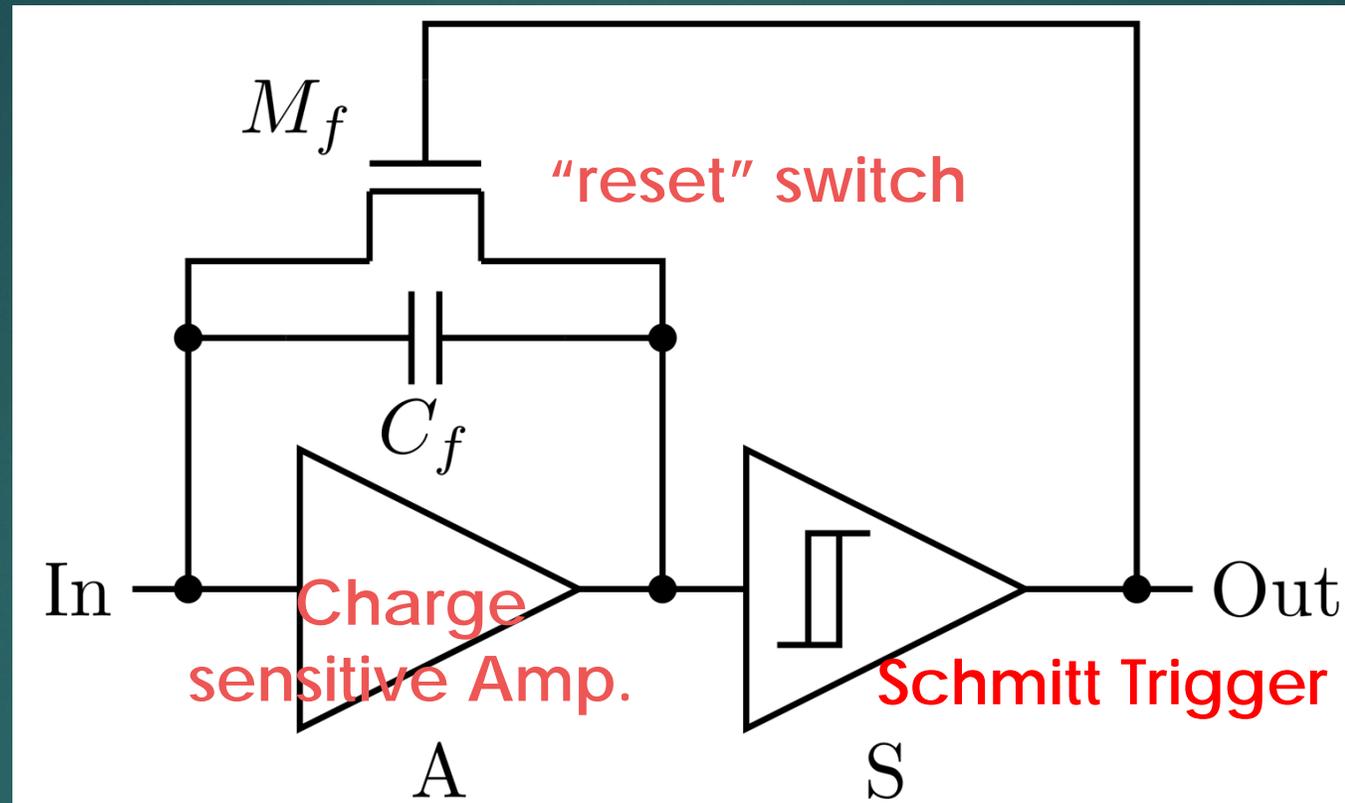
- Four central ideas being worked on
 - **Physics Simulations:** Quantify the conferred benefit of pixel vs. wire readout and the requirements of the ASIC design
 - **CIR Input:** all extraneous leakage current at the input node needs to be small (aA)
 - **Clock:** $\delta f/f \sim 10^{-6}$ per second
 - **Light Detection:** Exploring new ideas using photoconductors on the surface of the pixels

Readout System Development Work in Progress

Front End Electronics - Next section of this talk.

ASIC Back End / System Level readout & control
– see Gary Varner's talk.

Q-Pix: The Charge Integrate-Reset (CIR) Block

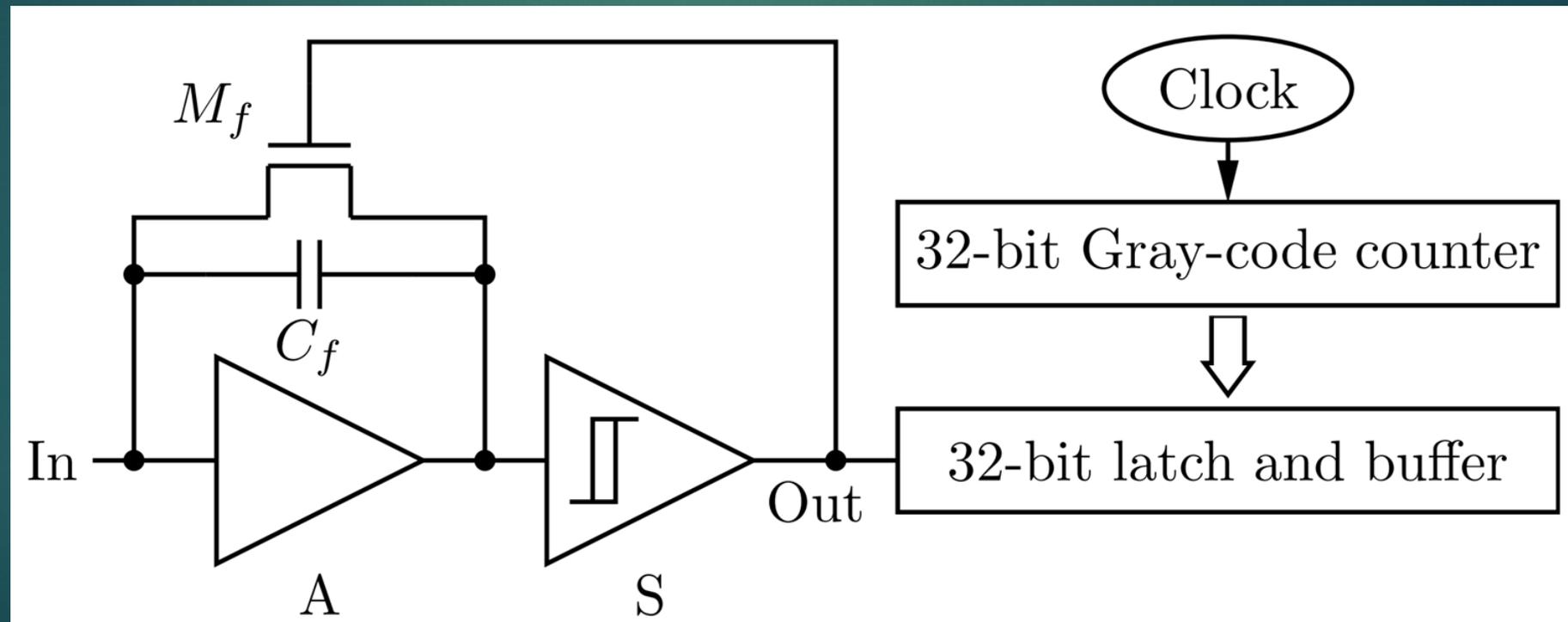


Charge from a pixel (In) integrates on a charge sensitive amplifier until a threshold ($V_{th} \sim \Delta Q / C_f$) is met which fires the Schmitt Trigger and causes a reset (M_f) and the loop repeats

Q-Pix: The Charge Integrate-Reset (CIR) Block

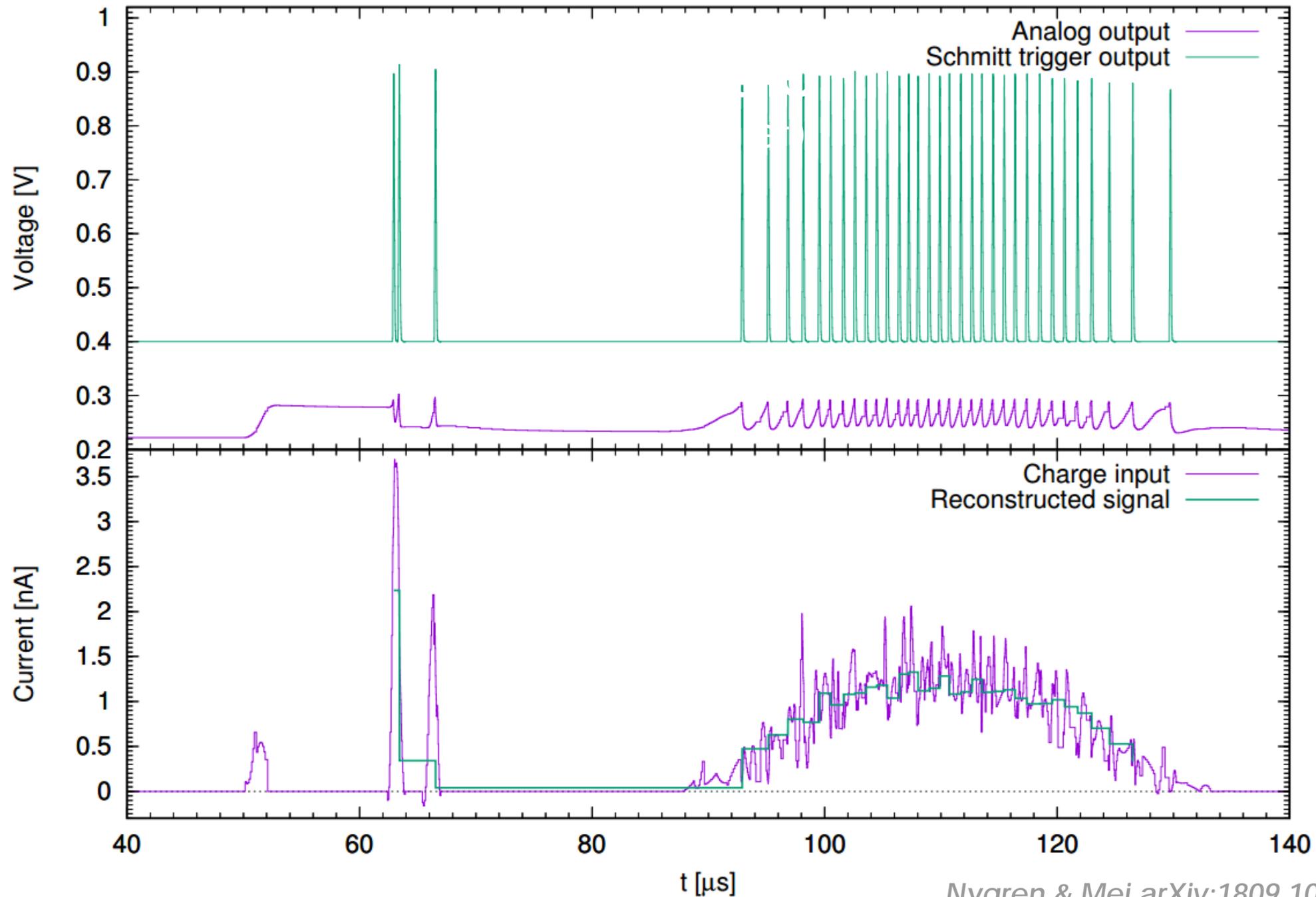
- Measure the time of the “reset” using a local clock (within the ASIC)
- Basic datum is 64 bits
 - 32 bit time + pixel address + ASIC ID + Configuration +

...



How it works...

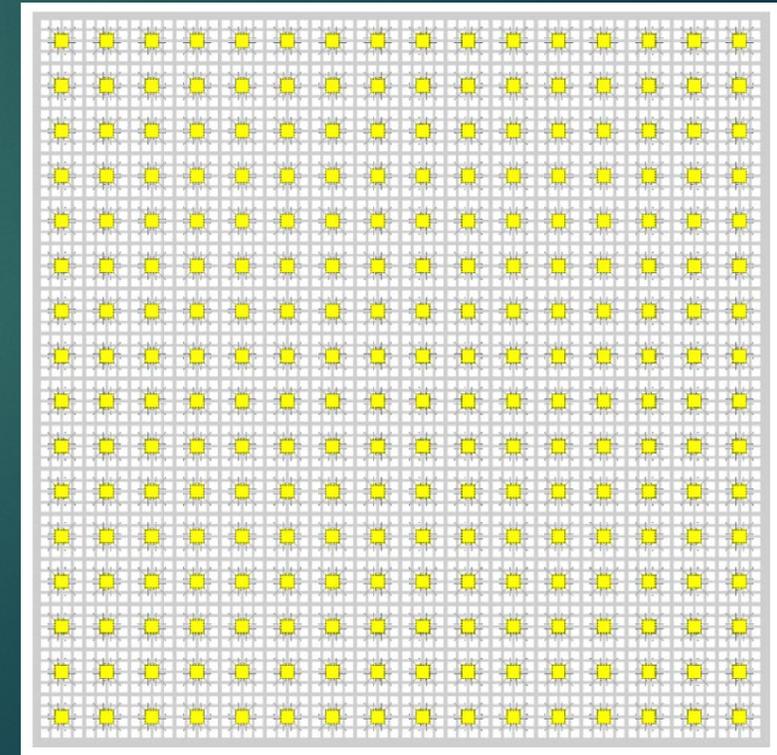
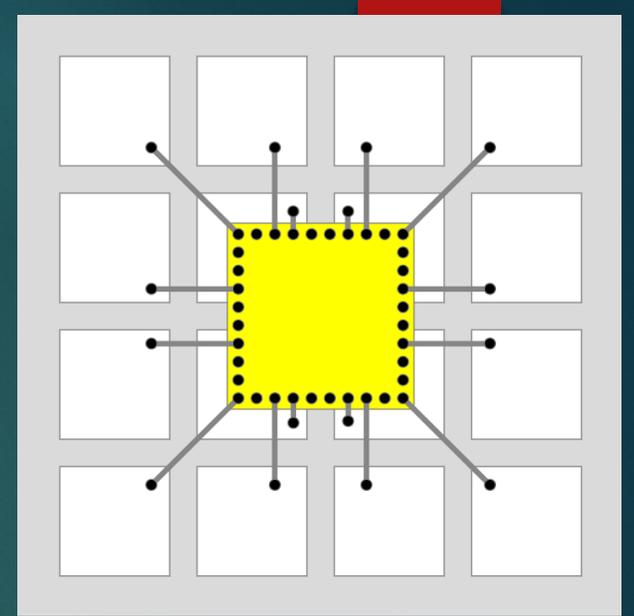
- Take the time difference between sequential resets
 - Reset Time Difference = RTD
- Total charge for any **RTD = ΔQ**
- RTD's measure the **instantaneous current** and captures the waveform
 - Small average current (background) = **Large RTD**
 - **Background from ^{39}Ar ~ 100 aA (625e⁻/second)**
 - Large average current (signal) = **Small RTD**
 - **Typical minimum ionizing track ~ 1.5 nA**
- Signal / Background ~ 10^7
 - Background and Signal should be easy to distinguish
 - No signal differentiation (unlike induction wires)



Q-Pix ASIC Concept

16- possibly more pixels / ASIC

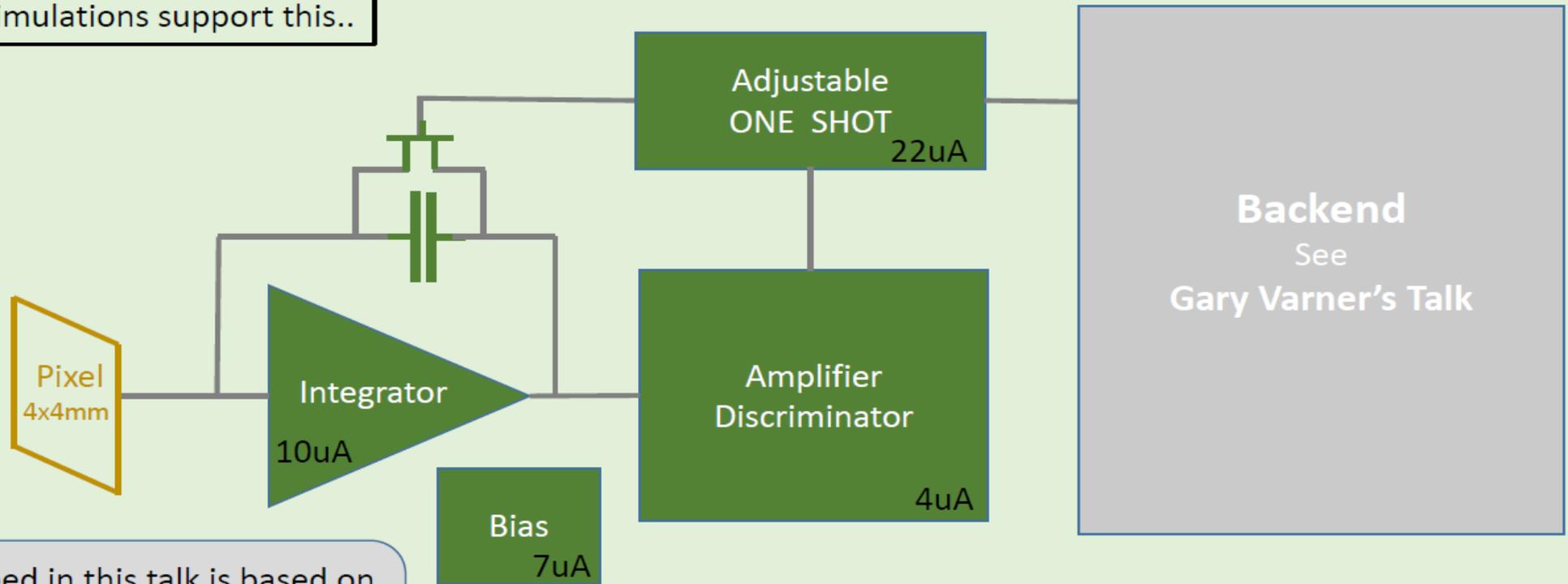
- 1 Free-running clock/ASIC
- 1 capture register for clock value, ASIC, pixel subset
- Necessary buffer depth for beam/burst events
- State machine to manage dynamic network, token passing, clock domain crossing, data transfer to network (many details to be worked out)
- **Basic unit would be a "tile" of 16x16 ASICs (4096 4mm x 4mm pixels)**
 - Tile size 25.6 cm x 25.6 cm



Front End Readout Development Underway

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Integrator at COLD temp
...estimated ENC < 100e
Analog simulations support this..



Work described in this talk is based on our "in house" **130nm Technology**. We intend to move to a **180nm technology** in the next few weeks.

Single (FE only) Channel POWER/ch	
Present FE Design	51μW
Projected final prototype FE	26μW

Under the hood... still in development stage

▶ Integrator (two stage)-

- ▶ PMOS Common Source Input referenced to an on chip 1V regulator to minimize PSRR followed by the
- ▶ Trans conductance amp.

Total Gain with 75fF MIM feedback (+reset strays) 17mV/fC

▶ Amplifier/Discriminator -

- ▶ Diff pair amplifier ~150mV/fC followed by differential pair comparator.

▶ Oneshot - D flip flop (DFF) with reset - switches programmable current that discharges a capacitor wired to reset the DFF. Sets the RESET width

"Q" output of DFF provides Integrator reset and signals the back end that a unit charge has been acquired.

Startup... & operation

- ▶ Since this is a fed back integrator it is necessary to startup with reset on to guarantee initial conditions across the integration cap.
- ▶ An external reset generator serves to prime the system for consistent behavior. For warm operation where the integrator leakage is high it will be helpful to have the external system generate resets ~ 20ms.
- ▶ Since Reset occurs for a specific integrated charge, ΔQ , it's important to understand that a residue will remain on the integration cap when a non integer charge is processed.

Threshold Effects of a Unit Charge sensing FE

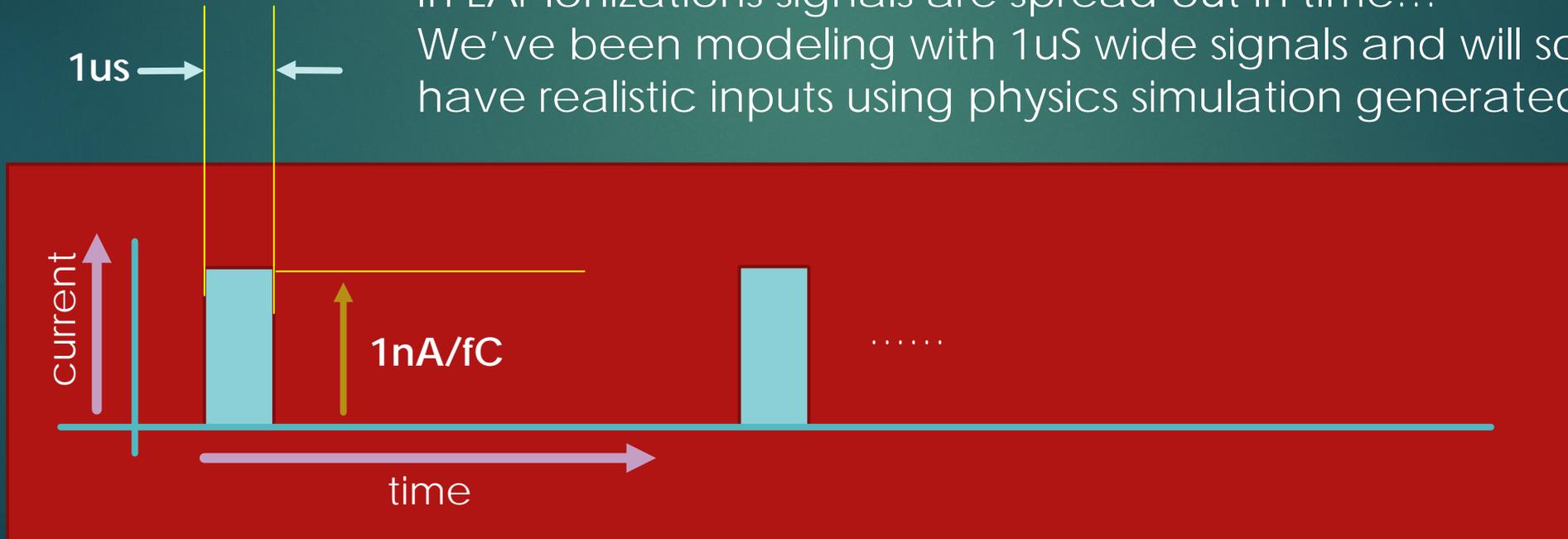
16

In **Qpix**: The number of outputs (resets) produced by an input pulse is proportional to the number (programmable) unit charges sensed by the front end.

→ The timing of the arrival of these sensed unit charge pulses is used to describe details of the ionizing track.

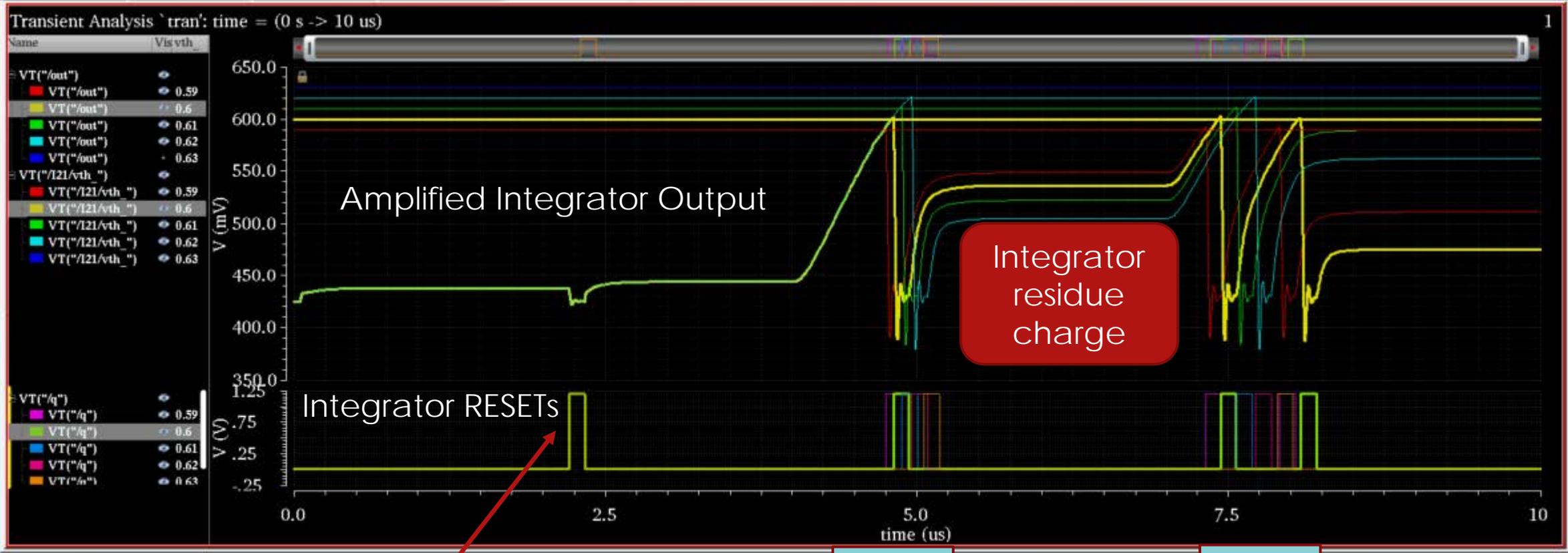
In LAr Ionizations signals are spread out in time...

We've been modeling with 1 μ S wide signals and will soon have realistic inputs using physics simulation generated data.



Multiple Runs Ramping Threshold for 1fC input

Two, 1fC, Input Pulses Generate Three integrator reset well below 1fC threshold



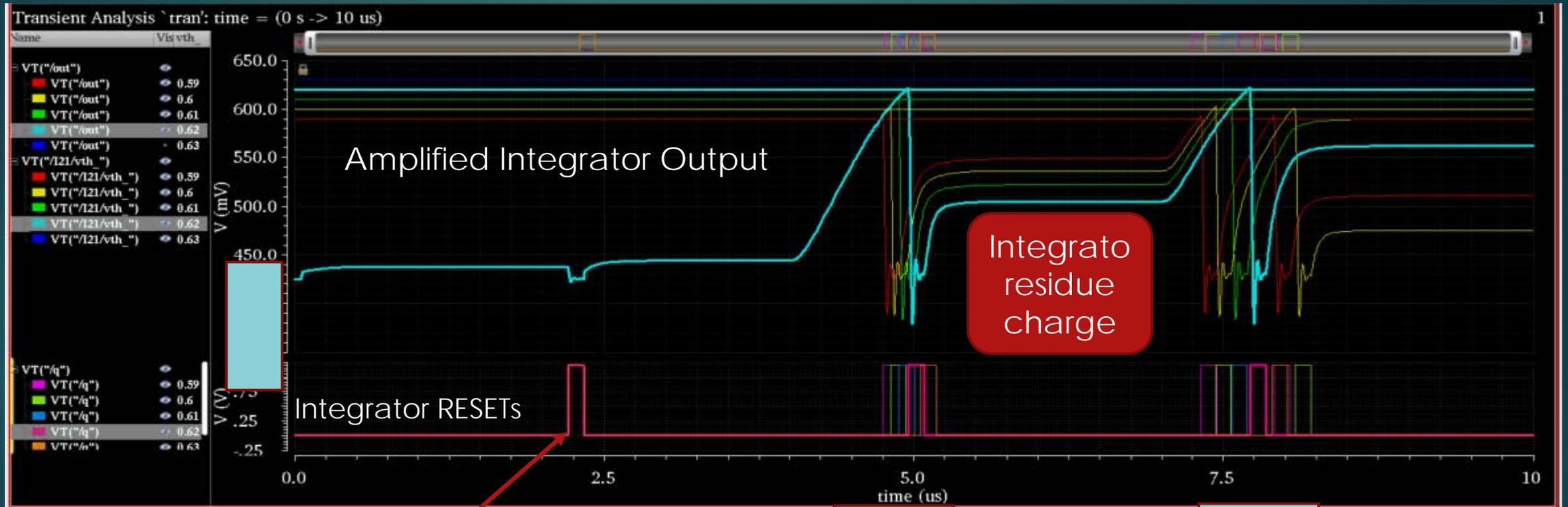
Externally Generated an external reset At the beginning

1fC Input charge

1fC Input charge

Multiple Runs Ramping Threshold

Two, 1fC Input Pulses Generate Two reset pulses near 1fC threshold, Integrator residue still fairly large.



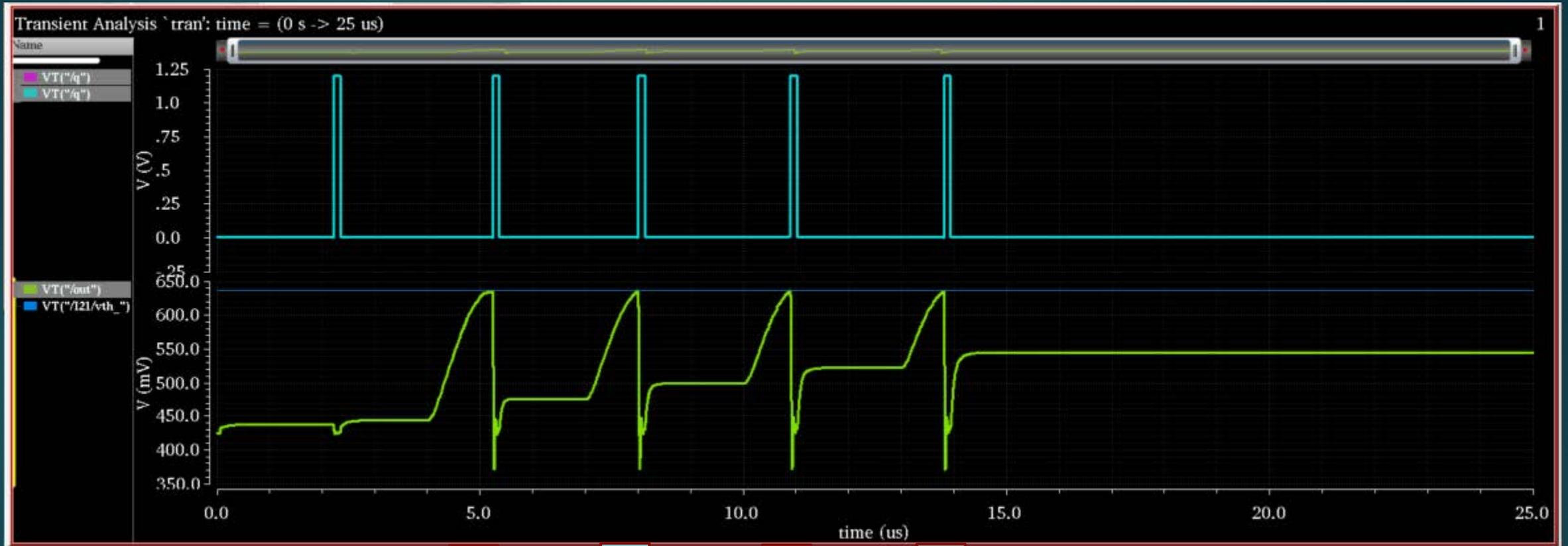
Externally Generated an external reset At the beginning

1fC Input charge

1fC Input charge

4 equal Amplitude Pulses 1 fC

19



1 fC

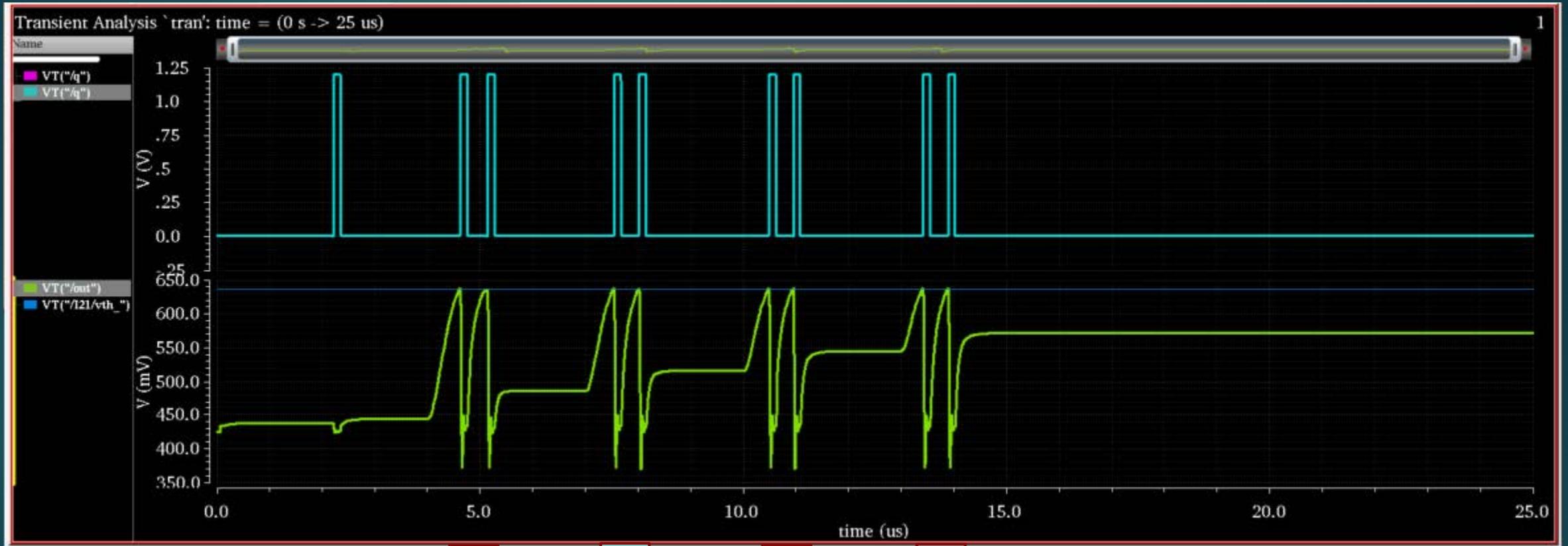
1 fC

1 fC

1 fC

4 equal Amplitude Pulses 2 fC

20



2 fC

2 fC

2 fC

2 fC

4 equal Amplitude Pulses 3 fC

21



3 fC

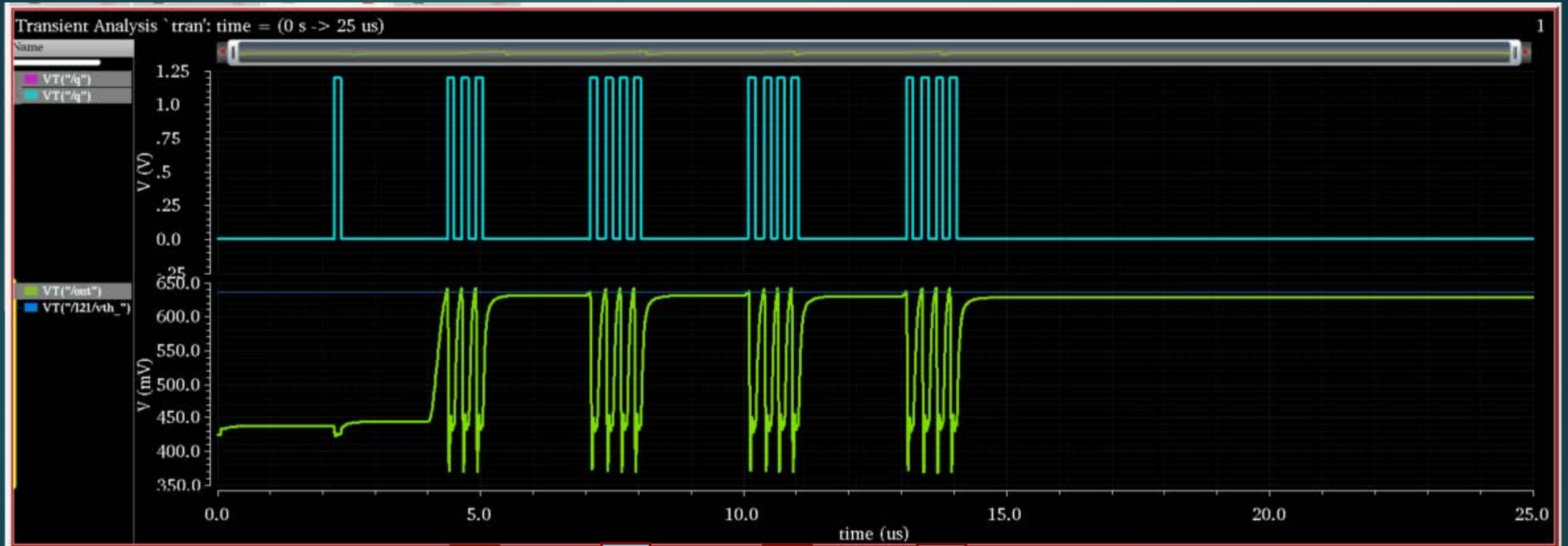
3 fC

3 fC

3 fC

4 equal Amplitude Pulses 4 fC

22



4 fC

4 fC

4 fC

4 fC

Low Power Front end Design Status

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We have been studying circuit configurations developing candidate blocks and learning how to minimize power and are ready to input physics generated ionizations provided by UTA.

- ▶ The 130nm process we are using is similar to the target 180nm process being used in other pixel developments and intended for the prototype FE development. A signed NDA for the target process was recently acquired. Work presently underway will give us a head start in the implementation of the prototype FE design in the target process.
- ▶ A prototype submission will answer many important questions, most importantly about the integrator leakage current at Liquid Argon Temperatures.
- ▶ We expect to be ready to submit a multi-ch. prototype in the Spring 2020.