



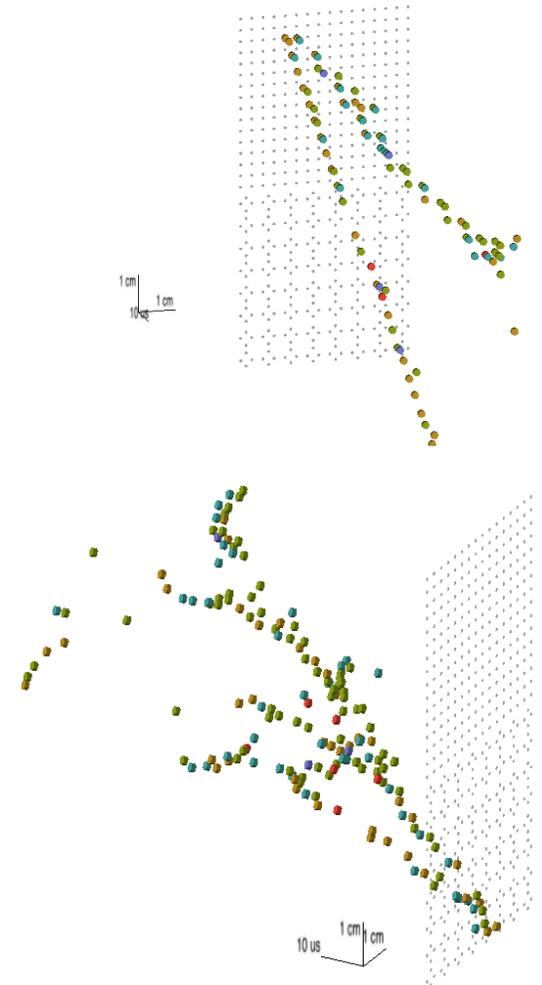
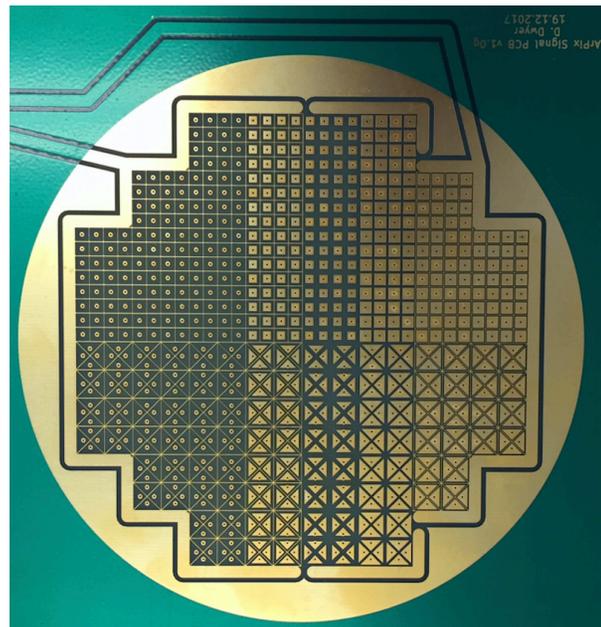
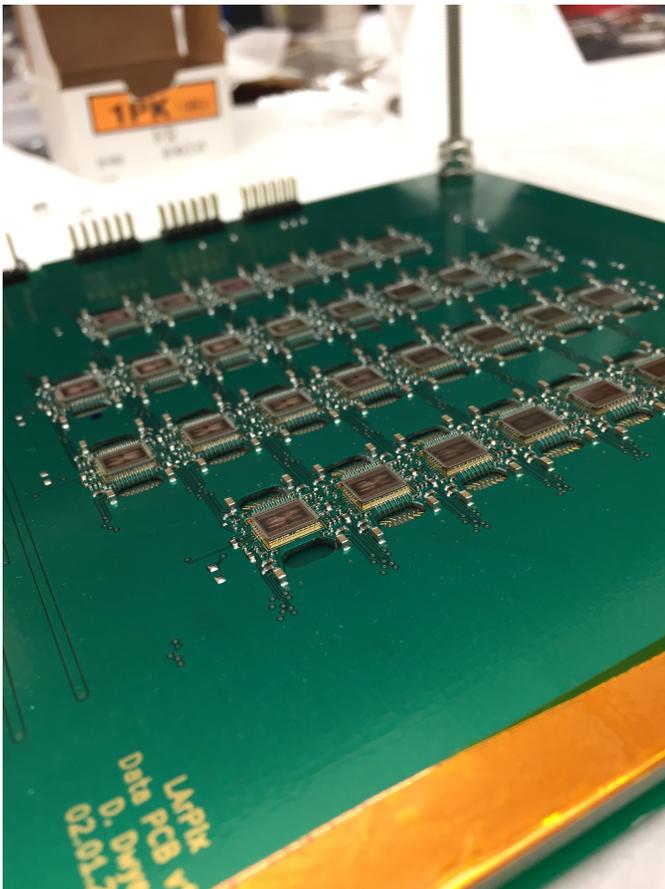
LArPix:

Pixelated Charge Readout for Large LArTPCs

Dan Dwyer (LBNL)

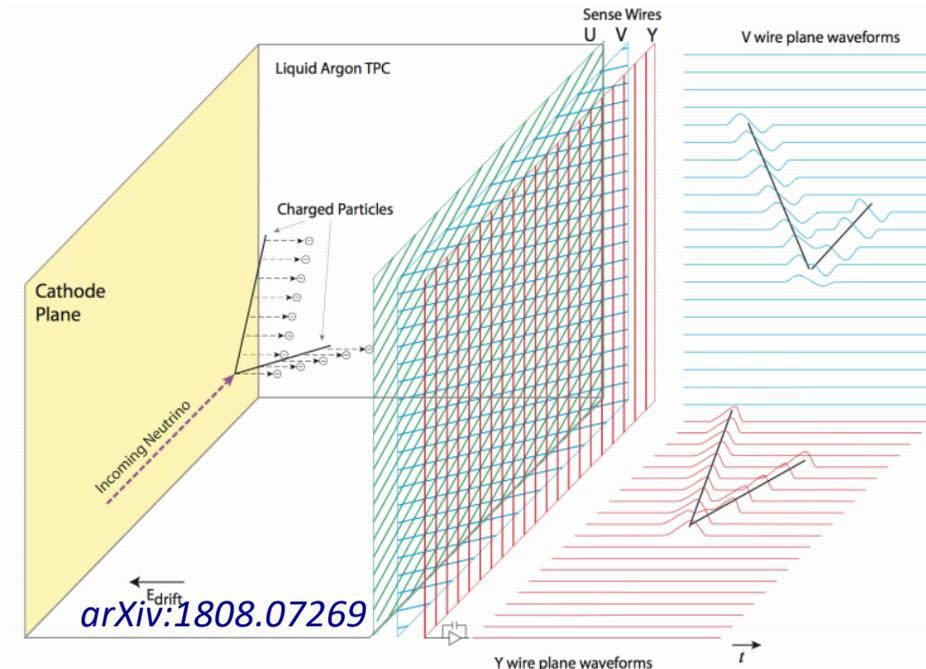
DUNE Module of Opportunity Workshop

Nov. 13, 2019



LArTPC Charge Readout

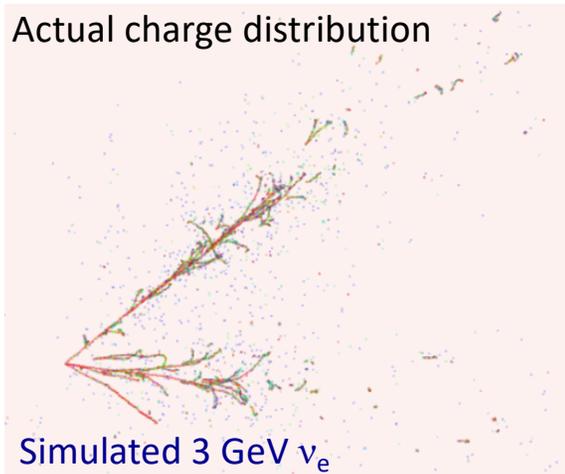
Existing LArTPCs infer 3D signal from three 2D views:



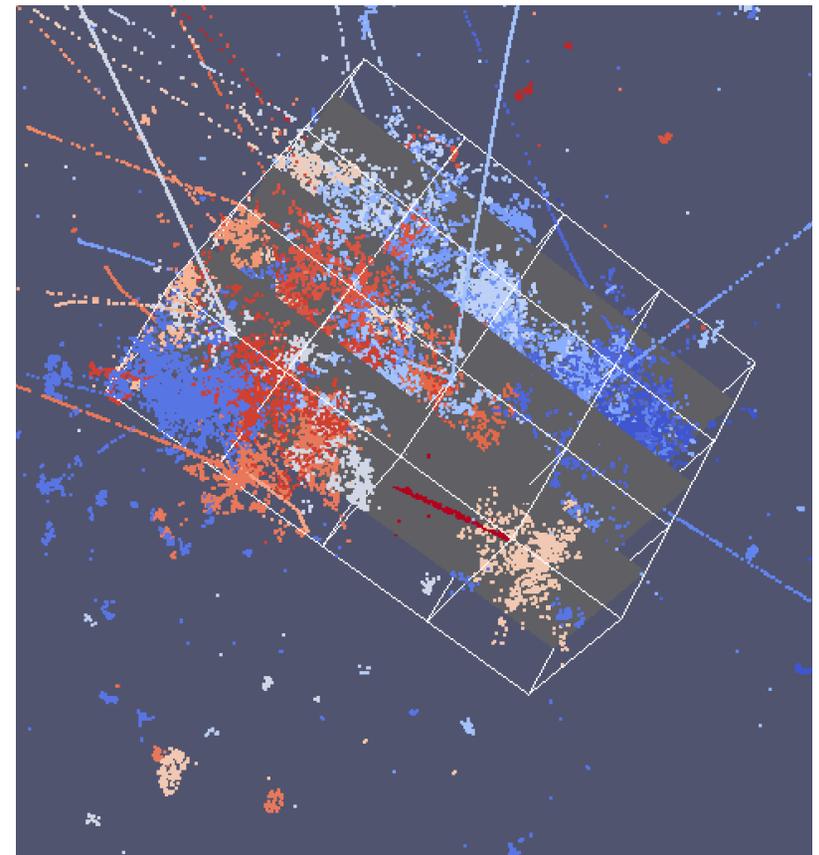
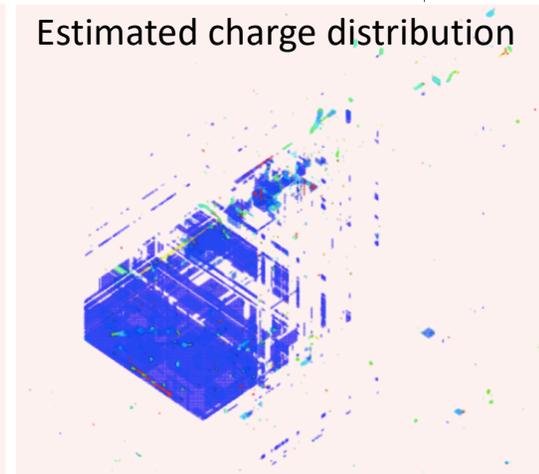
DUNE Near LArTPC:
High neutrino rate
exacerbates ambiguities.

Ambiguities in projective wire readout:

Actual charge distribution



Estimated charge distribution

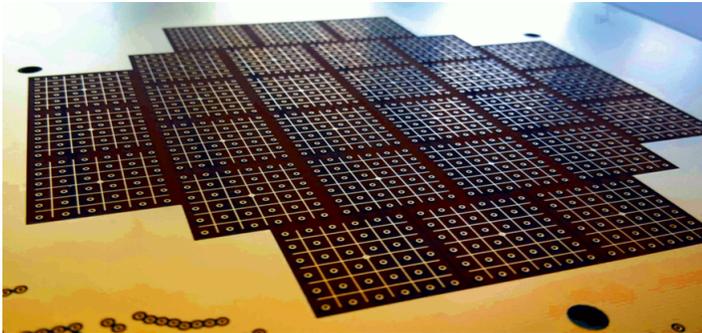


Example neutrino signals from one LBNF spill

A True 3D LArTPC?

Pixel Readout Development

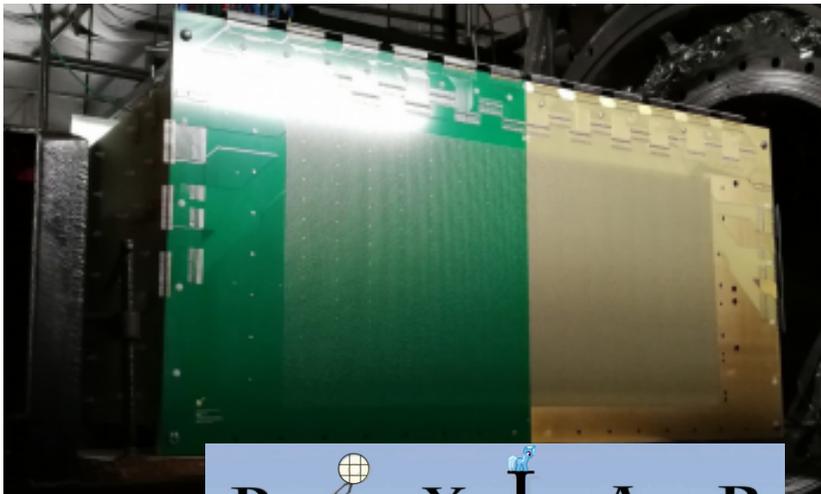
Demonstration of pixel sensor feasibility (Bern/ArgonCube)



ArgonCube 2x2 Demonstrator



Progress with in-beam tests (LArIAT/PixLAR)



Critical Technology: Pixel electronics

- Low-power, low-noise, cryo-compatible
- $O(10^5)$ channels / m^2

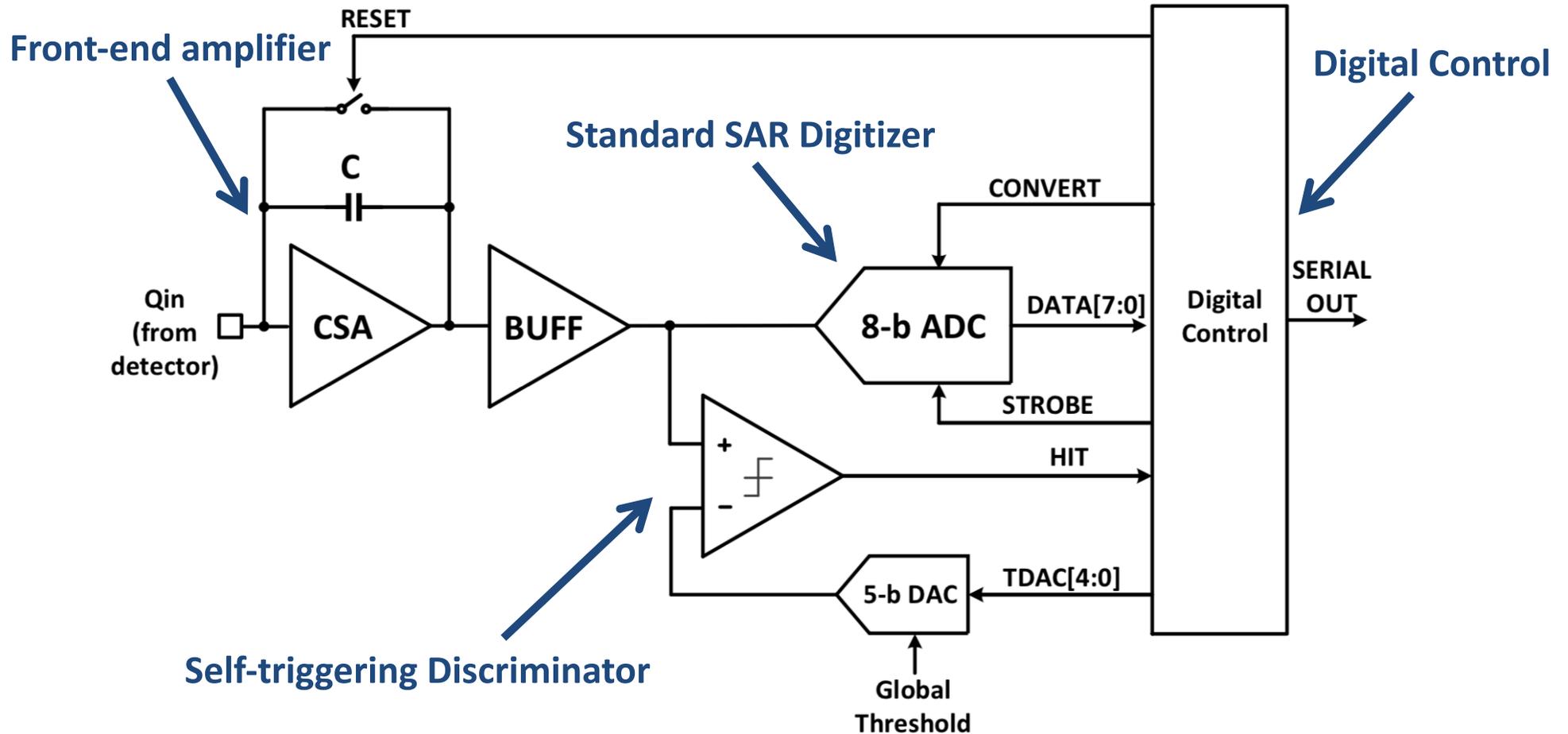
→ Focus of LBNL effort



LArPix Design

True 3D readout: A dedicated front-end channel for every pixel

Approach: Amplifier with Self-triggered Digitization and Readout

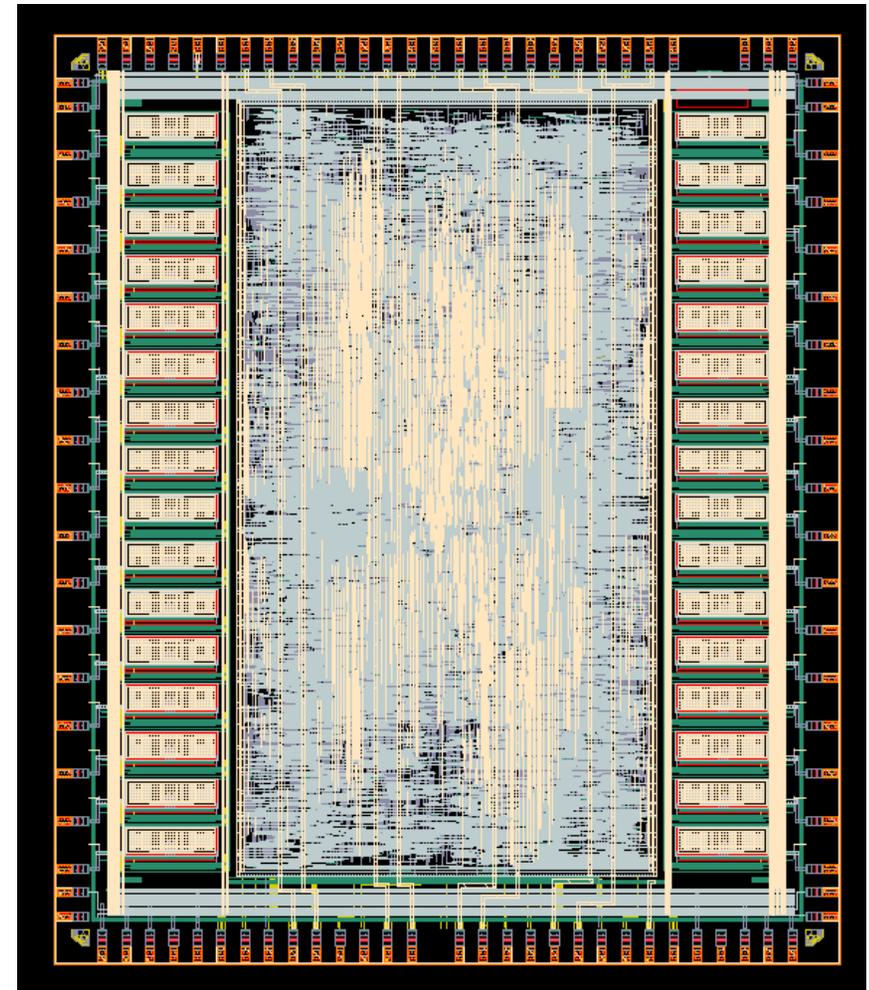
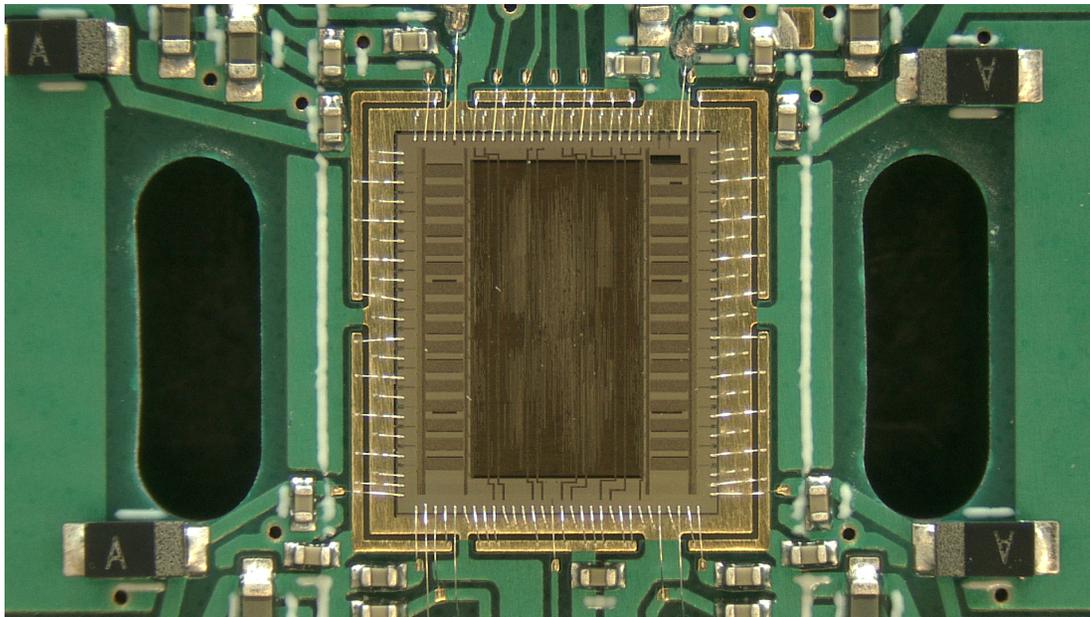


Achieve low power: avoid digitization and readout of mostly quiescent data.

LArPix-v1: ASIC Development

LArPix-v1 ASIC:

- Dec. 2016: Design began
- June 2017: Submitted for fabrication
- Oct. 2017: First chips, test boards @ LBNL
- Dec. 2017: Bench tests successfully completed
- Jan. 2018: Assembled sensor, integrated LArTPC



Process: 180nm bulk CMOS

Design and testing team @ LBNL:

D. Dwyer, C. Grace, M. Garcia-Sciveres,
A. Krieger, D. Gnani, T. Stezelberger,
S. Kohn, P. Madigan, H. Steiner

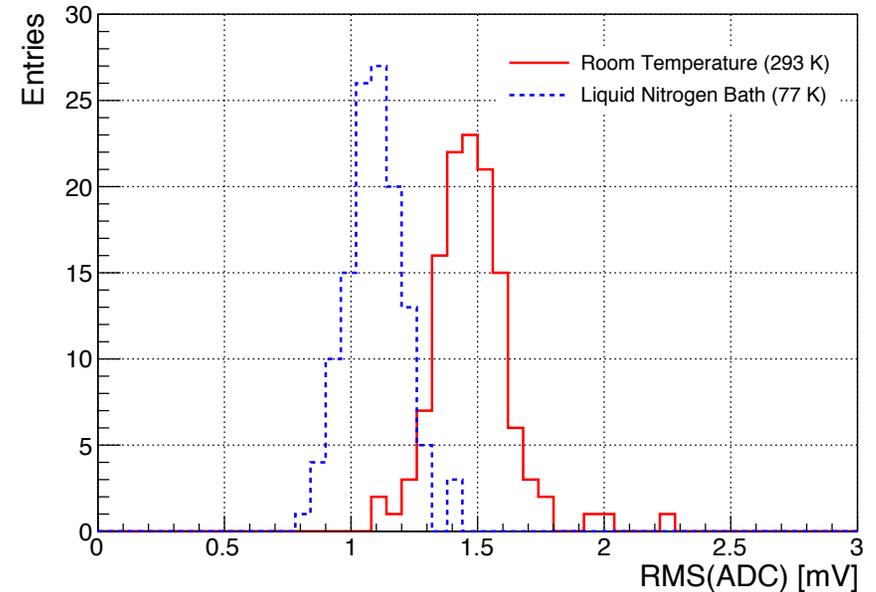
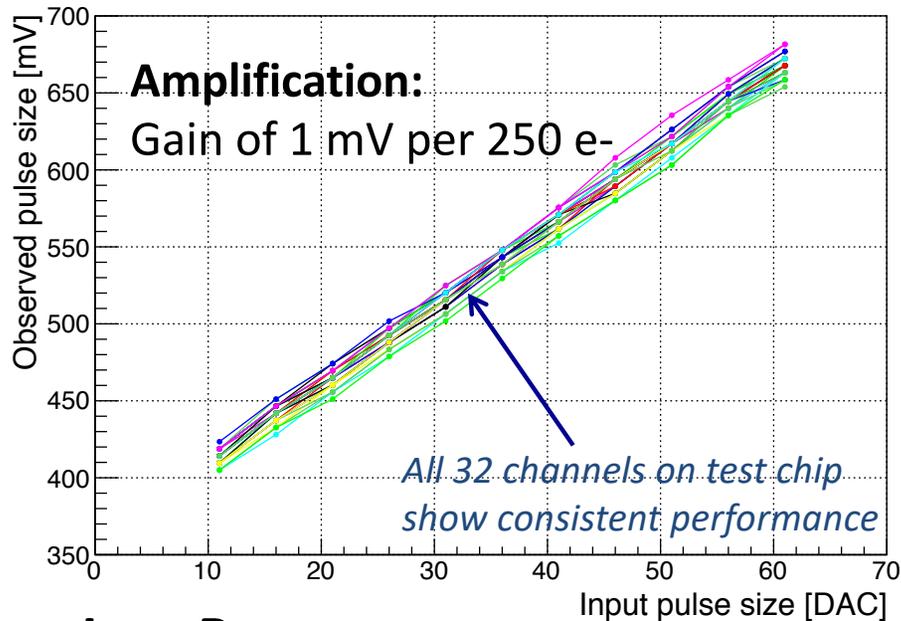
Initial Bench-testing Results

Demonstrated low-noise low-power cryogenic amplification, digitization, and readout:

Low Noise:

~1.5 mV (~375 e-) at room temp

~1.1 mV (~275 e-) in LN² bath



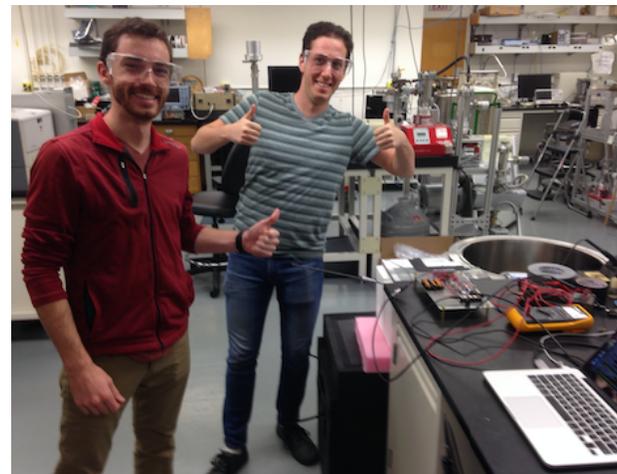
Low Power:

Average power for 128-channel readout:

- Analog: 24 μ W/channel
- Digital: 38 μ W/channel
- **Total: 62 μ W/channel**

Performance exceeded design targets:

- < 500 e- ENC
- < 100 μ W/channel

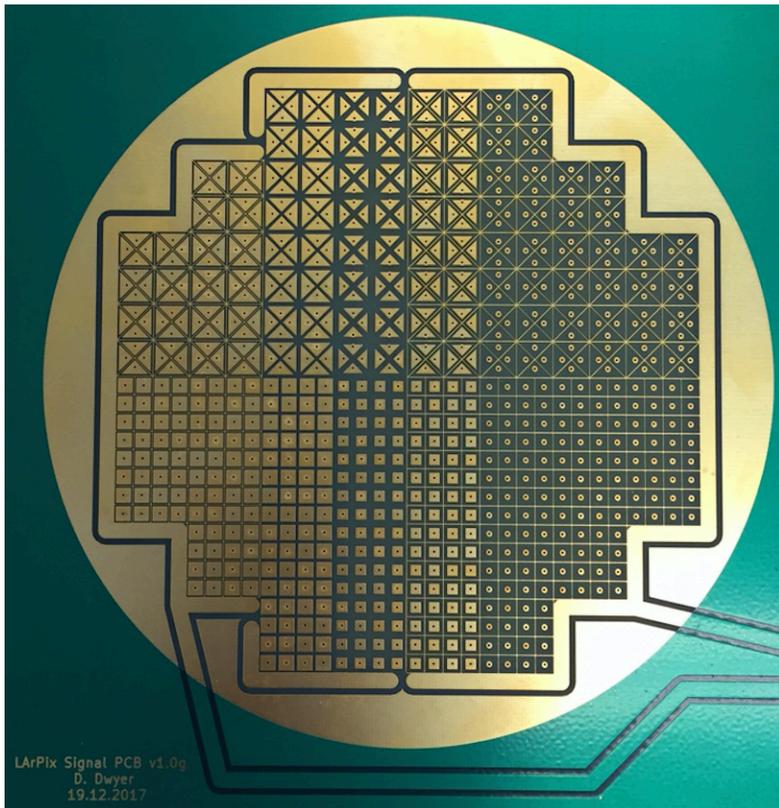


P. Madigan, S. Kohn: drove testing effort

LArPix-v1: Readout Assembly

Pixel Board:

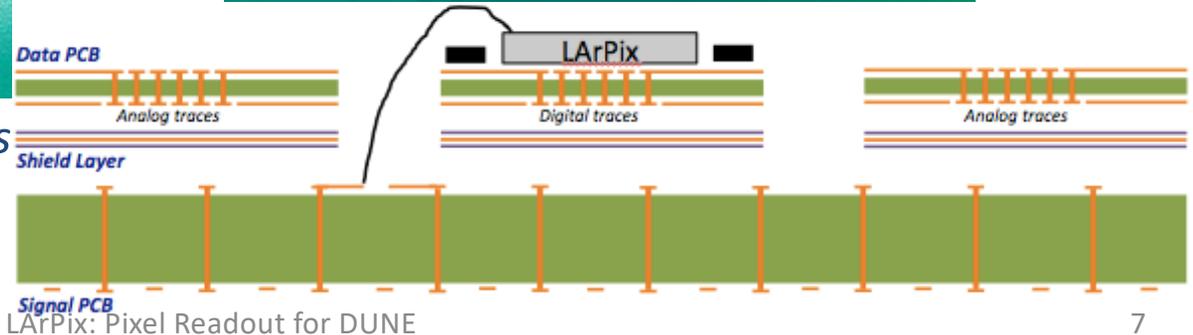
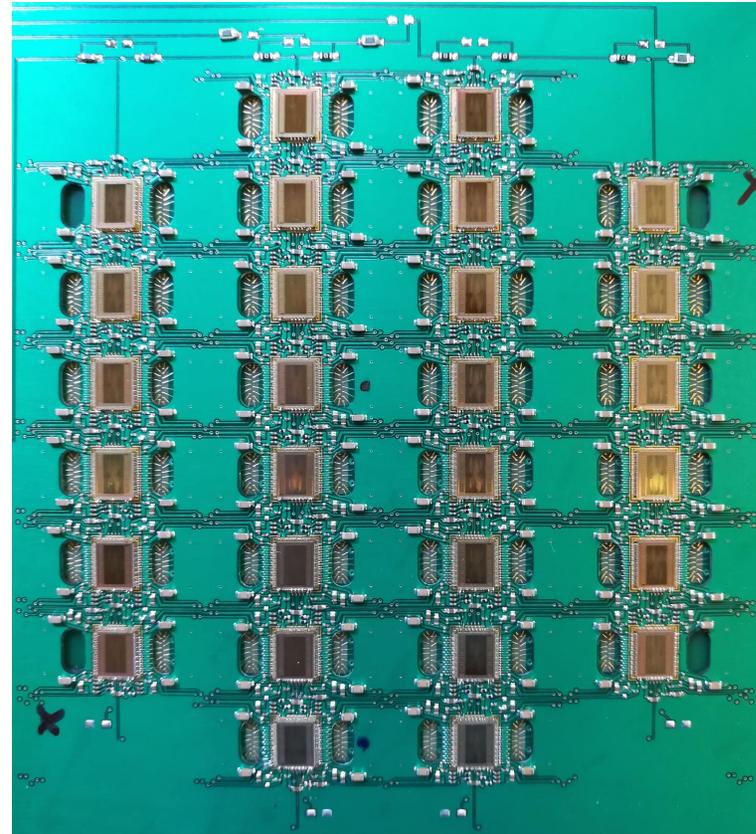
Standard printed circuit board
 Fits Bern Pixel Demonstrator TPC
 10 different pixel geometries



10 cm diameter, 3mm pitch, 832 pixels

Complete readout assembly

28-chip LArPix data board sandwiched to pixel board

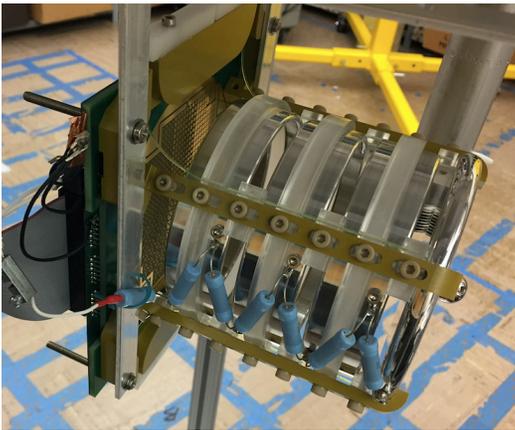


LArTPC Operation

Demonstration of cosmic ray detection at increasing scales

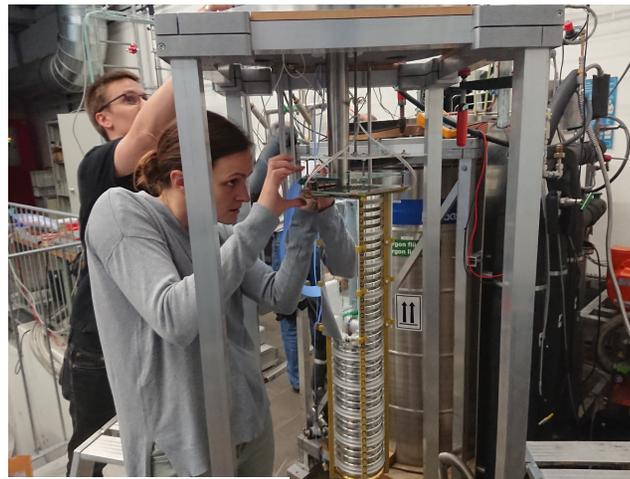
Feb 2018:

128-pixel system @ LBNL
10 cm drift, 200 V/cm



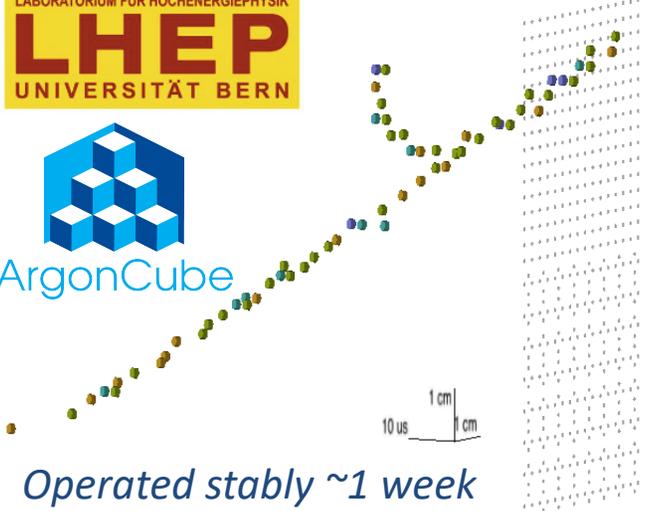
Apr 2018:

512-pixel system @ Bern
60 cm drift, 1 kV/cm



LABORATORIUM FÜR HOCHENERGIEPHYSIK
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ArgonCube

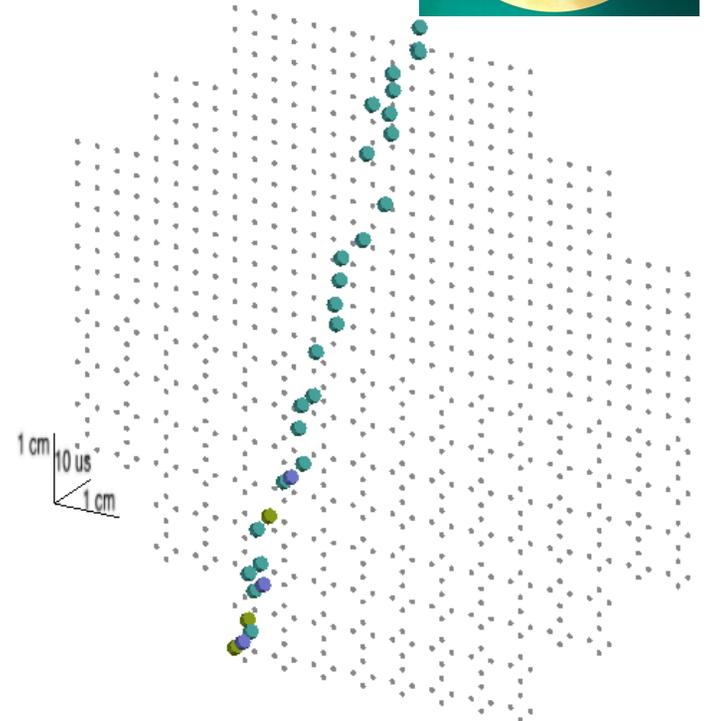
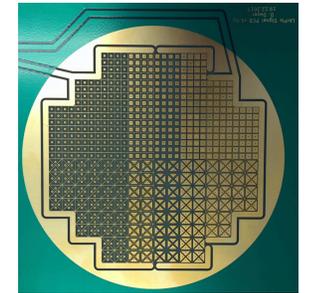


Operated stably ~1 week

LArPix: Pixel Readout for DUNE

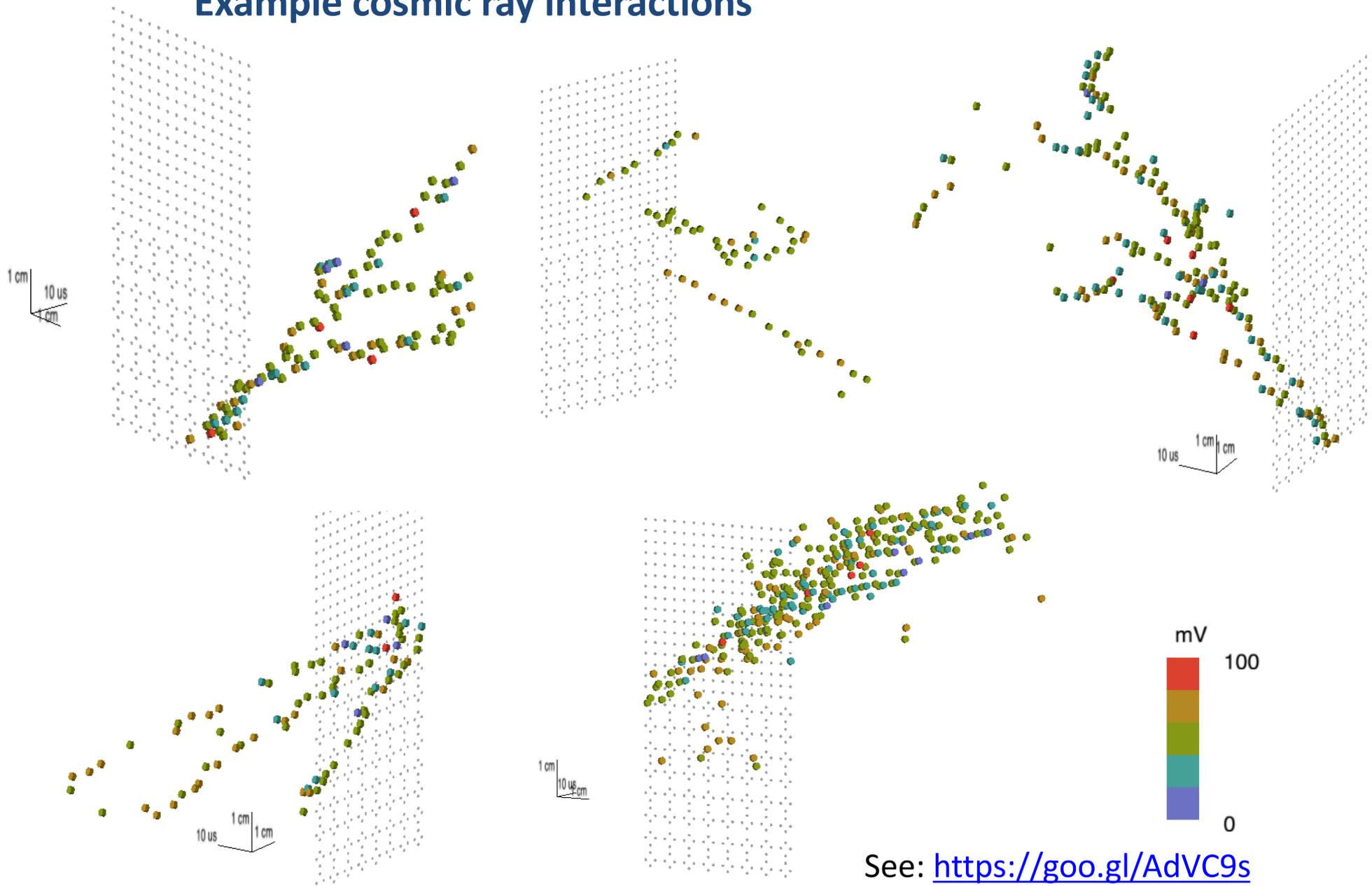
May 2018:

832-pixel system @ LBNL



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Example cosmic ray interactions



See: <https://goo.gl/AdVC9s>



LArPix-v1 Raw Data

Brief description of raw LArPix-v1 data

54-bit hit record: Pixel ID, ADC value, timestamp, status bits

Each colored point shows one self-triggered hit

- Hit x, y position from pixel location (3 mm precision)
- Position along drift given by timestamp (200 ns precision)
- Color shows hit amplitude (2 mV precision)
- ADC value converted to mV based on initial calibration

No filtering, manipulation applied to raw data.

→ Noise is very low: $>20:1$ SNR for MIPs

Comment on LArPix data rates:

Pixel self-triggering substantially reduces data volume:

LArPix operation @ Bern:

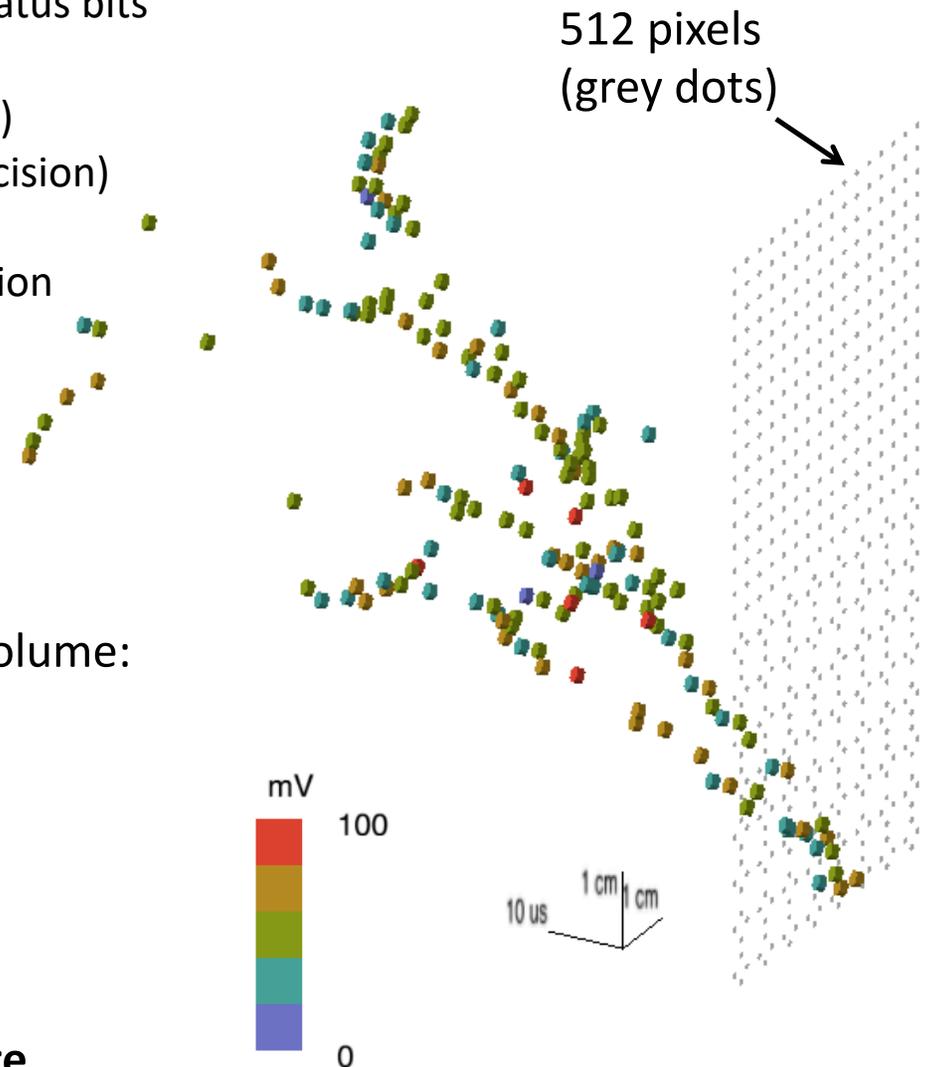
60cm drift at surface

512 pixels, ~ 0.3 Hz/pixel → **~ 3 kB/s total rate**

DUNE Near Detector:

50cm drift underground

8M pixels, ~ 0.01 Hz / pixel → **~ 2 MB/s total rate**

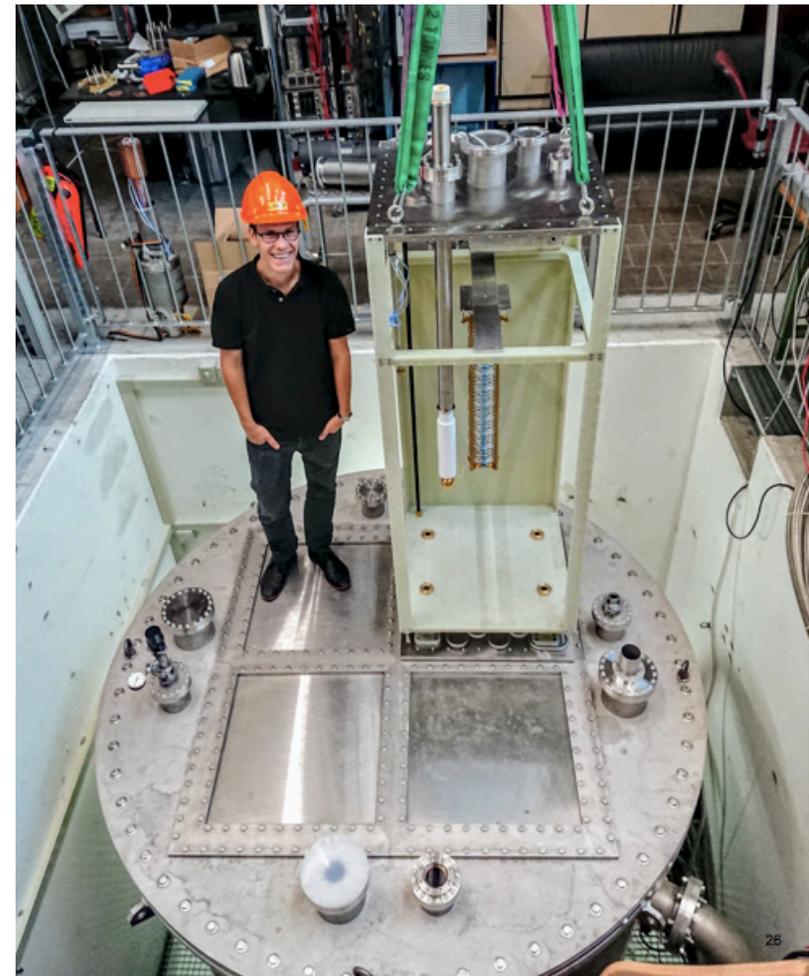
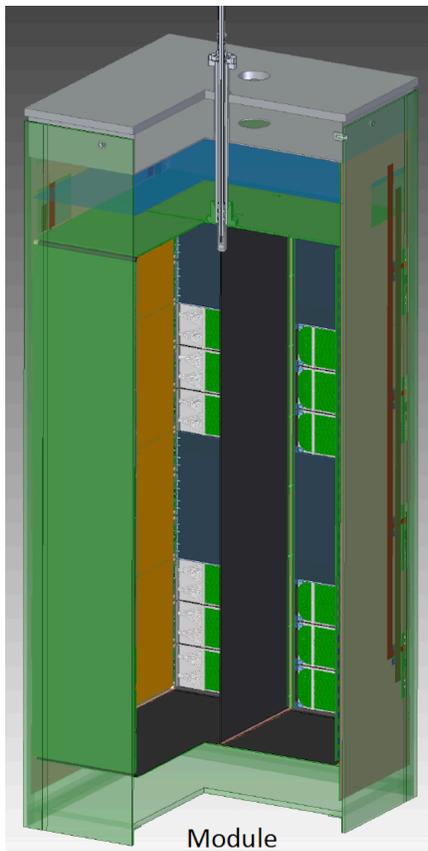


Next Step: Scalability

Demonstrate system scalability in large LArTPC: ArgonCube 2x2 Demonstrator

4 modular LArTPCs
Total active mass: ~ 3 ton
Readout area: 6.4 m^2
400k pixels, 6.3k ASICs

System currently under construction.
Demonstrator for DUNE Near Detector





DUNE Pixel Readout Group

Team effort to realize the LArPix system for the ArgonCube 2x2 Demonstrator



^b
UNIVERSITÄT
BERN



Weekly meetings focused on design and production for the ArgonCube 2x2 Demonstrator
→ Let me know if you are interested in joining the effort!



LArPix-v2: ASIC Improvements

Exploring LArPix-v2 for scalable assembly and improved physics performance:

v2 design completed (Sep. 2019)

New readout scheme to address system reliability (Hydra I/O)

Improved layout (more compact, better shielded)

Internal biasing (more tunable, simpler PCB)

64 channels per ASIC (x2 LArPix-v1)

Improved signal threshold range

Reduced deadtime

Enhanced triggering functionality

Integrated monitoring system

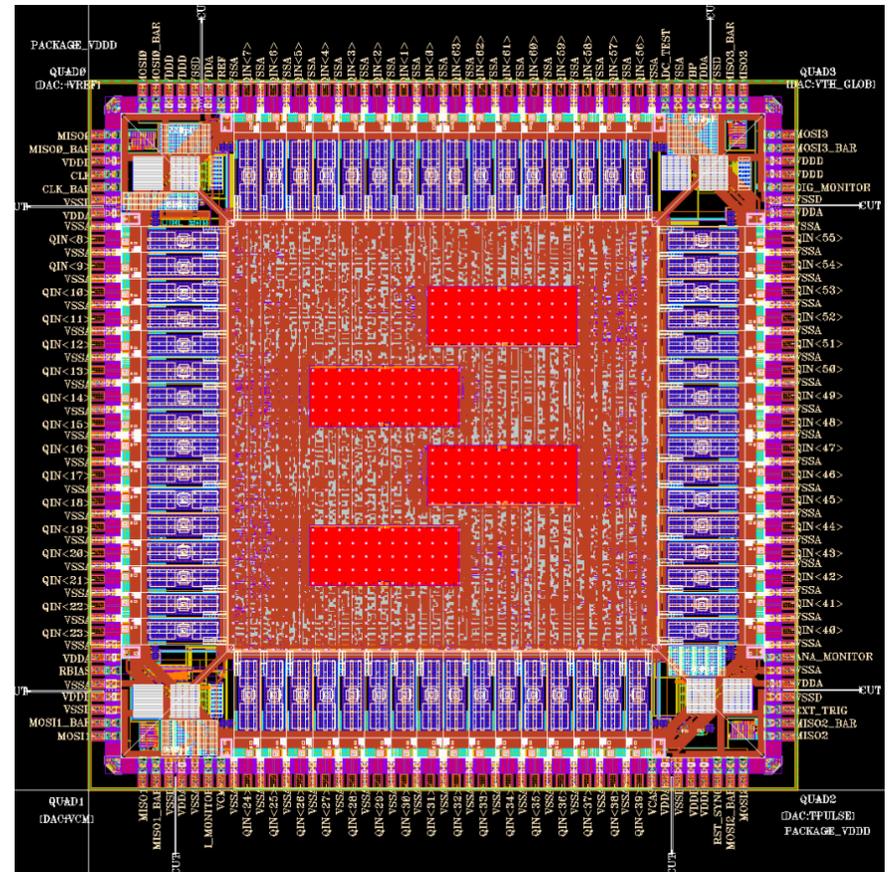
Improved integrated front-end pulser

Compact SRAM-based FIFO

Improved hit noise rejection, deglitching

Lower-noise differential CMOS I/O option

Expect to receive v2 ASICs in Dec. 2019

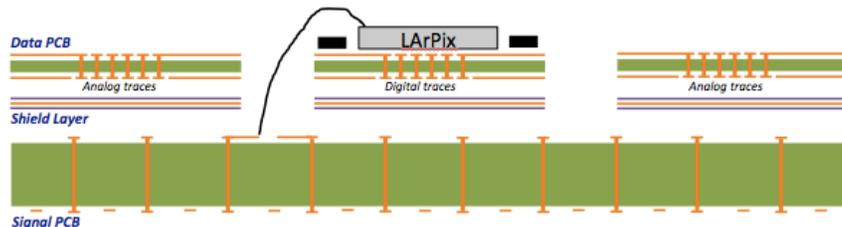
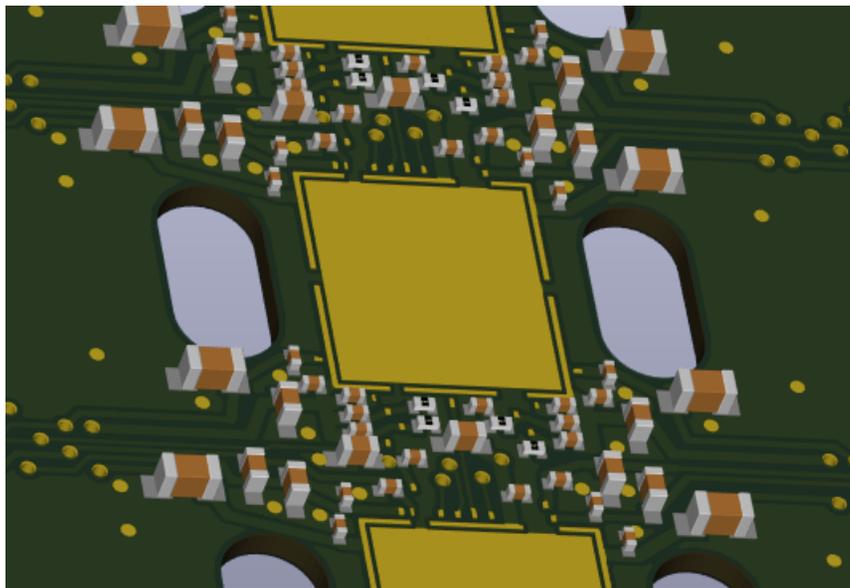


LArPix-v2: Pixel Tile

New modular pixel tile for ArgonCube 2x2 Demonstrator

Current v1 Pixel Tile:

- No active components, aside from v1 ASICs
- Chip-on-board attachment
- 3mm pixel pitch
- Very crowded layout
- Sandwich of two PCBs

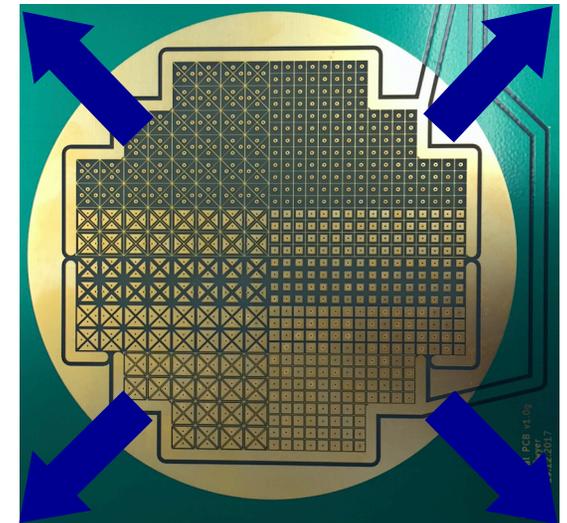
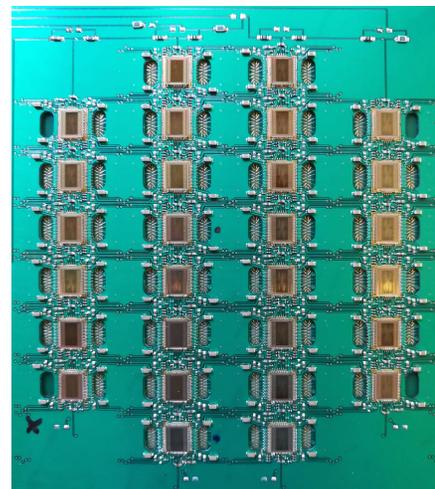


Modifications for v2 Pixel Tile:

- No active components, aside from v2 ASICs
- Packaged ASICs
- 4mm pixel pitch
- Many fewer passive components
- Single PCB
- Pixels edge-to-edge



→ *Planning on completely commercial production*



LArPix-v2 Pixel Tile Concept

Pixel Tile design for the ArgonCube 2x2 Demonstrator

Frontside:

- Grid of 80 x 80 pixels

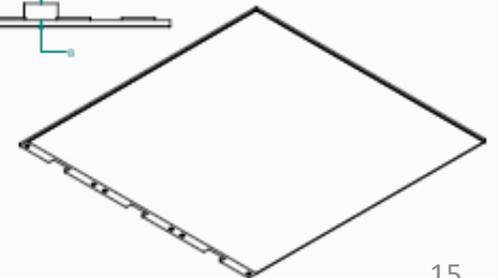
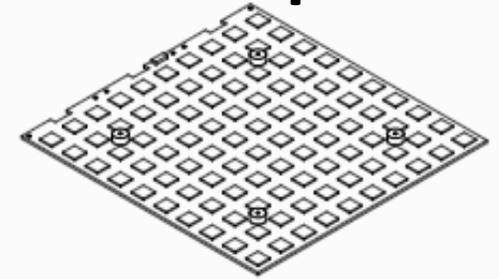
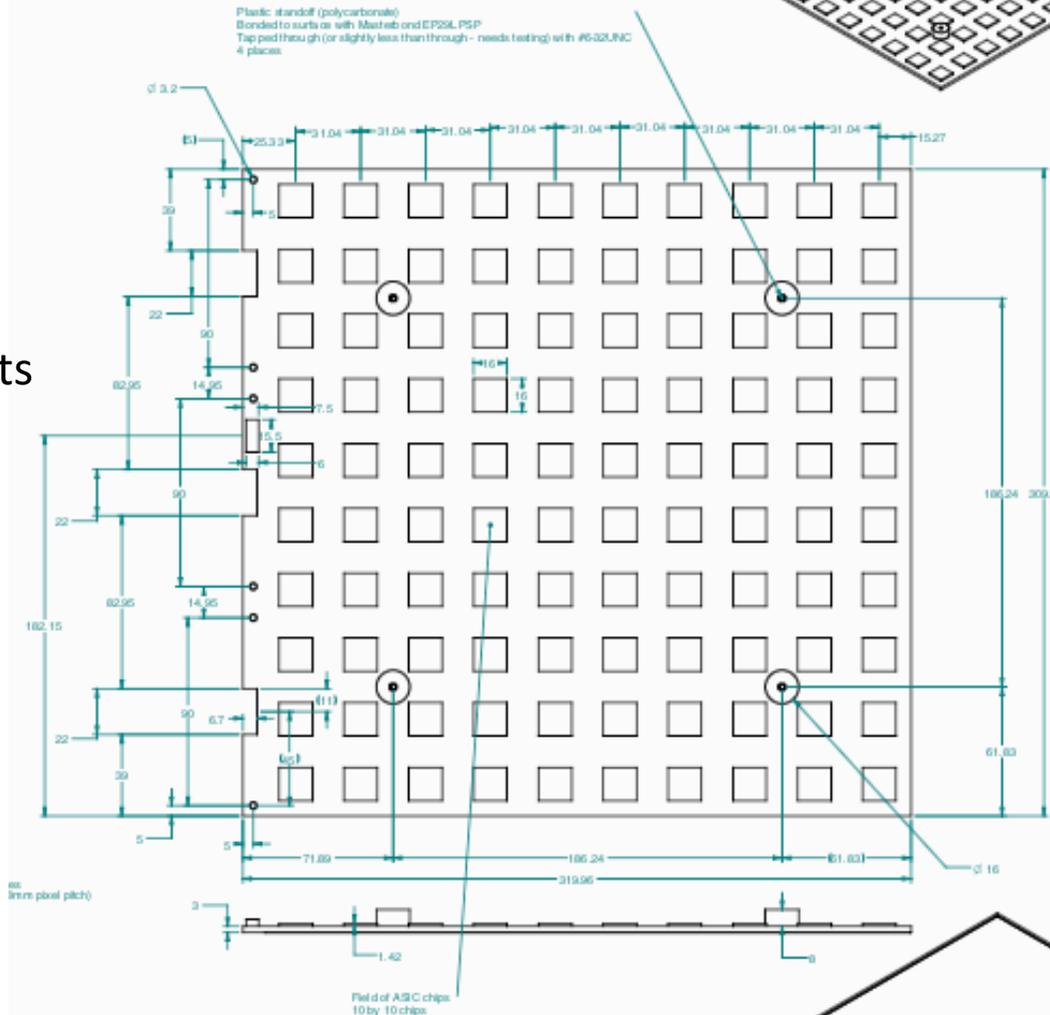
Backside:

- Grid of 10 x 10 LArPix ASICs
- 4 mechanical attachment points

'Inactive' edge:

~1 cm strip at edge for services:

- Pixel Tile cable connector
- Routing for LArPix ASICs
- Mount point for light system



Mechanical layout courtesy of K. Skarpaas

LArPix-v1.5

Recently tested new pixel PCB Tile design using packaged LArPix-v1 ASICs

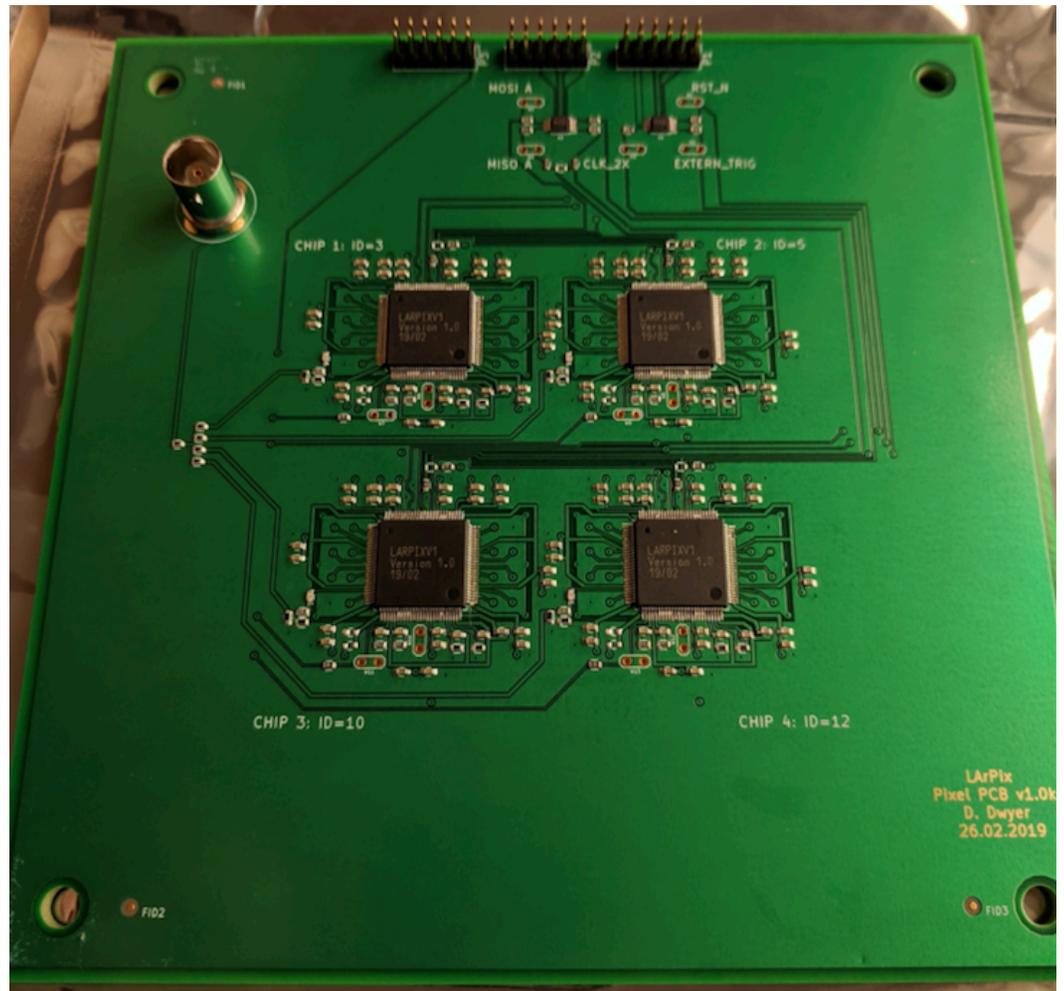
Provided integrated test of:

- v1 ASIC in QFP-100pin package
- Multi-layer pixel PCB construction
- Pixel tile assembly techniques
- Signal quality / performance
- System robustness in LAr

Provided advanced tests of many aspects of LArPix-v2 design.

Generally successful:

- No ASIC failure at cryo temp
→ *even with rapid thermal cycling*
- Increased digital-to-analog crosstalk for packaged v1 ASIC
→ *Mitigate in v2 using differential I/O*
- More likelihood of boiling for packaged ASIC relative to chip-on-board construction
→ *Exploring dependence on LAr depth, thermal coupling of ASIC to PCB*





LArPix-v2: Hydra I/O

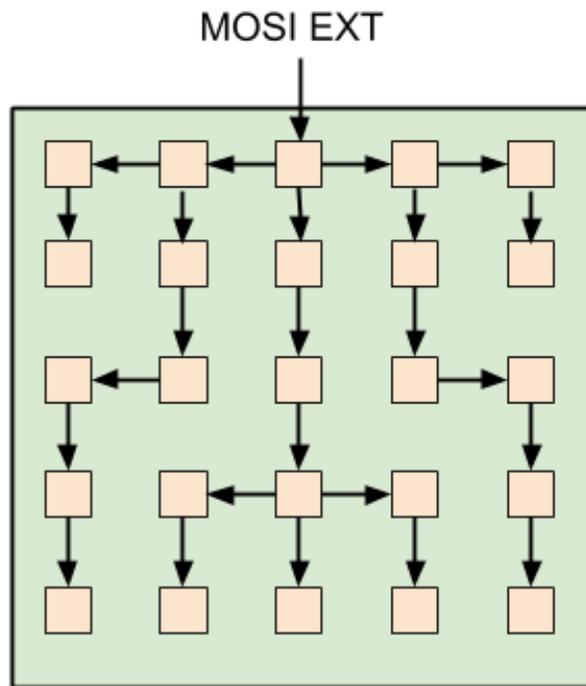
New design for robust I/O and control architecture

Repurpose existing LArPix-v1 low-power data I/O circuit

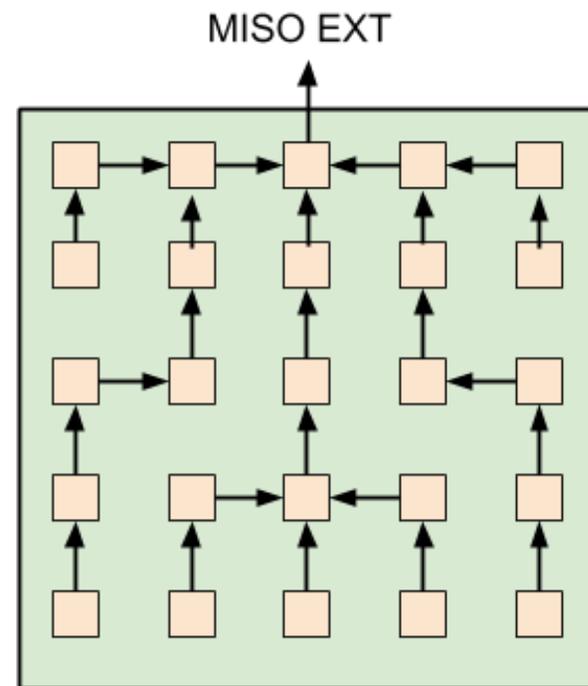
Very slight change enables richer, dynamic I/O architecture

- I/O can occur between any neighboring chips on pixel tile
- Network is built by explicitly connecting neighboring ASICs in a determined fashion

Example: 5 x 5 Pixel Tile



Upstream configuration commands



Downstream data flow

LArPix-v2: Hydra I/O

New design for robust I/O and control architecture

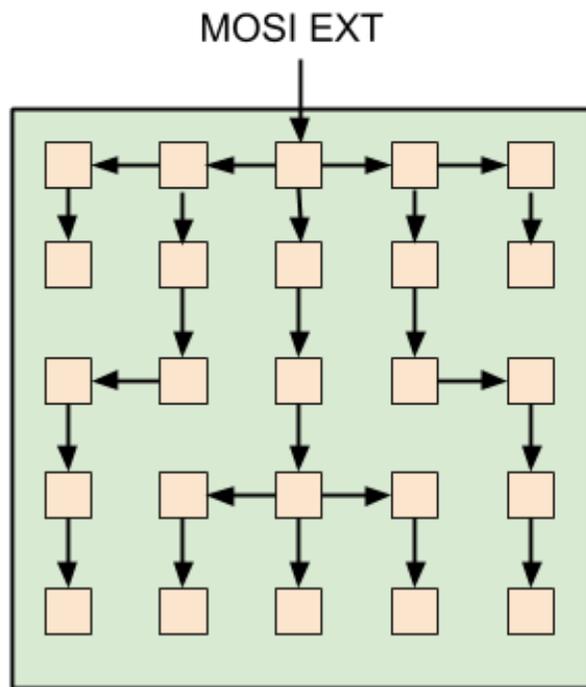
Pixel tile robust to arbitrary chip failure.

Network assembly can be initiated by any chip at tile edge

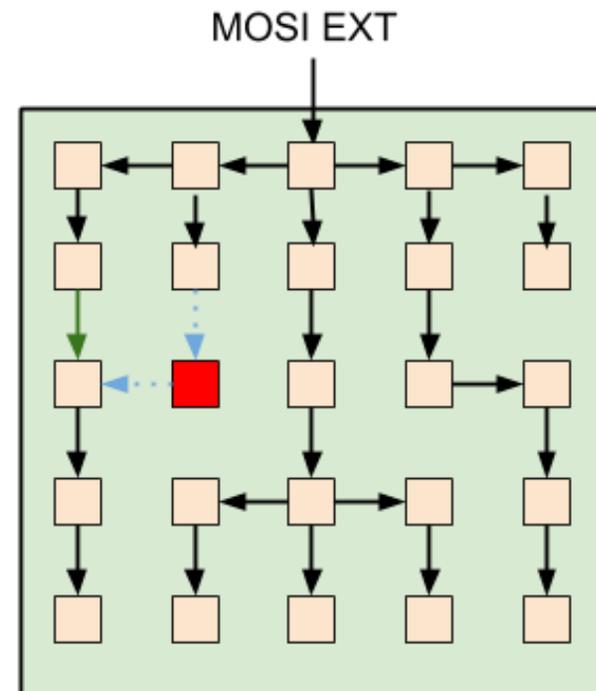
Most of chip circuitry is dormant (disconnected from power) until connected to I/O network.

- Protects against flawed chip drawing excess power or injecting noise into system.

Example: 5 x 5 Pixel Tile



Upstream configuration commands



Network reconfigured, avoiding dead chip

LArPix-v2: Control Electronics

Design Philosophy:

Leverage commercial techniques for simple, scalable readout controller

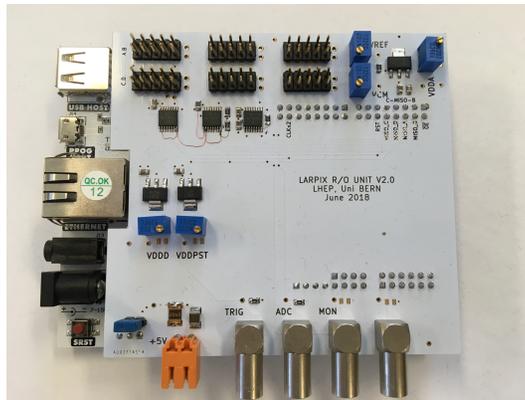
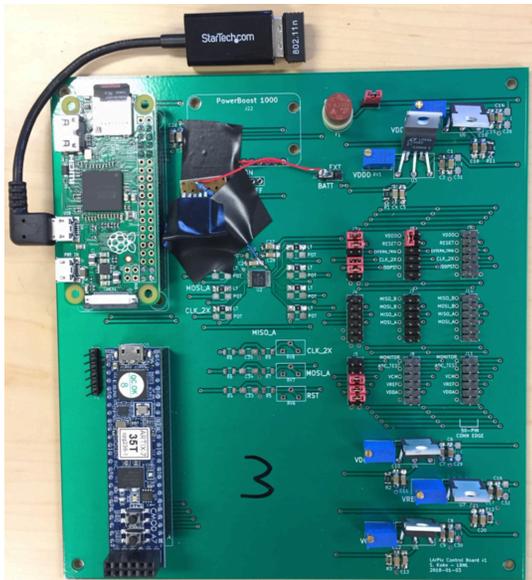
LArPix-v1 Controller (gen 1)

Design: S. Kohn, P. Madigan

Custom interface electronics board with COTS daughter boards:

‘Digital bridge’: Digilent Cmod FPGA

‘DAQ-included’: RaspPi-Zero



LArPix-v1 Controller (gen 2)

Design: I. Kreslo

‘Interface’ mezzanine on COTS Arty Zynq ‘Digital’ board

Zynq provides in-chip FPGA-CPU bridge

Scalable output via ZeroMQ messaging over ethernet

LArPix-v2 Controller a.k.a. PAC-MAN

Design: Team effort, with UC-Davis taking the lead

‘Interface’ mezzanine on COTS TRENZ Zynq board

Substantial improvement of power and noise isolation

Integrated testing, tuning features to facilitate scalable system commissioning and operation



TRENZ TE0720



Module of Opportunity

Adaptation of LArPix for operation in Far Detector Module?

DUNE Near Detector vs. Far Detector specifications:

In principle, physics performance specs for Near Detector are sufficient for Far Detector
Far Detector anode area (assuming FD drift distance unchanged): $\sim x15$ of Near Detector
Continuous self-triggered readout likely results in modest raw data volume: ~ 30 MB/s
Assembly, testing, installation of pixel tiles likely manageable.
Commercial production costs for pixel tiles seem quite reasonable.

→ Will be validated by LArPix system production for the ArgonCube 2x2 Demonstrator

Key difference:

→ *Far Detector requirements for system robustness and longevity far more stringent*

Related system tasks:

Anode Plane:

Requires mechanical and electrical redesign of FD anode plane structure for pixel tiles

Photon Detection System:

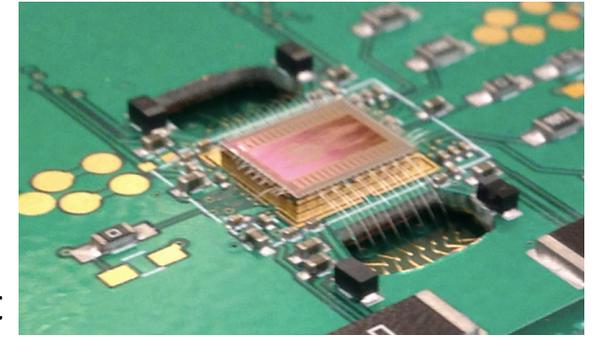
Pixel tiles not compatible with FD photon detectors nested within anode plane
Alternate approach to photon detector deployment will be required.

Large-scale Demonstration:

Before adoption for 4th module, need full-scale FD system validation (in ProtoDUNE@CERN?)



LArPix Summary



3D pixelated charge readout for LArTPCs:

LArPix demonstrates feasibility of low-noise low-power 3D readout

Unique front-end channel for every pixel

Key purpose: overcome neutrino pileup in DUNE Near Detector LArTPC

LArPix Progress:

Successful operation of O(1k) channel LArPix readout system in LArTPCs

Development of fully-scalable LArPix-v2 ASIC, Pixel Tile, Control Electronics

Next Step: ArgonCube 2x2 Demonstrator

Commission and operate ~0.4 M-channel pixelated LArTPC

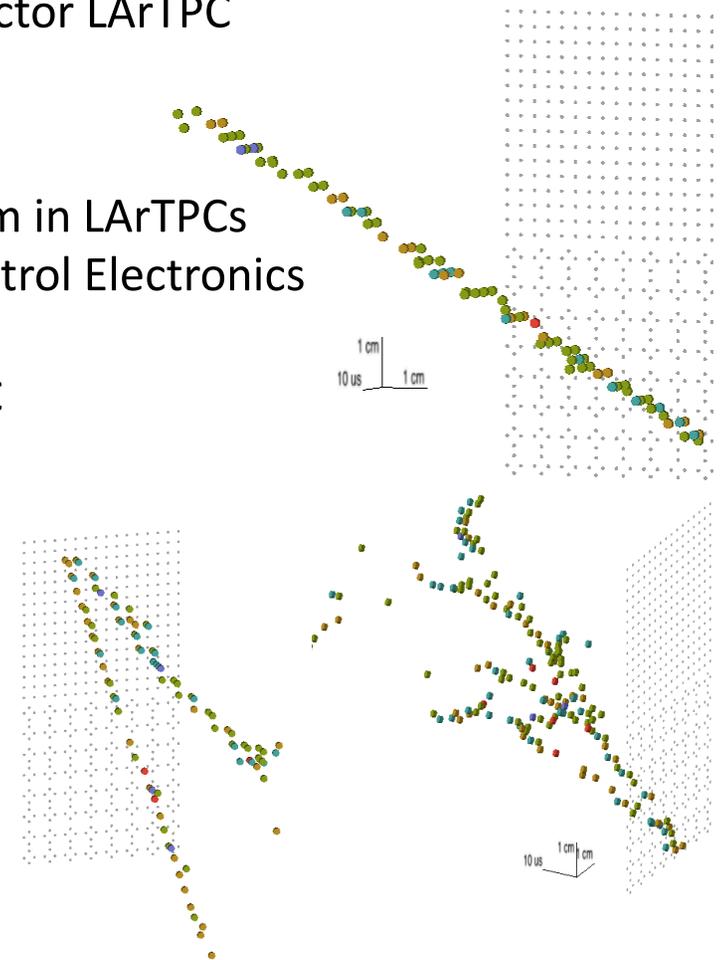
Module of Opportunity:

LArPix specs for Near Detector compatible with requirements for Module of Opportunity

→ *Primary technical hurdle: system longevity*

Must revise anode plane design to support pixel tiles

Must adapt current arrangement of photon detectors



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