HGCROC
402.4.4.1.1 Module Base Plates (Baseplates)
402.4.4.1.3 Module Circuit Boards (Hexaboards)

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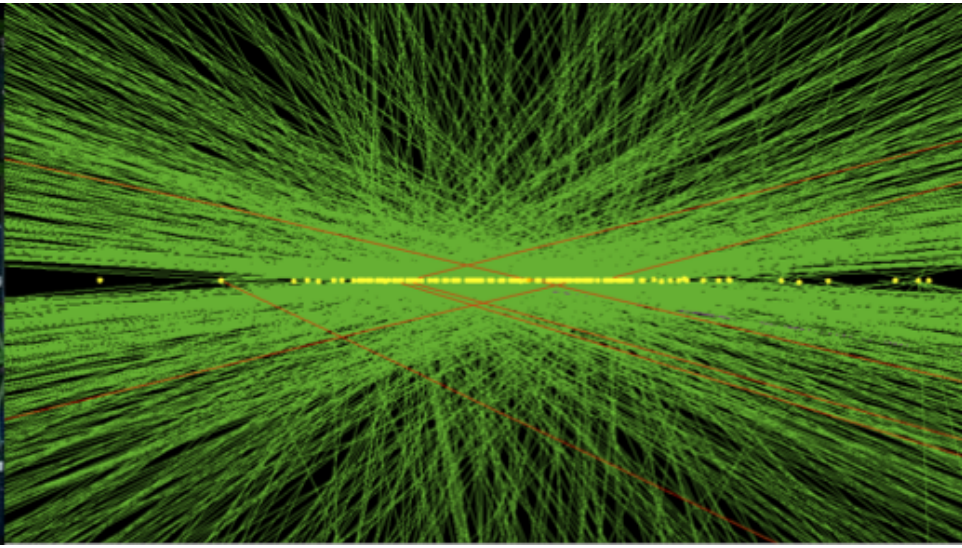
HL LHC CMS CD-1 Review

October 23, 2019



Outline

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  - Design, evolution, and recent progress
- Module Circuit Boards (Hexaboards)
  - Design and recent progress
- Module Base Plates (Baseplates)
  - Design and status
- QA/QC
- Resource Optimization
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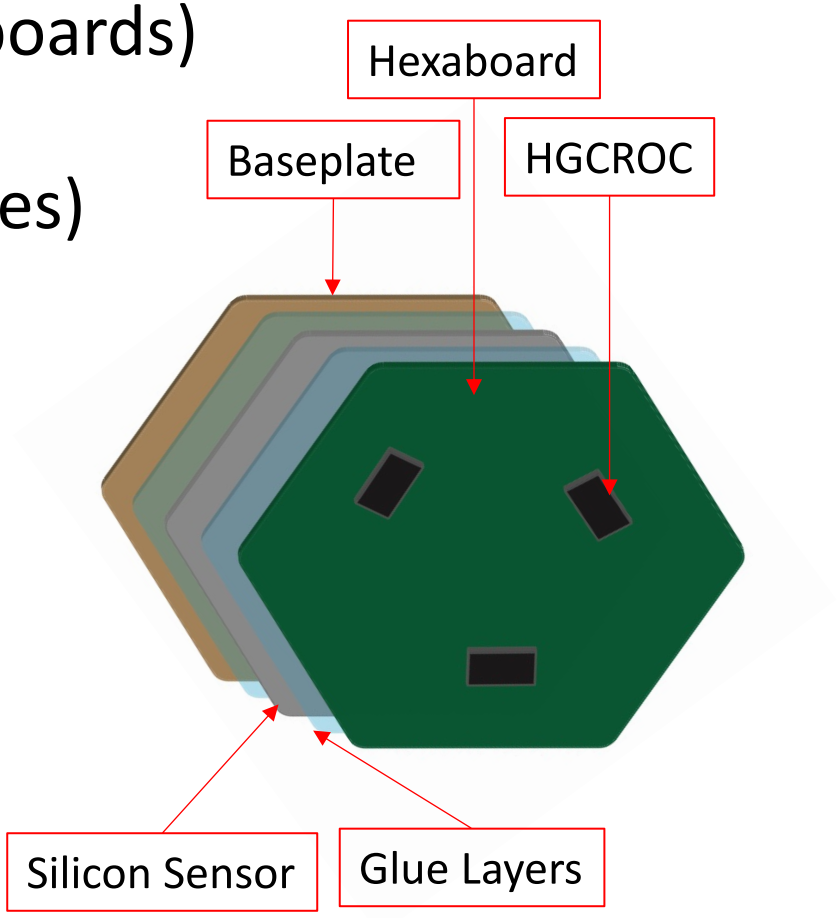
- ES&H
- Summary



WBS Structure & Dictionary

- **402.4.4.1.1 CE – Module Base Plates (Baseplates)**

This WBS includes the procurement of materials for prototyping of baseplates for the silicon modules of the hadronic section of the endcap calorimeter (CE-H). This WBS element also includes the labor costs associated with baseplate R&D and prototyping as well as quality control (QC) during production of baseplates.

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- **402.4.4.1.2 CE – Module Kapton (OBSOLETE)**

- **402.4.4.1.3 CE – Module Circuit Boards (Hexaboards)**

This WBS covers the cost of the design, purchase, fabrication, and assembly of module circuit boards (PCBs) for the hadronic section of the endcap calorimeter (CE). It also includes carrying out a series of prototypes and pre-production steps, as well as procurement of the PCBs, including the assembly of electronic components onto the PCBs. The PCB production and assembly of components will be performed in industry. In addition, this WBS covers the cost of initial testing of the PCBs at the institution responsible for this task.

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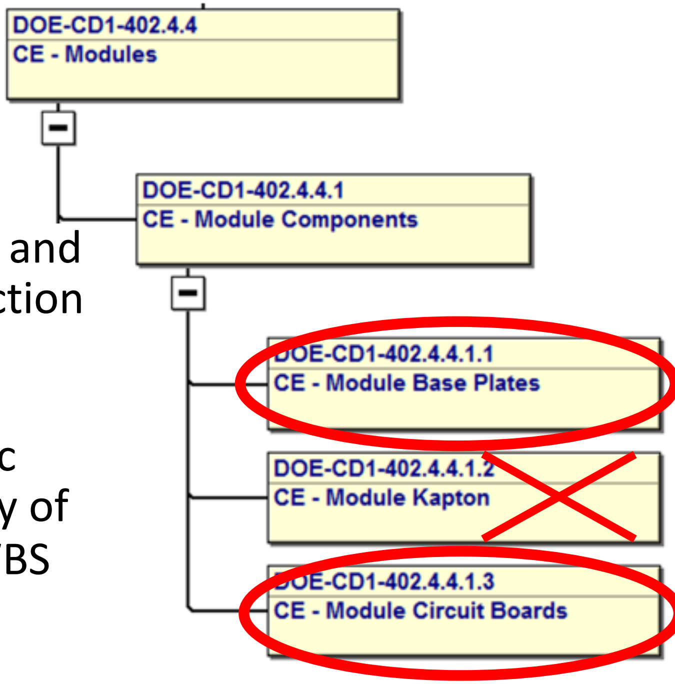


Biographical Sketch

- L3 manager for CE Sensors and Modules (402.4.3 and 402.4.4) with Manfred Paulini
- Professor of physics, TTU, (2000 – present)
- Detector R&D:
  - Cherenkov calorimeters (*e.g*. CMS HF)
  - Dual-readout calorimeters (DREAM and RD-52)
  - Radiation-damage studies in calorimeters
  - Doped-quartz optical fiber development for future applications
  - Development of new detector techniques using silicon
- Physics:
  - Standard Model (A_{FB}), Beyond Standard Model searches (mono- and di-jets), and studies in multi-boson physics (aTGC, aQGC)
- CMS HF Technical Coordinator (1994-2007)
- CMS HCAL IB Chair (2007-2009)
- CMS Endcap/Forward Calorimeter Calibration Coordinator (2009-2010)

HGCROC

HGCROC Design Considerations

- Radiation tolerance (EC-sci-eng-002, EC-eng-005) up to ~1.5 MGy and 10^{16} n_{eq}/cm^2 and SEU compliant
- Ability to calibrate with minimum-ionizing particles (MIPs) throughout HL-LHC lifetime with *S*/*N*>5(1.7) and keep level noise level below 2500 e^- for 65 pC cell
- Linearity better than 1% over full range
- Good timing information <100 ps for pulses above 12 fC (3 MIPs in 300 μm sensor)
- Fast shaping time (<20 ns) to minimize out of time pileup
- Leakage current compensation with irradiation
- High channel (78) density per chip
- Low power consumption (~14 mW/ch) in -30°C operation

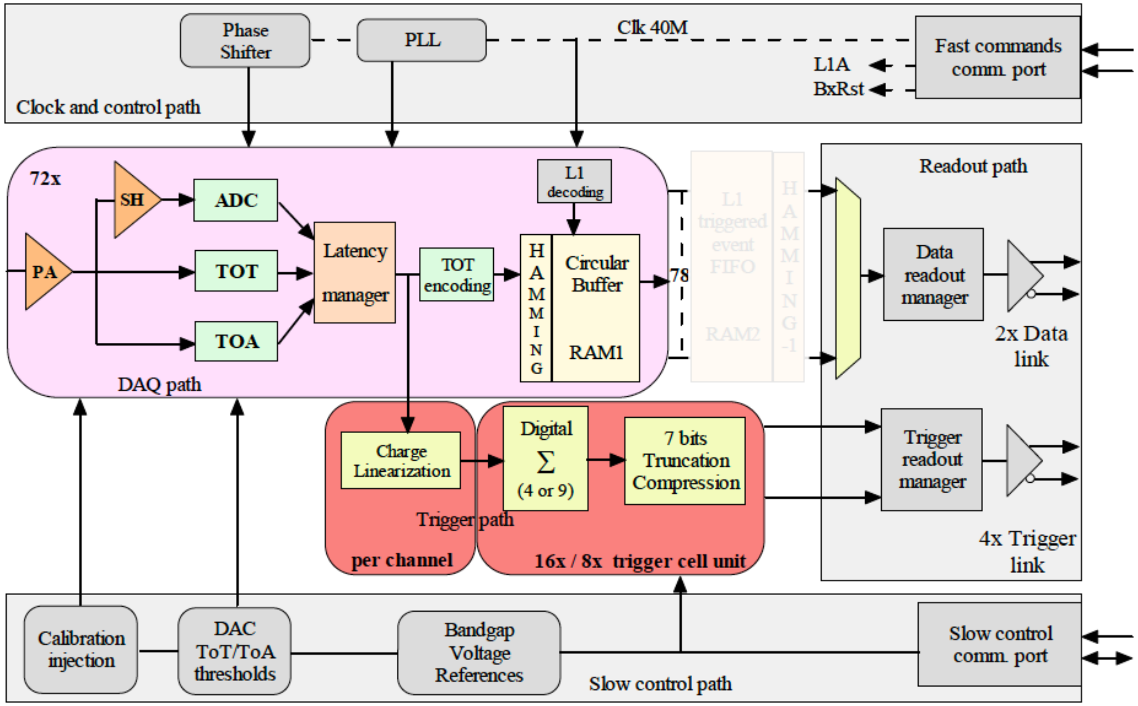
Charge #2

HGCROC US Contributions

- The US has been playing important roles in HGCROC project from the start
  - US engineers involved in development of specifications and validation tests
  - HGCROC sends data to ECON (a major component in US scope) and the interface requires close collaboration in TRG and DAQ data formats
  - HGCROC progress has been excellent and the design adheres to these protocols (HGCROC2 for TRG and HGCROC3 for DAQ)
- Design and R&D carried out by the French groups building on the SKIROC (2016) and SKIROC-CMS (2017) experience
  - Analog part (PLL, calibration, monitoring, serializer) by IRFU and OMEGA
  - Digital part (fast components and TRG considerations) by OMEGA
  - Integration by OMEGA

HGCROC2 Test Boards and Status

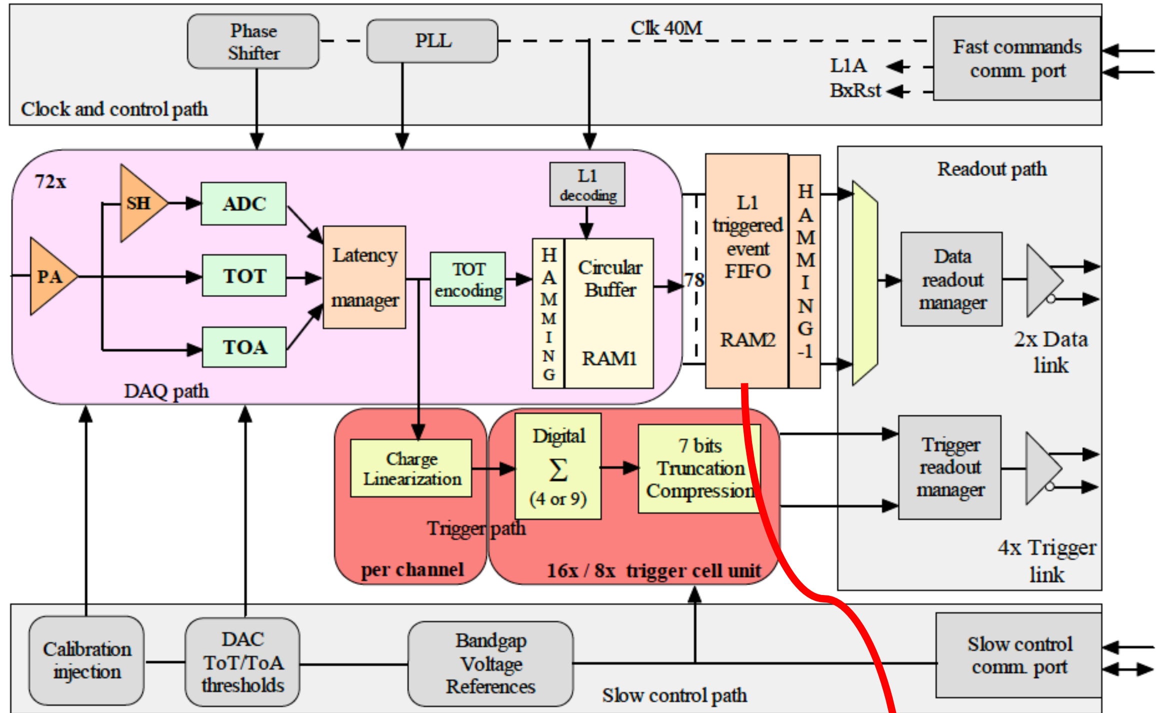
Status

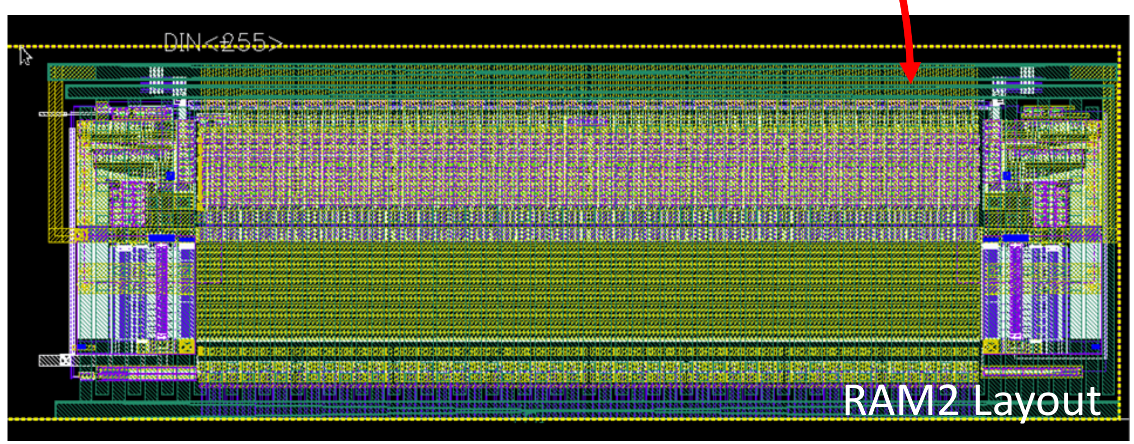


- HGCROC2 incorporates design improvements based on tests of HGCROC1. Chips have been packaged and are being tested
- Test socket made to run reception tests of the (~1000) packaged chips for V2 hexaboards
- 8 boards with naked dies on IC boards were tested in July and first test results are very good
- Digital noise in analog section largely eliminated
- Power consumption as expected
- Radiation tests are scheduled for the next month

HGCROC3 Status

- HGCROC2 represents a significant step forward
- HGCROC3 submission is planned for February 2020 will add the last piece of the full de-randomizer
- Many of the changes/improvements are informed by measurements from HGCROC1 and HGCROC2
- New PLL design (test vehicle) submitted to be received by December 2019 and radiation tests will follow in early 2020
- HGCROC project has made excellent progress and expect to remain on schedule





HGCROC Delayed Risk

RT-402-4-13-D CE - HGCROC front end chip is delayed

Risk Rank:	2 (Medium) **Scores:** Probability : 2 (L) ; Cost: 1 (L) Schedule: 3 (H))	**Risk Status:**	Open
Summary:	If the HGCROC front end chip delivery date is delayed then the assembly of module boards and therefore the assembly of the modules gets delayed. This may jeopardize the delivery of cassettes on time. This risk can include delays in any of the prototype HGCROC chip submissions besides the final production run.		
Risk Type:	Threat	**Owner:**	Jeremiah Michael Mans
WBS:	402.4 CE - Calorimeter Endcap	**Risk Area:**	External Risk / Collaborators
Probability (P):	20%	**Technical Impact:**	0 (N) - negligible technical impact
Cost Impact:	PDF = 3-point - triangular Minimum = 21 k$ Most likely = 126 k$ Maximum = 252 k$ Mean = 133.0 k$ P * <Impact> = 27.0 k$	**Schedule Impact:**	PDF = 3-point - triangular Minimum = 1.0 months Most likely = 6.0 months Maximum = 12.0 months Mean = 6.33 months P * <Impact> = 1.266 months
Basis of Estimate:	The min/likely/max delays are estimated to be 1/6/12 months. The L3 burn rate due to the delay of downstream activities is $21k/month (CMS-doc-13481). No addition costs have been assume in this risk entry for a possible acceleration of module and cassette production. These are incluided as a separate risk event. Min cost = 1 month * $21k burn rate = $21k. Likely cost = 6 months * $21k burn rate = $126k. Max cost = 12 months * $21k burn rate = $252k.		
Cause or Trigger:		**Impacted Activities:**	Assembly of module boards. JM: Implemented between: (A) 'vendor fabricates HGROC' and 'vendor delivers HGROC' for silicon, and (B) 'prepare and place orders' and 'delivery of HGROC-SiPM' for scintillator. LT: assume burn rate cost is equally shared between these two items.
Start date:	1-Dec-2019	**End date:**	1-Dec-2020
Risk Mitigations:	Develop test stands so that components that depend on the HGCROC can be tested as much as possible using emulators and older/prototype/non-production versions of the HGCROC chip. Include significant engineering so that we can help verify and validate the prototype and production HGCROC chip functionality and quality as quickly as possible. Use prototype and pre-production HGCROC chips in the 2 major system prototypes for vertical slice tests and in beam tests, and irradiation studies. Ensure the module and cassette production facilities are setup to be able to accelerate production if needed.		
Risk Responses:	Help validate or test the HGCROC chips as quickly as possible to reduce the testing time. Accelerate downstream production (modules and cassette) as needed.		
More details:	CMS-doc-13481		

- Risk covers possible delay to module and tilemodule construction due to a late HGCROC, costs are from standing army delays
- Second risk covers possibility that US effort is needed to address issues seen in the HGCROC3

402.4.4.1.3 Module Circuit Boards (Hexaboards)

Charge #2

Hexaboard Design Considerations

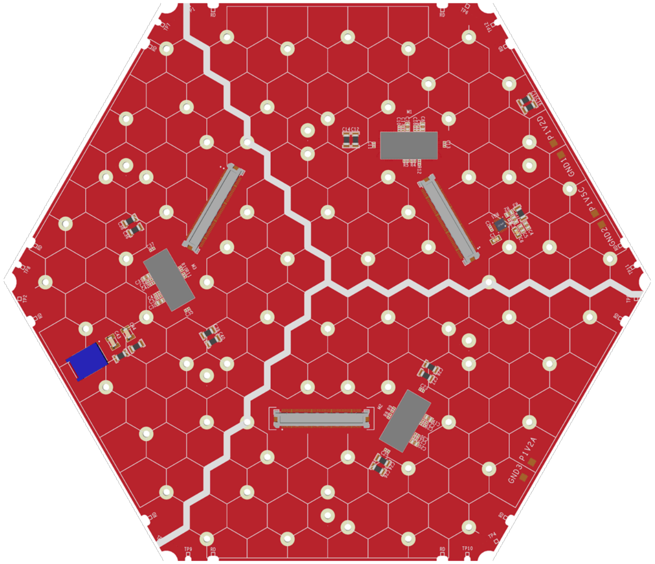
- Hexaboards contain HGCROCs for charge collection from silicon pads and power for biasing the silicon sensors, as well as links to pass information onto motherboards
  - High transverse granularity demands high cell density in hexaboards (EC-sci-eng-004). Low density (LD) hexaboards contain 192 (1.18 cm^2) cells whereas high density (HD) hexaboards contain 432 (0.52 cm^2) cells. Hexaboard layout has to match those of sensors (EC-eng-027) and contain wire-bonding pads (EC-eng-028)
  - The front end electronics system, including hexaboards, need be radiation hard (EC-eng-005, EC-eng-007) for the lifetime of the detector
  - Redundancy and robustness (sci-req-1)
  - Low temperature operation (-30 ^{o}C)

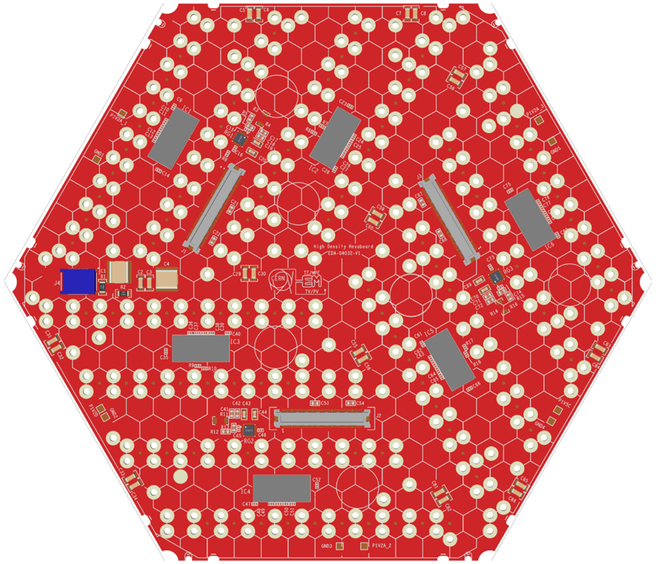
Hexaboard Status

- Design is carried out by CERN and several versions (6" and 8") were produced in industry and successfully used in beam tests since 2016
- Currently we have two 8" versions:
  - Normal through-hole vias ("V1")
  - Blind and buried vias ("V2")
- Six of each version produced:
  - Hexaboard by Cistelaier (IT)
  - Component assembly and wire bonding by Hybrid SA (CH)
- All 12 work, no difference between versions before module assembly
- Test systems exists and analysis software being modified for LD

8” Hexaboards-V2 Status

- Both LD and HD include blind & buried vias – necessary for routing especially under the ASICs – which increases production cost
- LD is out for production and will be populated by components including HGCROC2
- HD and odd-sized to follow
- HD hole design may be further optimized (shape and number)
- Conceptual design for both types is mature and on schedule

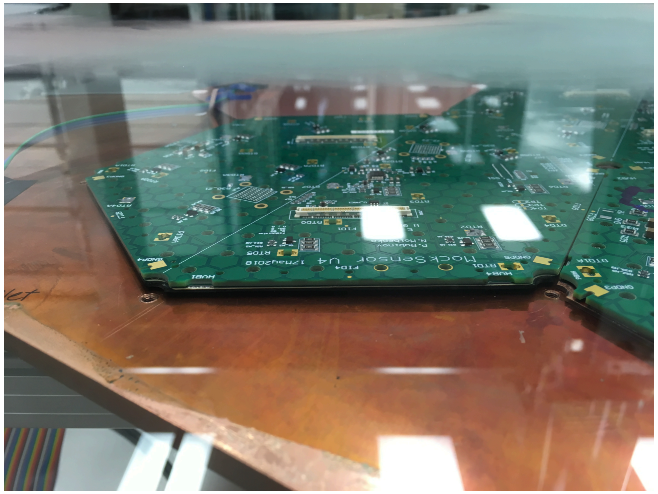


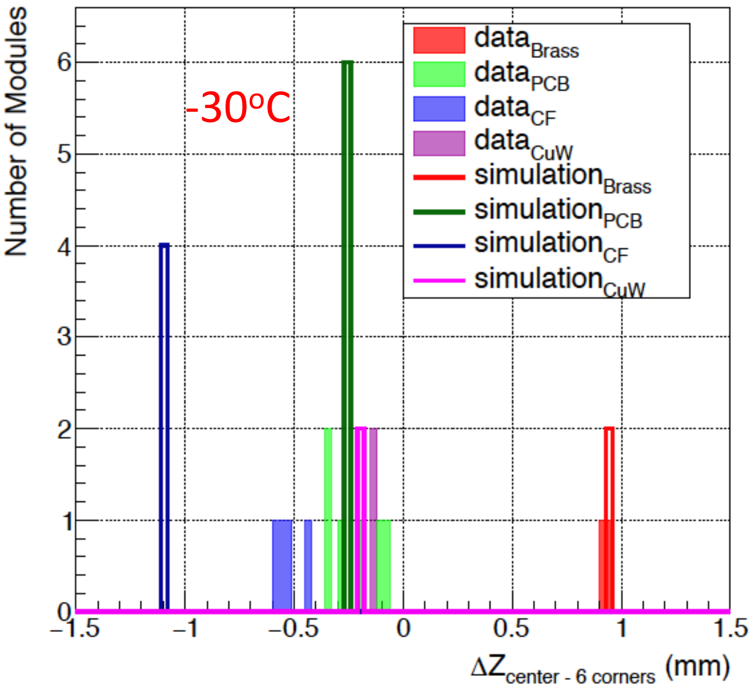


402.4.4.1.1 Module Base Plates (Baseplates)

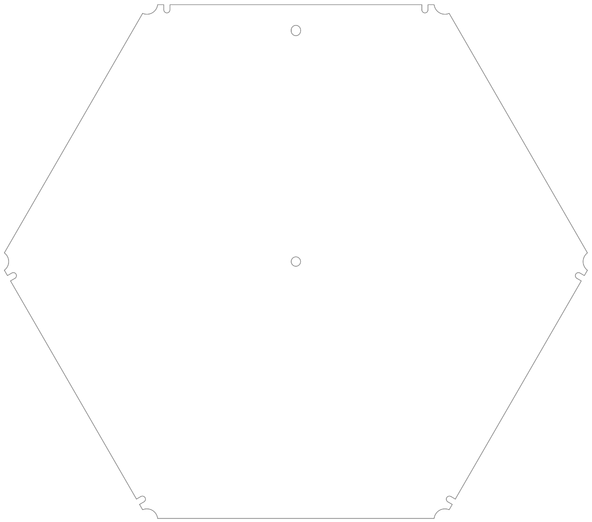
Baseplate Design & Status - I

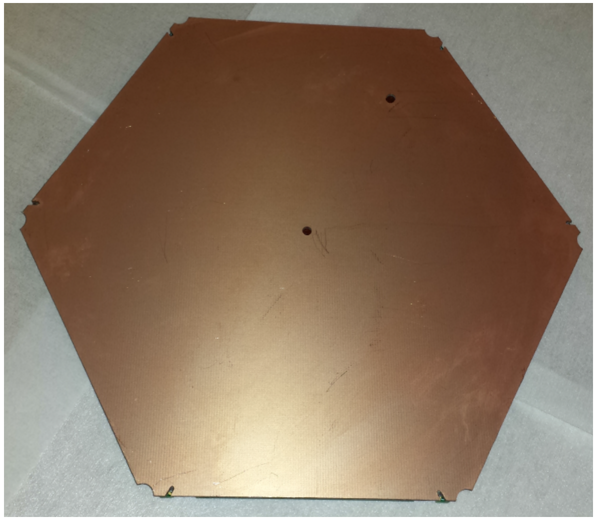
- PCB baseplate design eliminated the Kapton layer from the module stack and satisfactorily addressed the thermal deformation issues at low temperatures and simplified sensor biasing
- CMM measurements at -30 ºC are verified by FEA calculations: the average deformation is less than 250 μm between the edges and center for unfastened modules on cooling plate
- Thickness (1.0±0.1 mm), flatness (±25 μm), dimensional tolerances (±50 μm), good thermal conductivity with silicon sensor (EC-eng-046)
- Baseplate must be radiation hard for the detector lifetime (3 ab^{-1})





Baseplate Design & Status - II





- US developed the concept (details in cms-docdb-13771-v1) and performed complete R&D
- Production (10,140 standard and 2,552 odd-sized) will be carried out by international partners
- Baseplates will be purchased (20%) early in production and do not pose schedule or availability risk
- MAC centers are equipped with resources for complete baseplate QC before module assembly

QA/QC Hexaboards/Baseplates

- Hexaboards
  - QA: Hexaboard prototypes will be made as needed
  - QA: Electrical and thermal performance of the hexaboards will be tested as the design parameters are refined
  - QA: QA Audit Site visit to KSU will take place in advance
  - QC: Hexaboards will be tested by the manufacturer before electronics components are mounted
  - QC: Complete functionality of hexaboards with HGCROCs will be tested at KSU before module assembly at MACs
- Baseplates
  - QA: Baseplate prototypes will be continued to be made as needed
  - QA: Proto-1/2 baseplates will be verified before final production
  - QA: QA Audit Site visit to CMU, TTU and UCSB will take place in advance
  - QC: Project technicians at MACs will validate dimensional characteristics using an optical gauging unit before module assembly
- QC: Database will be utilized to track components, assembled parts, and test results
- Conforms to cms-doc-13093

Resource Optimization

Charge #4

- We have distributed and optimized the project across institutions and vendors. Teams with experience in calorimetry, detector design and construction, and electronics are responsible for the key elements:
- HGCROC
  - The French groups (IRFU, OMEGA,...) and CERN are responsible for the HGCROC design and production
- Hexaboards
  - Hexaboard is designed in collaboration between CERN and Kansas State (KSU) and produced by industry. Both groups are experienced in electronics board design, development, production and testing (*e.g.* Phase I)
- Baseplates
  - Baseplates will be produced by industry and acceptance tests will be carried out at the module assembly sites (CMU, TTU, UCSB)
- All universities have access to low-cost undergraduate technicians

ES&H

Charge #6

- The hazards with hexaboards involve high voltage, thermal cycling, and lasers when tested in assembled modules
- ES&H Site Visit to KSU as well as MACs will take place in advance
- All ES&H aspects of the HL LHC CMS Detector Upgrade Project will be handled in accordance with the Fermilab Integrated Safety Management approach, and the rules and procedures laid out in the Fermilab ES&H Manual (FESHM)
- We are following our Integrated Safety Management Plan (cms-doc-13395) and have documented our hazards in the preliminary Hazard Awareness Report (cms-doc-13394)
- In General Safety is achieved through standard Lab/Institute practices
  - No construction, accelerator operation, or exotic fabrication
  - No imminent peril situations or unusual hazards
  - Items comply with local safety standards in site of fabrication and operation
  - Site Safety officers at Institutes identified in the SOW

Institutions (Hexaboards/baseplates)

Charge #5

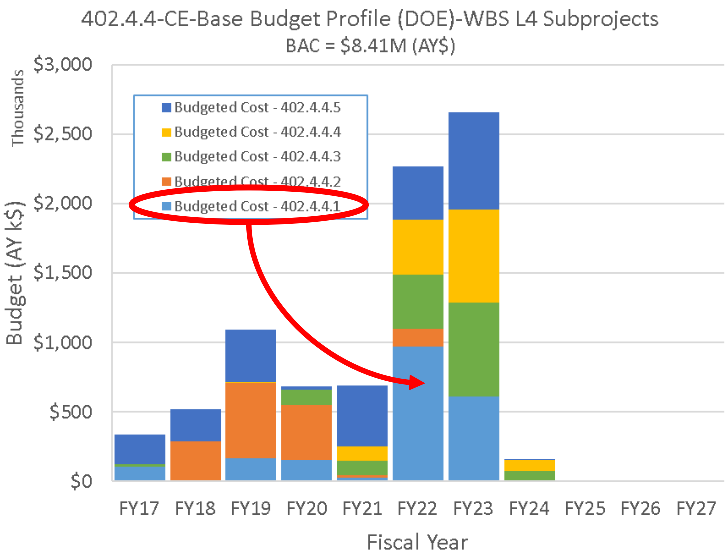
- Brown University (U. Heintz)
  - Irradiations
- Carnegie Mellon University (M. Paulini)
  - Prototypes and modules
- Fermilab (Z. Geczse, P. Rubinov)
  - System engineering and baseplate design
- Texas Tech University (N. Akchurin)
  - Prototypes and modules
- UC-Santa Barbara (J. Incandela)
  - Prototypes and modules
- Kansas State (K. Kaadze)
  - Hexaboard design, procurement and testing

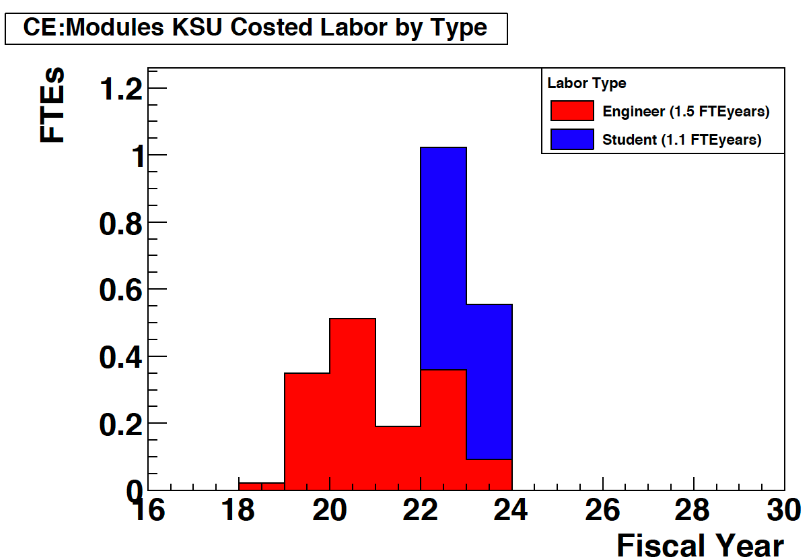
Cost Estimate & Profile

Charge #3

- The overall cost is modest and well matched with the US plan and institutional resources. The cost estimates are based on quotes. The dominating M&S is for hexaboards ($1.36M). Baseplate cost has gone down significantly (PCB and iCMS)
- The cost and labor profiles peak in FY22 and FY23 where the baseplate and hexaboard purchases and hexaboard QC will take place
- Kansas State is responsible for hexaboard purchase and testing using undergraduate technicians with oversight by engineers

WBS	Direct M&S ($)	Labor (Hours)	FTE	Direct + Indirect + Esc. ($)	Estimate Uncertainty ($)	Total Cost ($)
DOE-CD1-402.4.4.1 CE - Module Components	**1,382,564**	**7744**	**4.38**	**2,051,899**	**547,065**	**2,598,964**
DOE-CD1-402.4.4.1.1 CE - Module Base Plates	24,153	1192	0.67	145,031	20,499	165,530
DOE-CD1-402.4.4.1.3 CE - Module Circuit Boards	1,358,411	6552	3.71	1,906,868	526,566	2,433,434





Charge #3

Schedule & Milestones

- Overall schedule has been updated to match the present HGCROC schedule (HGCROC submission on Feb 2020) by accelerating the module and cassette production
- There are no major schedule concerns for baseplate and hexaboard production for timely delivery to MACs

HGCROCV2 Available	28-Jun-19
CE.MO.5: HGCROC-V2 module validated	27-Jan-20
CE.FE.10: HGCROC-V3 submission	3-Feb-20
HGCROCV3 Available	30-Jun-20
Production Silicon Module PCB Design Available	1-Feb-21
CE.EL.5: Final Hexaboard qualified	4-Feb-21
CE.MO.6: HGCROC-V3 module validated	8-Feb-21
CE.FE.12: HGCROC ready for mass production	15-Apr-21
CE.MO.7: Module components orders placed	30-Nov-21
CE.MO.8: Final module qualified	6-Dec-21
Production HGCROC Available	4-Jan-22
CE.MO.9: Modules production 5% complete	24-Jun-22
CE.MO.11: Modules production 100% complete	13-Feb-24

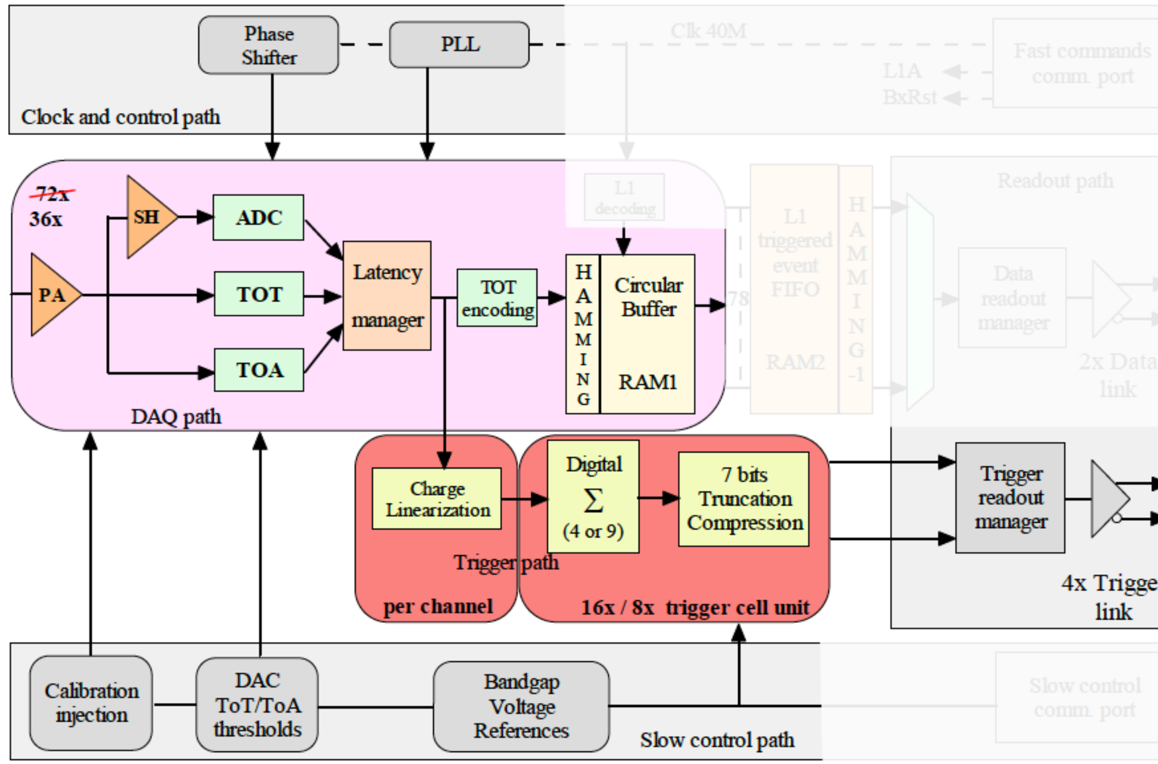
Summary

- Recent technical progress in HGCROC development and hexaboard design/production signify significant strides forward in this project and maintain schedule
- In collaboration with iCMS, major effort over next two years will concentrate on the production versions of HGCROC and 8-inch hexaboard
  - Evaluate HGCROC and hexaboard performance in prototype modules
  - Understand their failure modes
  - Continue developing system test procedures in preparation for the production phase
- Cost, schedule, and risks are well understood and the present designs are mature

Backup

HGCROC1 Status

- All analog block work after more than 200 Mrad
- CLPS receiver seems to be degraded but still works by adjusting the power voltage
- CLPS transmitter works fine
- PLL fails after 40 Mrad
- Slow control path needs to be further tested for reproducibility



- There is a failure around SRAM but not the SRAM itself, perhaps reading, writing, serialization. It is under investigation
- New PLL design (test vehicle) submitted to be received by December 2019 and radiation tests will follow in early 2020

Risk

RT-402-4-09-D CE - Module PCB batch failure

Risk Rank:	1 (Low) **Scores:** Probability : 1 (VL) ; Cost: 1 (L) Schedule: 2 (M))	**Risk Status:**	Open
Summary:	One batch worth 1000 module PCB's has low quality yield and is unusable. This risk covers a number of scenarios where the assembled module PCB's are unusable. This could include problems in the performance of the parts or in the module PCBs or in the assembly process, or in shipping or handling. We assume all PCBs will be remade and the parts on the assembled PCB are lost.		
Risk Type:	Threat	**Owner:**	Manfred Paulini
WBS:	402.4 CE - Calorimeter Endcap	**Risk Area:**	External Risk / Vendors
Probability (P):	5%	**Technical Impact:**	1 (L) - somewhat substandard
Cost Impact:	PDF = 2-point - flat range Minimum = 144 k$ Most likely = N/A Maximum = 186 k$ Mean = 165.0 k$ P * <Impact> = 8.0 k$	**Schedule Impact:**	PDF = 2-point - flat range Minimum = 2.0 months Most likely = N/A Maximum = 4.0 months Mean = 3 months P * <Impact> = 0.15 months
Basis of Estimate:	One batch worth 1000 module PCB's has low quality yield and is unusable.Cost impact is $102k and 2-4 month delay. Cost includes total cost of parts and assembly. The L3 burn rate due to the delay of downstream activities is $21k/month (CMS-doc-13481). Min cost = $102k + 2 months * $21k burn rate = $144k. Max cost = $102k + 4 months * $21k burn rate = $186k.		
Cause or Trigger:		**Impacted Activities:**	Module assembly at modules assembly sites.
Start date:	1-Oct-2019	**End date:**	2-Oct-2022
Risk Mitigations:	The design, and module PCB will go through two prototype stages and vertical slide tests, as well as beam tests. The production parts will go through QC, and the vendors will be qualified through the prototype cycles. Costs will be mitigated by writing the purchase contracts so we only pay for good parts.		
Risk Responses:	We will need to request additional funds from contingency to pay for the replacement assembled PCBs and we may need to accelerate module production, and/or cassette production in these are on the critical path.		
More details:	CMS-doc-13481		

Risk

RT-402-4-01-D CE - Additional FE ASIC engineering run required

Risk Rank:	3 (High) **Scores:** Probability : 3 (M) ; Cost: 2 (M) Schedule: 3 (H))	**Risk Status:**	Open
Summary:	The FE ASIC is not a USCMS deliverable. The required FE ASIC are expected to be received free of charge from the international project in exchange for the concentrator ASICs provided for the electromagnetic section of the CE (CE-E). However, the US, along with the rest of the collaboration, would share a portion of the cost of an additional engineering run for the FE ASIC beyond the current planned two engineering runs. If a significant flaw is observed after the second engineering run, a third cycle may be required. In this case, US ASIC engineering resources may be required to consult, validate, or finalize some specific part of the design. The likely risk is a radiation effect in the digital part of the ASIC, since that part of the chip will likely be completed last and the irradiation campaign will not be completed until after the engineering run.		
Risk Type:	Threat	**Owner:**	Jeremiah Michael Mans
WBS:	402.4 CE - Calorimeter Endcap	**Risk Area:**	Technical Risk / Quality
Probability (P):	25%	**Technical Impact:**	2 (M) - significantly substandard
Cost Impact:	PDF = 1-point - single value Minimum = N/A Most likely = 336 k$ Maximum = N/A Mean = 336.0 k$ P * <Impact> = 84.0 k$	**Schedule Impact:**	PDF = 1-point - single value Minimum = N/A Most likely = 8.0 months Maximum = N/A Mean = 8 months P * <Impact> = 2 months
Basis of Estimate:	Cost: Assume four months of ASIC engineering ($108k) and $60k MandS based on a 27% cost-share for the ASIC = $168k. The 27% fraction is the standard USCMS contribution to international CMS common costs. Schedule: An eight-month delay would be incurred. The L3 burn rate due to the delay of downstream activities is $21k/month (CMS-doc-13481). Some downstream activities may need to be accelerated if deemed necessary to complete production on schedule. The cost associated with such an acceleration is not included here but included as a separate risk. Total impact = $168k + 8months * $21k burn rate = $336k.		
Cause or Trigger:		**Impacted Activities:**	Silicon module PCB completion, silicon module assembly, scintillator tile-module assembly, and cassette assembly.
Start date:	1-Jun-2020	**End date:**	1-Mar-2021
Risk Mitigations:	Managers will work with engineering and development team to provide full quality assurance for the ASIC design before engineering runs occur. We have 1 FTE of extra engineering over 2 years to work with CERN and FE ASIC engineers to help validate the FE ASIC, in addition to the work that is needed to interface the chip into USCMS deliverables.		
Risk Responses:	Some downstream activities may need to be accelerated if deemed necessary to complete production on schedule. The cost associated with such an acceleration is not included here but included as a separate risk.		
More details:	CMS-doc-13481		