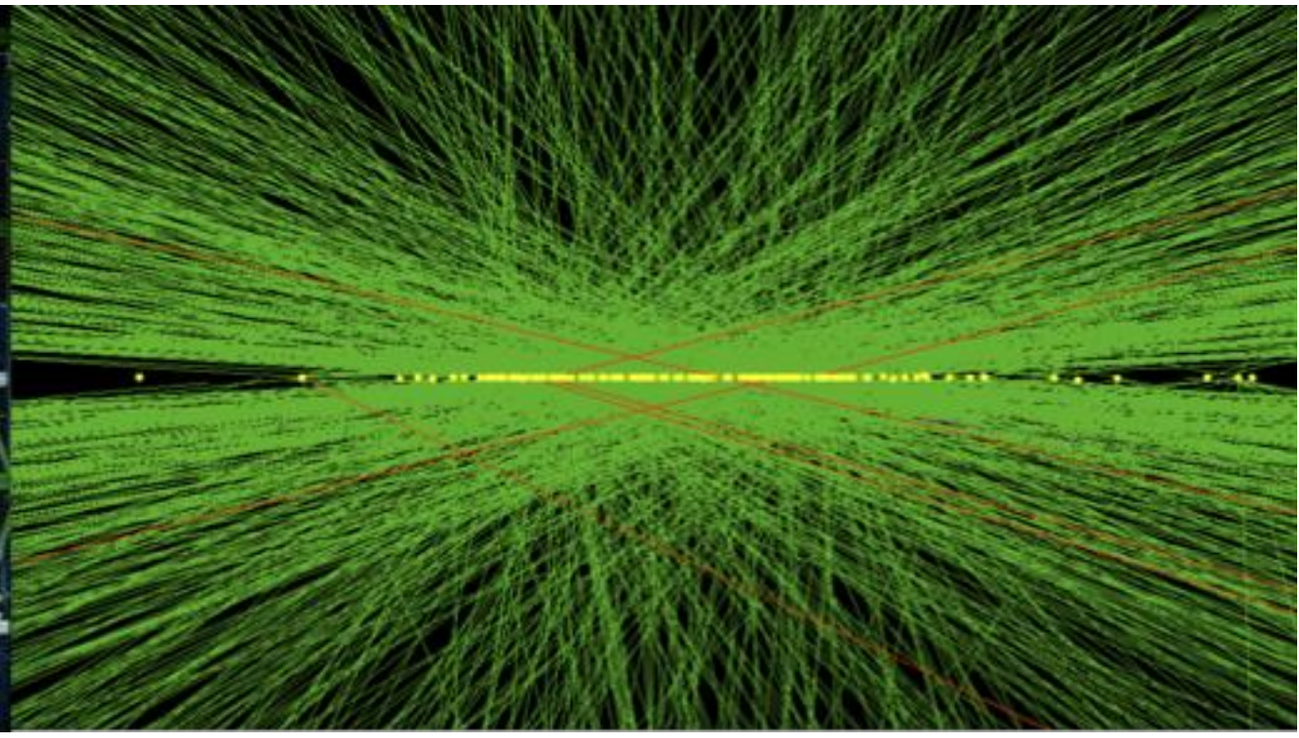
B05 : CE Concentrator ASIC

Jim Hirschauer (Fermilab), L3 Manager

CD1 Review

October 23, 2019



Outline

- Introduction and scope
- Conceptual design
- Cost, schedule, risks
- Organizational aspects
- Contributing institutions and resource optimization
- Quality assurance and quality control
- Prototype 1 plan and progress
- Summary

Biographical sketch

Charge #5

- Fermilab Scientist

HL-LHC upgrade:

- L3 manager for Endcap Calorimeter (EC) – Electronics and services
  - Lead physicist for ECON ASIC development/production
- iCMS coordinator for EC On-Motherboard Electronics

Phase 1 hadron calorimeter (HCAL) upgrade experience:

- L3 manager for barrel/endcap readout electronics 2013-2019.
  - Lead physicist for QIE10/QIE11 readout ASIC development/production
- Helped lead team through CD-1, CD-2/3, and CD-4.
- iCMS coordinator for HCAL barrel/endcap upgrade 2013-2019

Other experience:

- HCAL Operations Coordinator 2011-12.
- Chair of HCAL Institution Board since 2018.

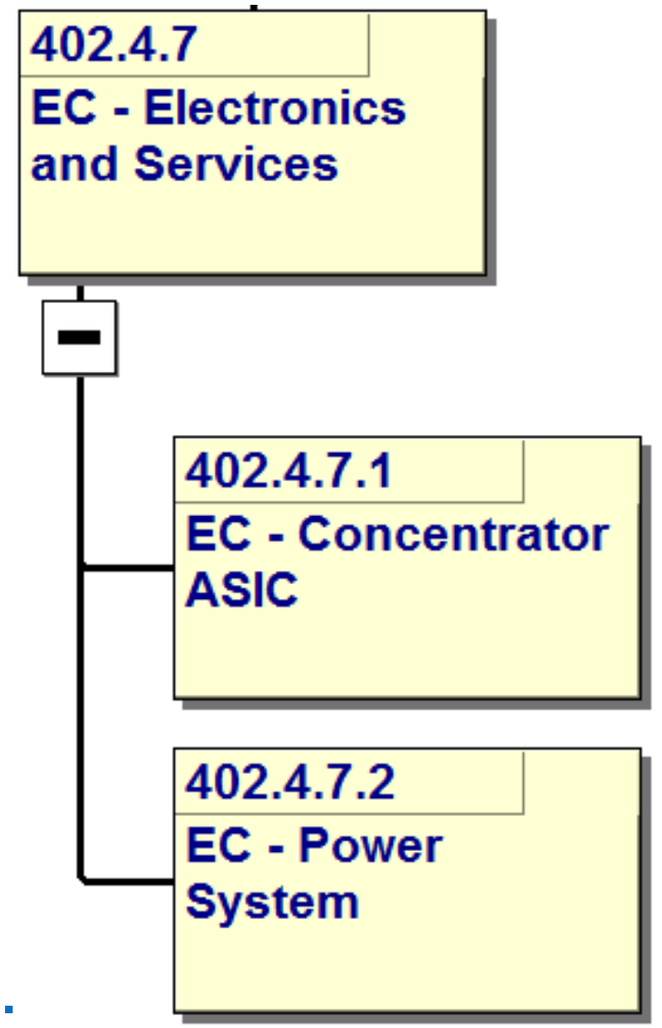
Research focus: Searches for supersymmetry in fully hadronic final states.

Introduction and scope

Deliverables and WBS structure

Charge #7

- 402.4.7.1 Concentrator ASIC
  - WBS includes specification, design, prototyping, prototype testing, production, packaging, and quality control of the "ECON" ASICs.
  - Deliverable is fully tested set of ASICs for entire EC.
  - Focus of this presentation.

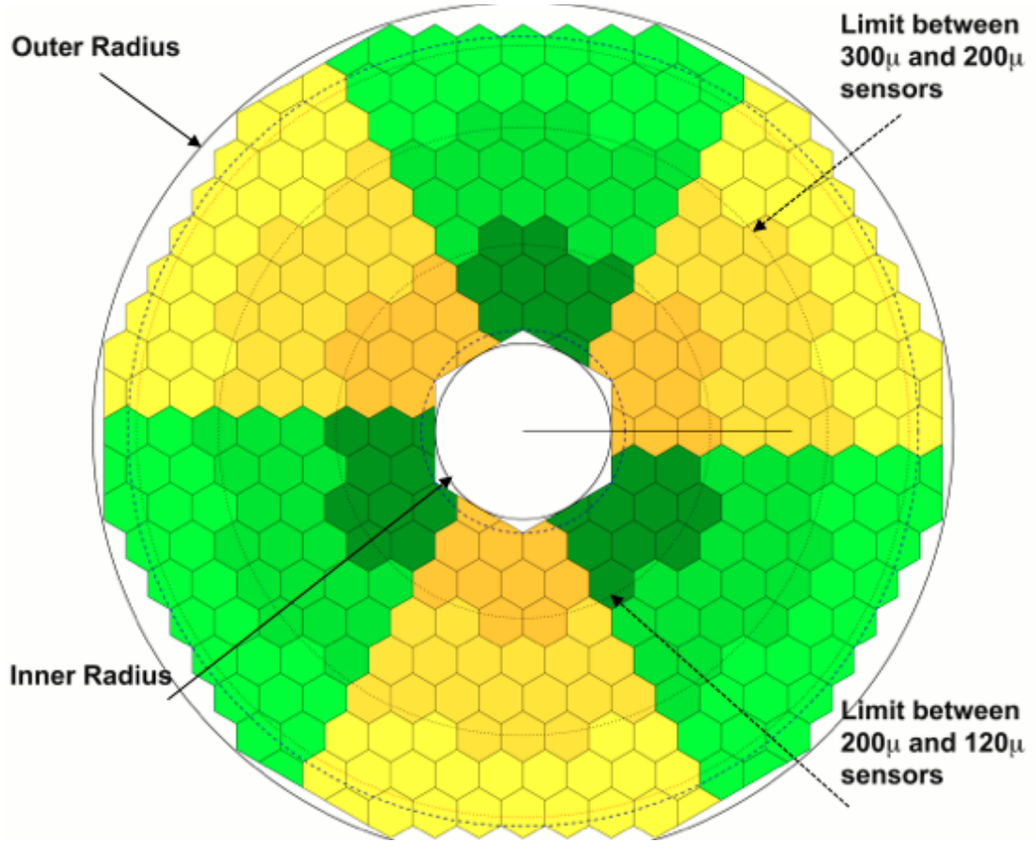


- 402.4.7.2 Power system
  - All scope included in objective KPP
  - US is responsible for 40% of the low voltage (10V for electronics) and high voltage (1kV for Si bias) systems.
  - WBS includes specification, prototype evaluation, procurement, and QC of the US fraction of the power system.
  - Deliverable is 40% of the tested power system.

Summary of ECON purpose

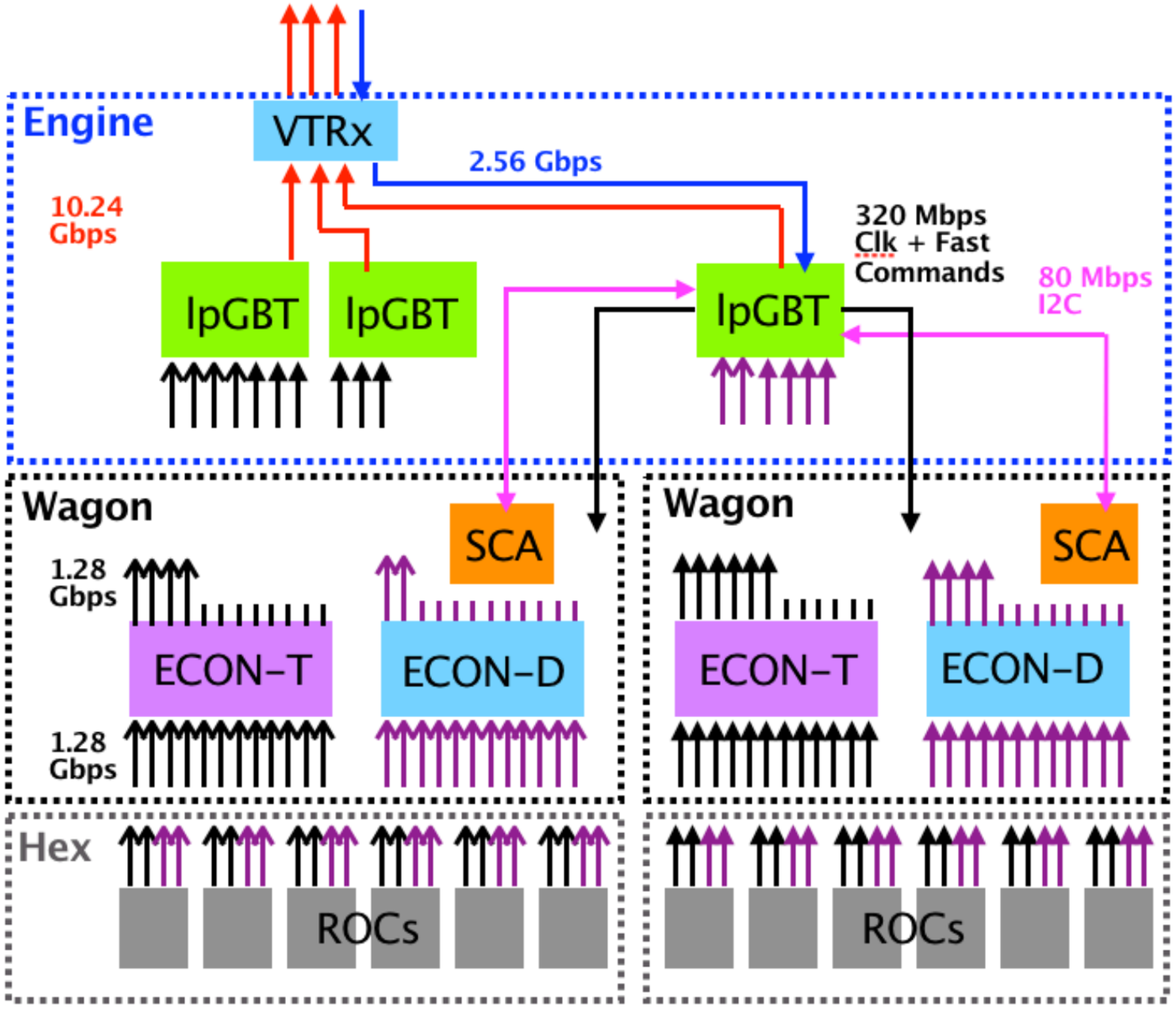
Charge #1

- EC has 4.3M trigger channels each sending >10 bits of data at 40 MHz.
  - Naively requires 215k lpGBT links costing $90M at $400/link.
- However, interesting energy is deposited mostly in the central part of the detector.
  - Bandwidth density is lower in outer part of detector.
- ECON will select and concentrate data associated with interesting energy depositions to maximize use of available bandwidth.
- ECON-based system requires 7k links instead of 215k.



Data flow

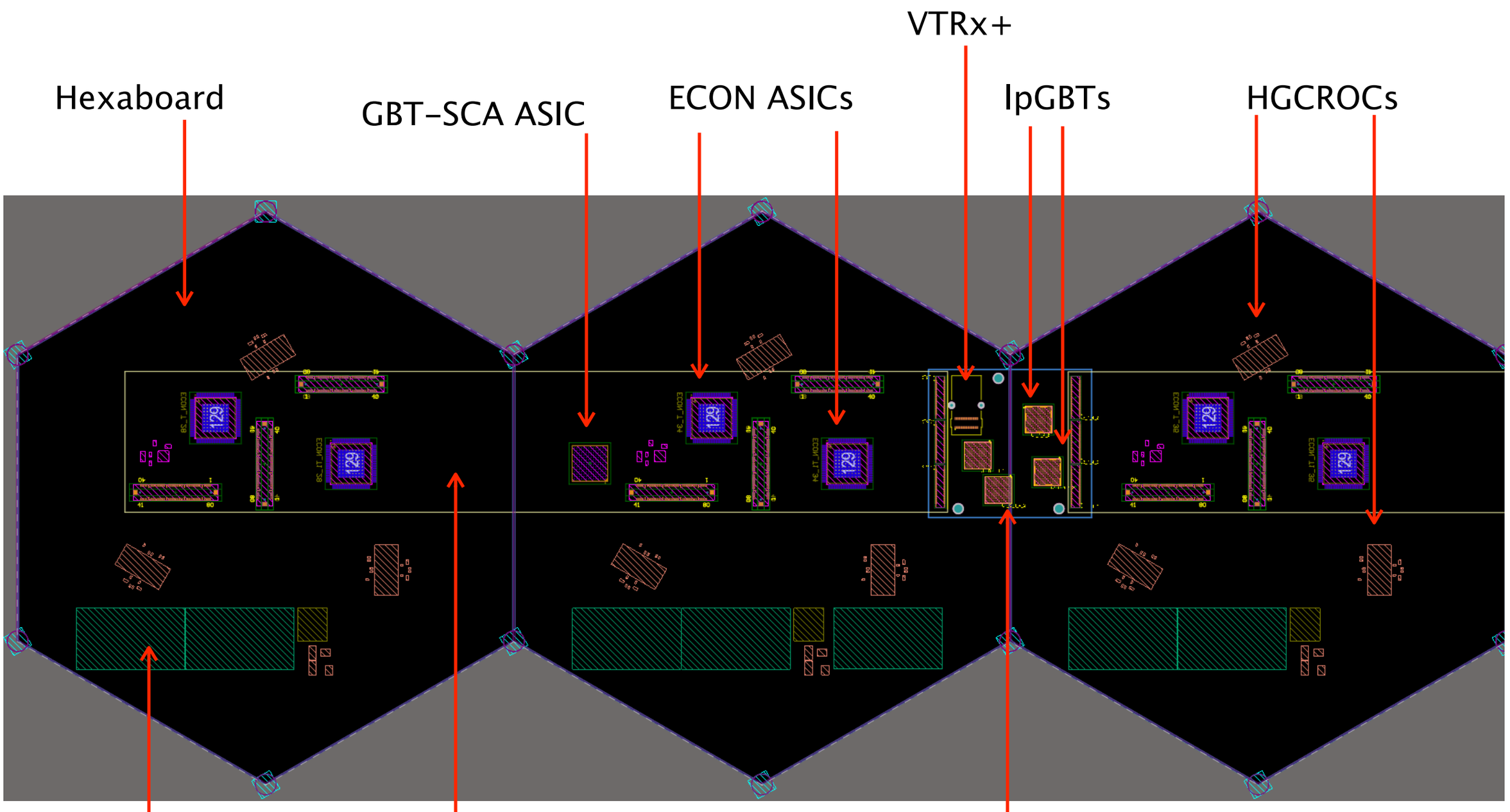
Charge #2



- Two data paths:
  - **40 MHz trigger (TRG) data:** ECON aggregates, selects/ compresses, serializes, and transmits to lpGBT.
  - **750 kHz of (DAQ) data:** On L1 accept, ECON applies zero suppression, aggregates, serializes, and transmits to lpGBT.

FE electronics architecture

Charge #2

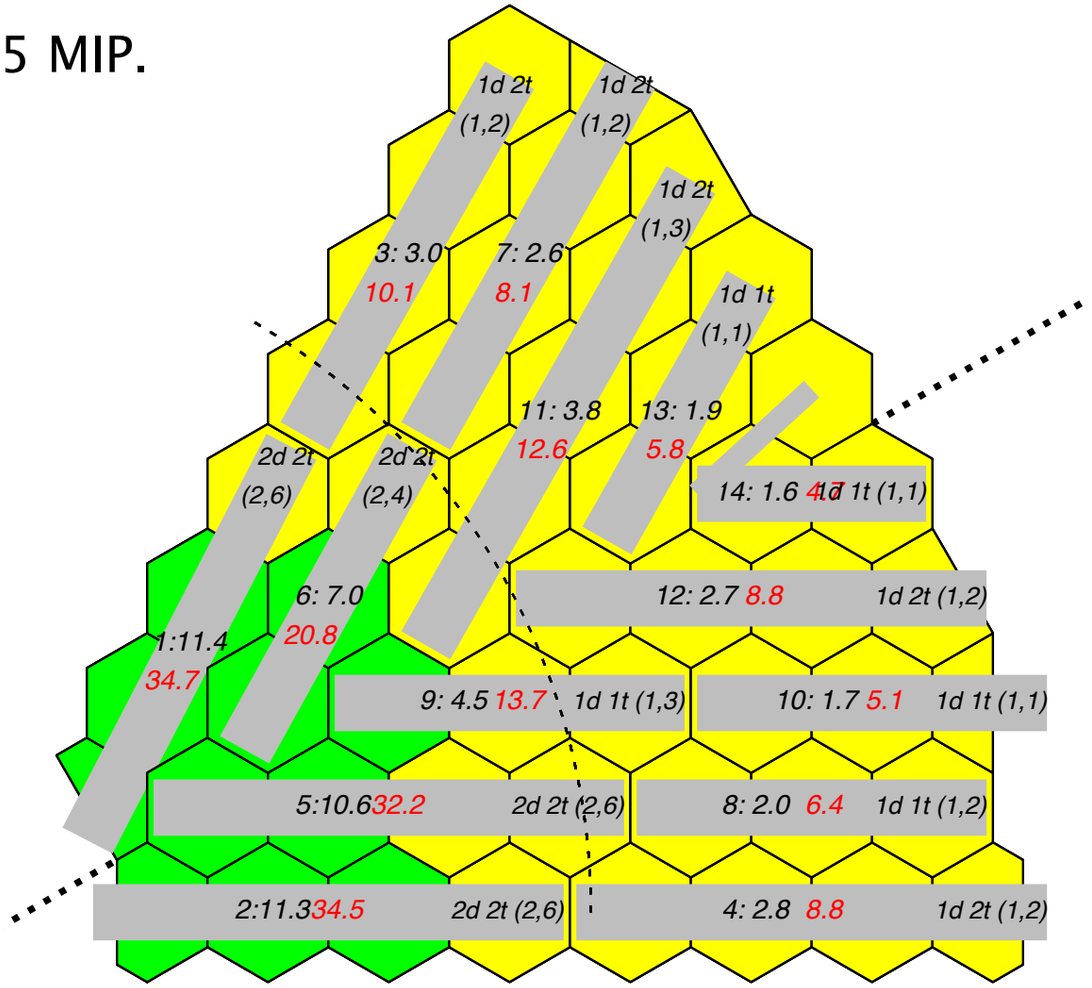


Occupancy and data rates

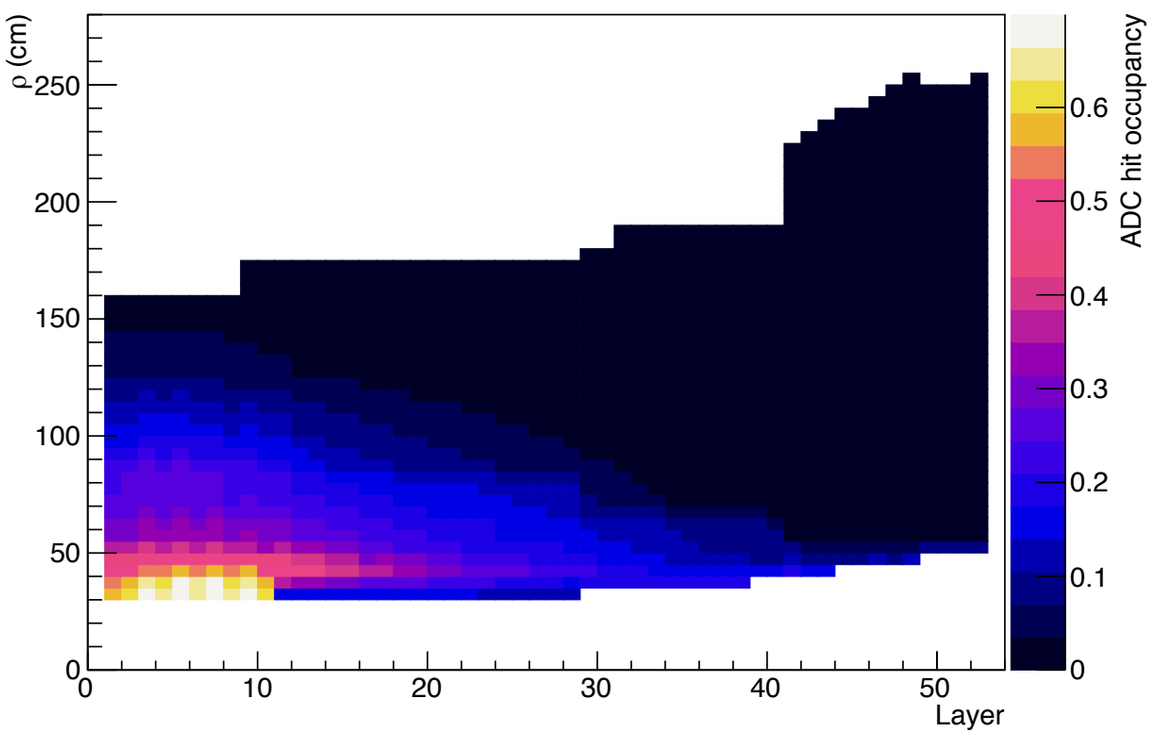
Charge #2

- Motherboard layout for 6th CE-E layer with data rates
  - Includes overhead associated with data headers, alignment patterns, etc.
- Red numbers are TRG data rates [Gbps]:
  - Based on simple threshold-based algorithm: read out all TRG data for channels with E>2 MIP_T and sum of energy in each ROC.
- Black numbers are DAQ data rates [Gbps] for E>0.5 MIP.
- Occupancy and data rates are well understood.

Layer 6 Module and Motherboard candidate layout



Occupancy vs. layer and radius



Conceptual design

Relevant requirements

Charge #2

- **EC-sci-engr-010**: radiation tolerance for 10 year HL-LHC operation.
  - **EC-engr-083**: ECON rad tolerant to 2 MGy, 1x10^{16} 1MeV-equivalent neutrons/cm^2, with SEU compliance
  - expect maximum of 300 kGy and 3x10^{16}/cm^2 on-detector

- **EC-sci-engr-011**: fit within evolving CMS HL-LHC upgrade requirements of interfacing systems.
  - **EC-engr-084**: ECON power consumption ≤5mW/channel

- **EC-sci-engr-008**: provide trigger info at 40 MHz w/ 5μs latency

- **EC-sci-engr-012**: readout bandwidth to accommodate luminosities up to 7.5e34/cm^2/s and trigger rates up to 750 kHz.
  - **EC-engr-081**: ECON TRG data transmission at 40MHz and DAQ data transmission at 750 kHz
  - **EC-engr-082**: ECON max latency is 16 BX

- Link: https://cms-docdb.cern.ch/cgi-bin/DocDB/ShowDocument?docid=13447

Basic ECON reqs/specs

Charge #2

- Trigger data transmission at 40 MHz
- DAQ data transmission at 750 kHz
- 16 BX latency for TRG path
  - Impacts maximum depth of buffers and architecture choices
- Radiation tolerance
  - Use 65 nm TSMC process
  - triple modular redundancy for registers and clocks
  - standard cell libraries characterized for latest radiation corners
  - extensive testing at prototype stage
- Low power
  - Use 65 nm TSMC process
  - Use power optimized design and algorithms
- Numbers of inputs/outputs
  - 12 inputs (1.28 Gbps), 14 outputs (1.28 Gbps)

ECON architecture choice

Charge #2,8

- ECON-related comments and recommendation from March 2019 CD-1 Director's Review (Dave Christian, Paul Derwent, Ping Gui):

Comments:

- ECON P1 consists of many analog, mixed signal and digital circuit blocks in a single chip with a BGA package with close-to-final pinout. Although some of the circuit blocks will be based on the existing ones in LpGBT as a starting point, it will still take much effort to understand the existing design, make necessary modifications, integrate, simulate and verify the performance. The design, verification and integration of all the blocks in a single chip takes large amount of manpower and coordination. The manpower of ASIC designers allocated to the project right now is barely minimal to complete the prototype I ASIC with the scheduled time period.

- Putting three channels of 10Gbps SCR+ENC+SER on a single chip not only increases the design complexity, but also introduces issues such as crosstalk and significantly increases the design risk.

- We are worried that, as currently envisioned, the first prototype of the ECON concentrator ASIC will take much longer to design than anticipated and will still have a significant risk of failure. We believe it would be safer to first design a prototype with 36 1.28 Gbps inputs and 7 1.28 Gbps outputs. This is the configuration required for ECON-D, and this configuration could also be used for ECON-T, albeit at the cost of a more complex printed circuit board design requiring more LpGBTs.

Recommendation: Consider the approach described above for the ECON ASICs to reduce schedule and performance risks.

- Summary :
  - ECON (P1) is a complex chip composed of analog, mixed, and digital blocks.
  - Person power for design and verification is barely sufficient.
  - Including 3x 10Gbps transmitter greatly increases design complexity and risk.
  - Consider design without 10Gbps transmitters.

ECON architecture choice

Charge #2,8

- Based on this **recommendation**, extensive **internal review**, and comprehensive **system optimization** studies, we have simplified ECON plan without impacting physics performance.

- New ECON architecture:
  - **Inputs** : 36x @ 1.28 Gbps ➔ 12x @ 1.28 Gbps
  - **Outputs** : 3x 10.24 Gbps ➔ 14x** @ 1.28 Gbps
  - **Package** : 18x18 Ball grid array ➔ 176-pin thin quad flat package
  - **Common pinout** for ECON-D and ECON-T

- Basic system idea : Use 1 ECON-T and 1 ECON-D per 8" module

** >12 needed to accommodate data headers in case that all channels are readout without supression.

ECON-T concept

Charge #2, #3

12 * 32b — **ePortRx + Word Aligner**

12 * 28b — **Switch matrix + Float ➔ Fix**

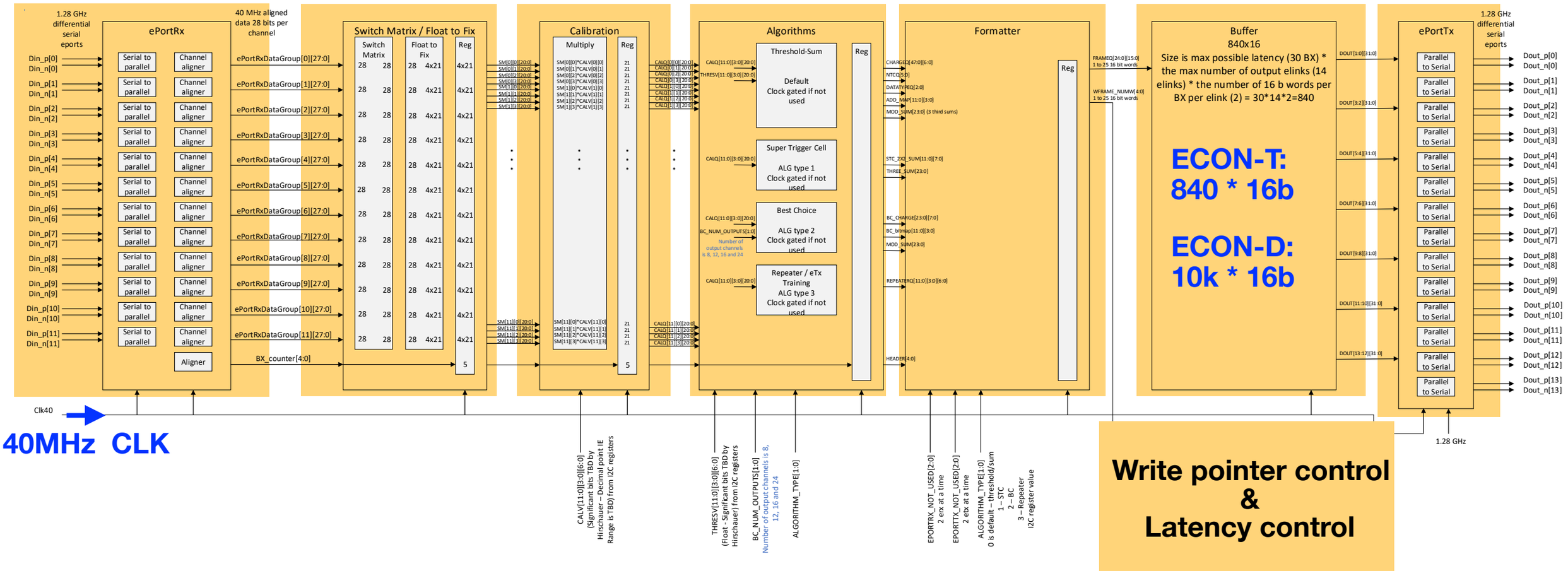
12 *4 * 21b — **Calib**

12 *4 * 21b — **Algorithms**

Various — **Formatter**

2 * 7 * 32b — **Buffer**

14 * 32b — **eTx**



- ECON-D inputs/outputs and architecture is the same, but RTL within each block differs.
- ePortRx + phase aligner from lpGBT

ECON development plan

Charge #3

	2019												2020												2021												2022				
	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M
Receivers			Design + Implementation																																							
Transmitters			Design + Implementation																																							
Control/Monitoring			Design + Implementation																																							
Algos / Data handling						Design + Implementation																																				
Verification						Verification																																				
Full chip assembly											Integration																															
ECON MPW																	Fab			Package		Radiation / Bench testing																				
HGCROC														Fab			Package		Radiation / Bench							System test																
Adjust / finalize																											Design + Implementation														
Verification																											Verification														
ECON Production																														Fab			Package		QC							
System testing														Full chip verification complete																					Radiation / system							
Milestones																																									
											Receiver complete						Submit prototype										Prototype complete						Submit production								ECON complete		
																	ECON ready for CD-2																									

- Initial plan (CD-1 Director's Review, March 2019) included two prototypes
  - prototype 1 : verify complex 10.24 Gbps transmitters
  - prototype 2 : verify whole chip
- With removal of 10.24 Gbps eTx, now planning single prototype for whole chip
  - Second prototype included as risk with 50% probability

ECON design features & philosophy

- **Simplified ECON ASICs** as much as possible without sacrificing physics performance. ✅
  - Use **common architecture** and pinout for ECON-D and ECON-T. ✅

- ECON ASICs are almost **100% digitial**
  - Primary mixed-signal components taken from lpGBT
  - Investment in top-end Cadence tools shifts resource needs from implementation ➔ RTL

- **Verification** is critical : capitalize on tools and extensive verification experience developed for DUNE ASICs. ✅

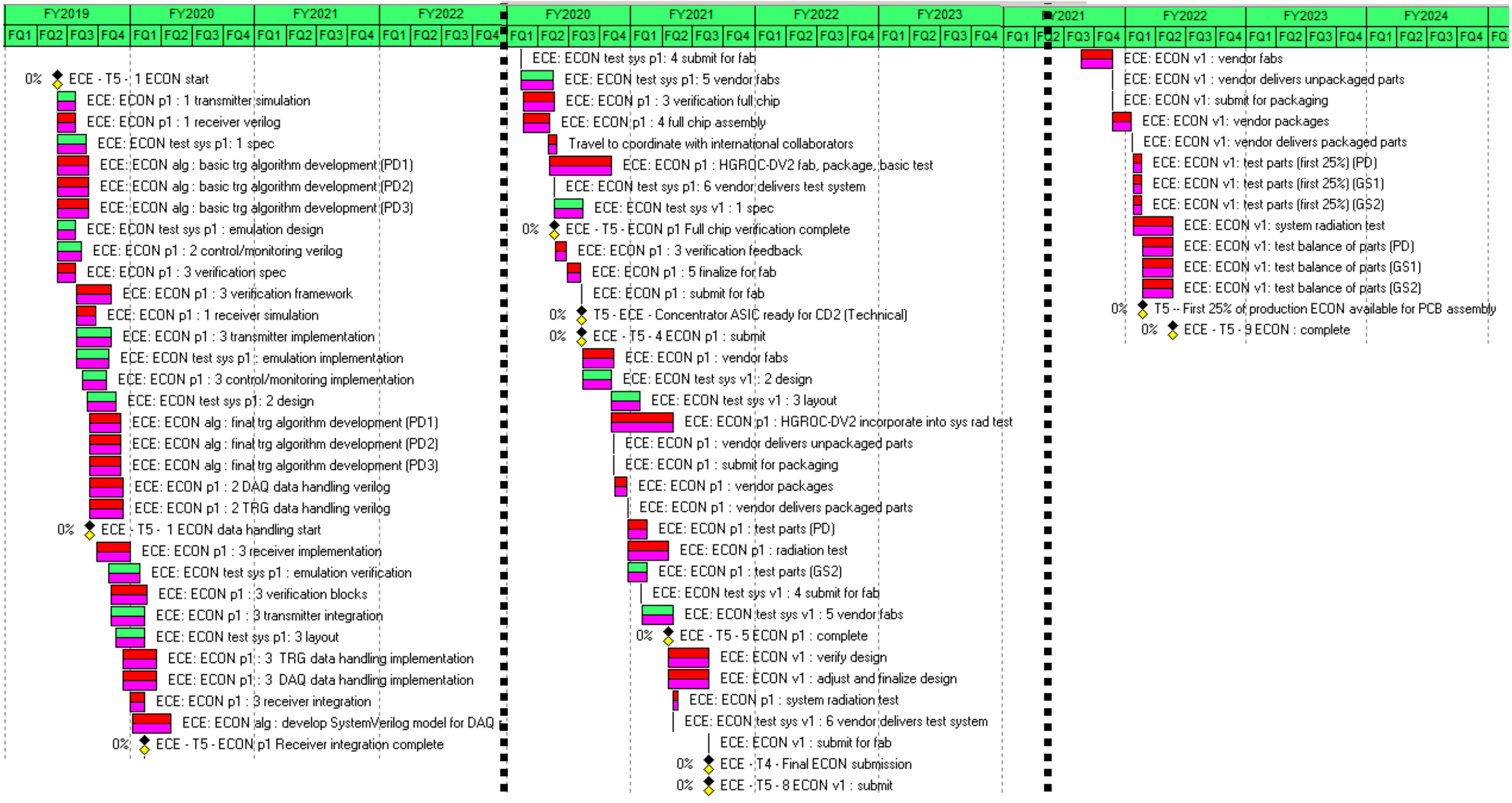
- **Modular design** simplifies timing closure and interactions among the team. ✅
  - Parallelism of modular design allows large team to make simultaneous progress.

- **Functionality built in** to allow independent and easy testing of individual blocks.
  - PRBS generator and comparator
  - Scan chains for testing triplicated components ✅

Cost and schedule

Schedule

Charge #3



ECON Milestones

Charge #3

- ECON interfaces to rest of project by supplying prototype and production ASICs for motherboard assembly ➔ each connection occurs in RLS at appropriate milestone.

Activity ID	Level	Activity	Date
ES30037C1	T5	Full chip verification complete	20-Feb-2020
ES30110	T5	Submit ECON prototypes for fabrication	08-May-2020
ES10280	T5	ECON prototypes complete	20-Jan-2021
ES30120	T5	Submit ECONs for production fabrication	20-May-2021
ES10660	T5	First 25% of production ECONs ready for PCB assembly	22-Nov-2021
ES19990	T5	ECON complete	23-Feb-2022

Cost estimate

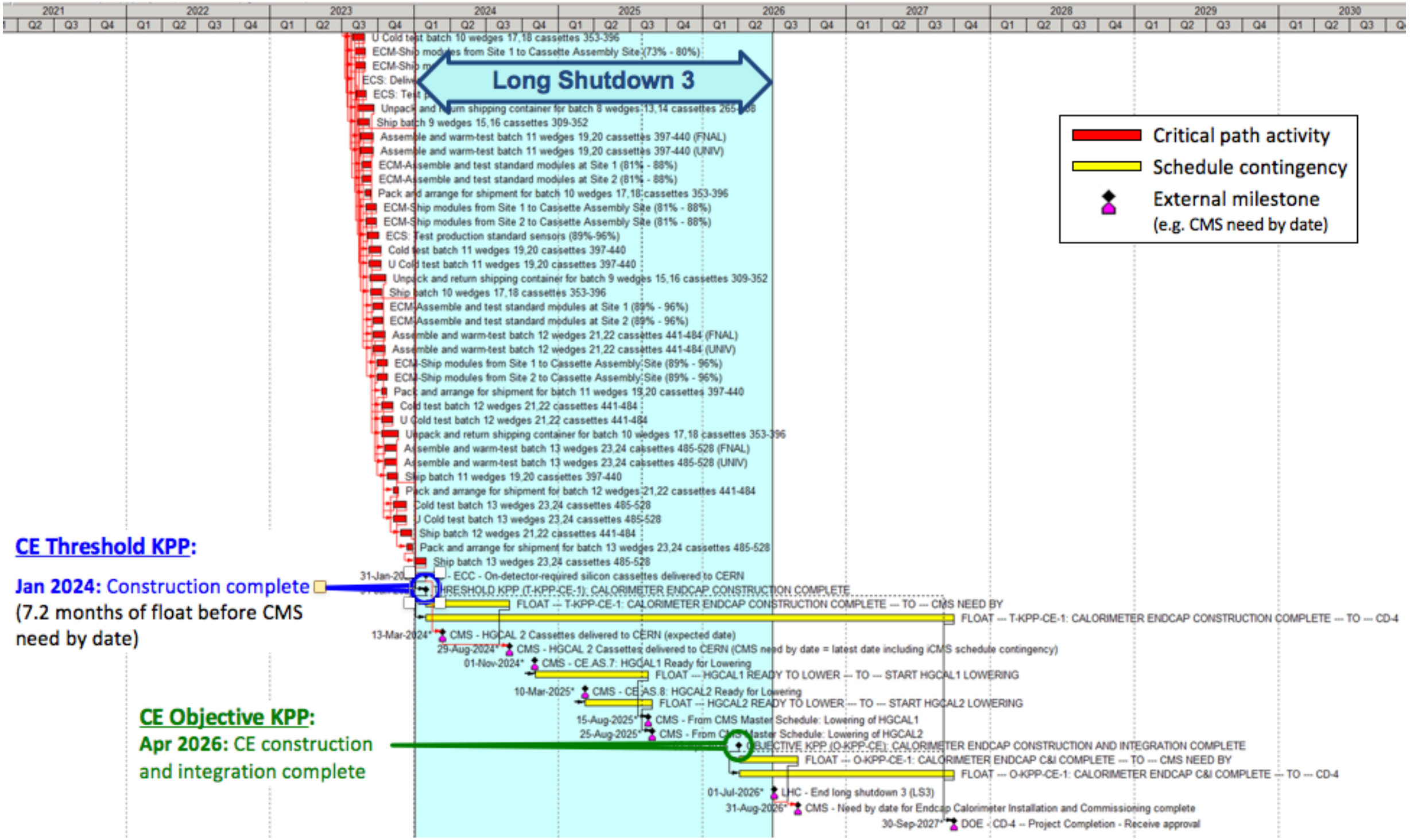
Charge #3

WBS	Direct M&S ($)	Labor (Hours)	FTE	Direct + Indirect + Esc. ($)	Estimate Uncertainty ($)	Total Cost ($)
DOE-CD1-402.4 402.4 CE - Calorimeter Endcap (at DOE CD1	21,051,786	332579	188.11	40,672,474	10,143,585	50,816,059
DOE-CD1-402.4.2 CE - Management	1,934,243	82022	46.39	3,807,266	622,019	4,429,285
DOE-CD1-402.4.3 CE - Sensors	7,501,635	14846	8.40	8,393,032	1,722,630	10,115,663
DOE-CD1-402.4.4 CE - Modules	2,932,730	96412	54.53	8,405,886	1,435,046	9,840,932
DOE-CD1-402.4.5 CE - Cassettes	3,677,813	47416	26.82	9,422,794	3,065,143	12,487,937
DOE-CD1-402.4.6 CE - Scintillator Calorimetry	2,084,047	60875	34.43	4,196,710	1,244,785	5,441,494
DOE-CD1-402.4.7 CE - Electronics and Services	2,921,318	31008	17.54	6,446,786	2,053,962	8,500,748
DOE-CD1-402.4.7.1 CE - Concentrator ASIC	1,516,100	27168	15.37	4,444,957	1,471,236	5,916,193
DOE-CD1-402.4.7.2 CE - Power System	1,405,218	3840	2.17	2,001,829	582,726	2,584,555

- Cost drivers (direct+indirect+esc):
  - ECON production & prod. packaging (M&S) : $0.752M + $0.568M
  - ECON design & verification (labor) : $1.874M (prototypes + production)
  - ECON testing (labor) : $0.859M (prototypes + production)

Critical path and float

Charge #3



CE Threshold KPP:

Jan 2024: Construction complete (7.2 months of float before CMS need by date)

CE Objective KPP:

Apr 2026: CE construction and integration complete

Critical path and float

Charge #3

- ECON is on critical path for start of silicon motherboard assembly:
  - 7 (2) month float for providing ECON prototype for scintillator (silicon) prototype motherboard verification.
  - 3 (-1) month float for providing final ECON for scintillator (silicon) motherboard assembly.
    - However, Motherboard Assembly has 4.5 months of float with respect to Cassette Assembly.
  - 7.2 month total US project float

- Greatest schedule risk is need for another round of ASIC prototype :
  - 7.5 month mean schedule impact

- More discussion at end of talk on how schedule can absorb ECON delays.

Risk : additional prototype run

Charge #3,7

RT-402-4-18-D CE - Additional concentrator ASIC engineering (MPW) run is required

Risk Rank:	3 (High) **Scores:** Probability : 4 (H) ; Cost: 2 (M) Schedule: 3 (H))	**Risk Status:**	Open
Summary:	Current planning includes the cost of two Multi-Project Wafer (MPW) prototype runs. If a significant flaw is observed after the second run, a third cycle may be required. This risk addresses the need an additional single run (either DAQ or TRG).		
Risk Type:	Threat	**Owner:**	James F Hirschauer
WBS:	402.4 CE - Calorimeter Endcap	**Risk Area:**	Technical Risk / Quality
Probability (P):	50%	**Technical Impact:**	0 (N) - negligible technical impact
Cost Impact:	PDF = 3-point - triangular Minimum = 164 k$ Most likely = 241 k$ Maximum = 385 k$ Mean = 263.3 k$ P * <Impact> = 132.0 k$	**Schedule Impact:**	PDF = 3-point - triangular Minimum = 6.0 months Most likely = 7.50 months Maximum = 9.0 months Mean = 7.5 months P * <Impact> = 3.75 months
Basis of Estimate:	Current planning includes the cost of two Multi-Project Wafer (MPW) prototype runs. If a significant flaw is observed after the second run, a third cycle may be required. This risk addresses the need an additional single run (either DAQ or TRG). The M&S costs are $136k for the MPW run and $28k for packaging. The labor cost for additional design work to fix the observed flaw is a 3-pt triangular PDF : 0/0.17/0.5 FTE. It is assumed the flaw is fairly easy to fix and the exact time needed depends on when when the issue is discovered, if in the beginning, middle, or end of the cycle. The additional testing is assumed to be modest and covered by the labor included for ASIC testing in the baseline. The min/likely/max cost is hence 164/209/295 k$. The L3 burn rate due to the delay of downstream activities is $21k/month (CMS-doc-13481), but there are 6 months of float available before cassette assembly is affected. therefore: Min cost = $164k + 0 = $164k. Likely cost = $209k + 1.5 months * $21k burn rate = $241k. Max cost = $295k + 3 months * $21k burn rate = $385k.		
Cause or Trigger:		**Impacted Activities:**	JM: Implemented in P6 between 'ECON p2 test parts' and 'ECON v1 finalize design'
Start date:	31-Aug-2020	**End date:**	30-Aug-2021
Risk Mitigations:	We will work closely with engineers to make sure that two planned engineering (MPW) runs are sufficient. We will be using some code blocks from the lpGBT that would have undergone some testing before the two MPW runs, and we will be including the prototype ECON ASIC in a major system prototype vertical slice test before the production run.		
Risk Responses:	Request additional funding for a third MPW run and for design changes. Reduce the needed testing time. Accelerate or parallelize the production of the motherboards if possible and if needed accelerate the cassette assembly and testing. The cost of accelerating the assembly of cassettes is covered by a separate risk.		
More details:	CMS-doc-13481		

Risk : additional production run

Charge #3,7

RT-402-4-04-D CE - Concentrator does not meet specifications

Risk Rank:	2 (Medium) **Scores:** Probability : 2 (L) ; Cost: 3 (H) Schedule: 3 (H))	**Risk Status:**	Open
Summary:	If the concentrator ASIC does not meet specifications after the production masks are produced then an additional set of masks will need to be produced and additional engineering effort is required to adjust the design so that the ASIC meet specifications. The risk probability depends on how many engineering/multi-project wafer runs are done and tested before the production masks are produced, and also on the exact maturity of the design (progress made), and on the schedule, e.g. if all irradiation tests can be done before the production masks are fabricated. The full packaging costs are realized only once since we would find the problem before packaging. The masks will include both TRG and DAQ chips.		
Risk Type:	Threat	**Owner:**	James F Hirschauer
WBS:	402.4 CE - Calorimeter Endcap	**Risk Area:**	Technical Risk / Requirements
Probability (P):	10%	**Technical Impact:**	2 (M) - significantly substandard
Cost Impact:	PDF = 3-point - triangular Minimum = 907 k$ Most likely = 971 k$ Maximum = 1,035 k$ Mean = 971.0 k$ P * <Impact> = 97.0 k$	**Schedule Impact:**	PDF = 3-point - triangular Minimum = 6.0 months Most likely = 7.50 months Maximum = 9.0 months Mean = 7.5 months P * <Impact> = 0.75 months
Basis of Estimate:	The M&S cost is $690k for masks and wafer and $25k for a single set up to package a few chips. The labor cost for the additional engineering effort is a 3-pt triangular PDF: 0.25-0.375-0.5 FTE. The min/likely/max cost is hence 781/813/846 k$. The L3 burn rate due to the delay of downstream activities is $21k/month (CMS-doc-13481). Min cost = $781k + 6 month * $21k burn rate = $907k. Likely cost = $813k + 7.5 months * $21k burn rate = $971k. Max cost = $846k + 9 months * $21k burn rate = $1035k.		
Cause or Trigger:	Concentrator ASIC as returned from production does not meet specification despite the two previous multi-project wafer runs (MPWs)	**Impacted Activities:**	
Start date:	30-Aug-2021	**End date:**	29-Aug-2022
Risk Mitigations:	This risk is mitigated by prototyping and testing the full design through two multi-project wafer submissions, and by design and production reviews. The ASICs from these will be used in full vertical slice tests, as well as beam tests and irradiation tests.		
Risk Responses:	To reduce the impact due to the delay of this ASIC we will need to implement a combination of the following: accelerate the production and testing of motherboards (MB) once the ASIC is available, and also the assembly of cassettes; do more assembly and testing in parallel for pieces that do not require the ASIC (for the MB), or that do not require the MB, to minimize the time to complete assembly of the MB and cassettes, and to minimize the time needed to for tests.		
More details:	CMS-doc-13481		

Contributing institutions and resource optimization

Resources and optimization

Charge #4,5

- Fermilab is the only US group with sufficient expertise and person power for ECON design.
- All work will be done by vendors except design and testing.
- Design for 1.28 Gbps receivers will be taken from lpGBT.
- Overall architecture, pinout, I/O, verification framework for ECON-T and ECON-D will be common.

- **FNAL Physicist :** 15+ yrs HEP / 5+ yrs Upgrade Coordination experience
  - ***Co-coordinator****: specification, ASIC and system architecture*
- **FNAL Engineer 1** : 15+ yrs digital experience in ASIC industry
  - ***Co-coordinator****: specification, ASIC architecture, top-level chip integration, RTL for some blocks*
- **FNAL Engineer 2:** 20+ yrs system/PCB/FPGA experience & HGCAL system design
  - *Specification, ASIC and system architecture*
- **FNAL Engineer 3**: 5+ yrs digital design experience
  - *Coordinate implementation (RTL ➔ physical design) and integrate lpGBT 1.28 Gbps receivers*
- **FNAL Engineer 4**: 10+ years of mixed signals design experience
  - *Design 1.28 Gbps transmitters and integrate lpGBT PLL*
- **Visiting engineer** : 40 years digital design experience
  - *RTL for various blocks and implementation*
- **FNAL Engineer 5**: 20+ yrs digital design and verification experience
  - *Coordinate verification*
- **FNAL Engineer 6**: 20+ yrs verilog/HDL experience
  - *Verification*
- **FNAL Engineer 7**: 10+ yrs in ASIC design support
  - *Tools support, RTL, implementation, and verification*
- **University of Split /FESB, Croatia:** 3 elec eng faculty with RTL and synthesis experience
  - *RTL for ECON algorithms*
- **LLR, Paris :** Electrical engineer and physicist with RTL experience
  - *RTL for ECON algorithms*
- **FNAL, Florida Tech University, Northwestern University :** Scientist, 2 post docs, 2-4 students
  - *Specification and verification*

Color code
- **ASIC design**
- **Verification**
- **External RTL design**
- **Specification, architecture, support**

Quality assurance and control

Charge #6

- Conforms to cms-doc-13093

- Quality assurance
  - Design will be based on results of extensive verification :
    - Power integrity with Cadence Voltus
    - ASIC- and system-level data integrity with SystemVerilog + Universal Verification Methodology
  - Modular design of internal block allows simplicity of interface
  - Designs include functionality to simplify testing
  - Prototype will undergo radiation and accelerated aging tests.
  - Vertical slice tests will be performed with prototype

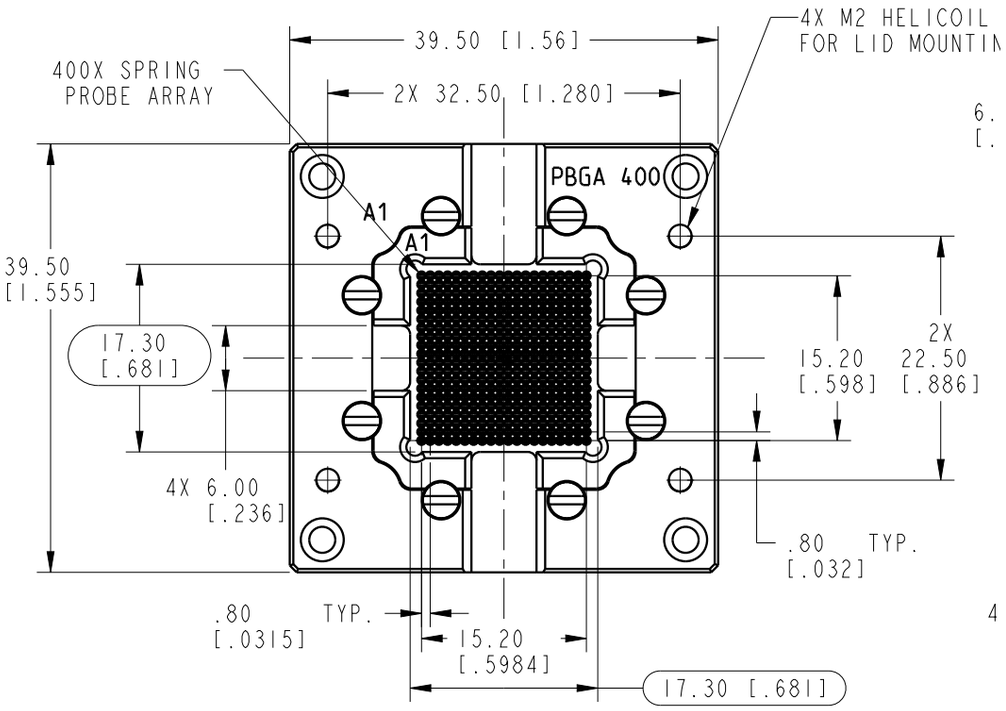
- Quality control
  - Full functionality of all ASICs will be tested with robotic ASIC tester.
  - Sample of production run will undergo radiation and accelerated aging tests.

ECON testing

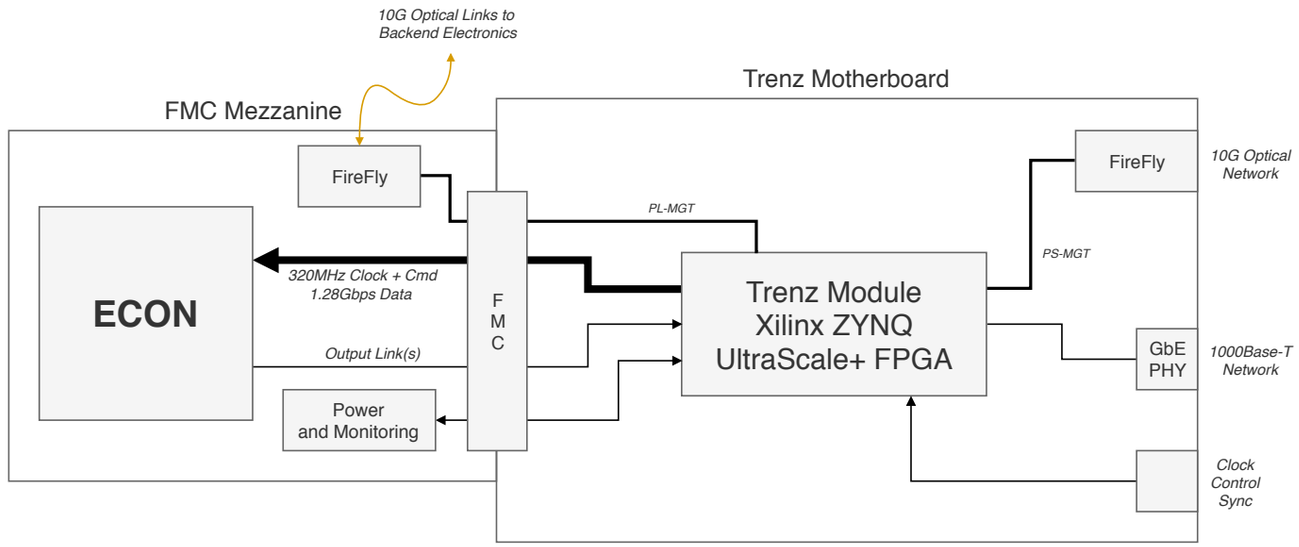
Charge #6

- Prototype / single chip evaluation
  - Must be ready to test ECON prototype immediately in Sep 2020.
  - System based on MPSoC w/ Zynq UltraScale+ FPGA
  - Will allow standalone testing of precise timing characteristics and coarse logic-level testing.
  - Will also serve as ECON emulator in early vertical slice tests.
- Robotic test system for 100 -10k parts
  - based on prototype test system and extensive robot test experience at FNAL

Candidate socket for robotic ASIC tester



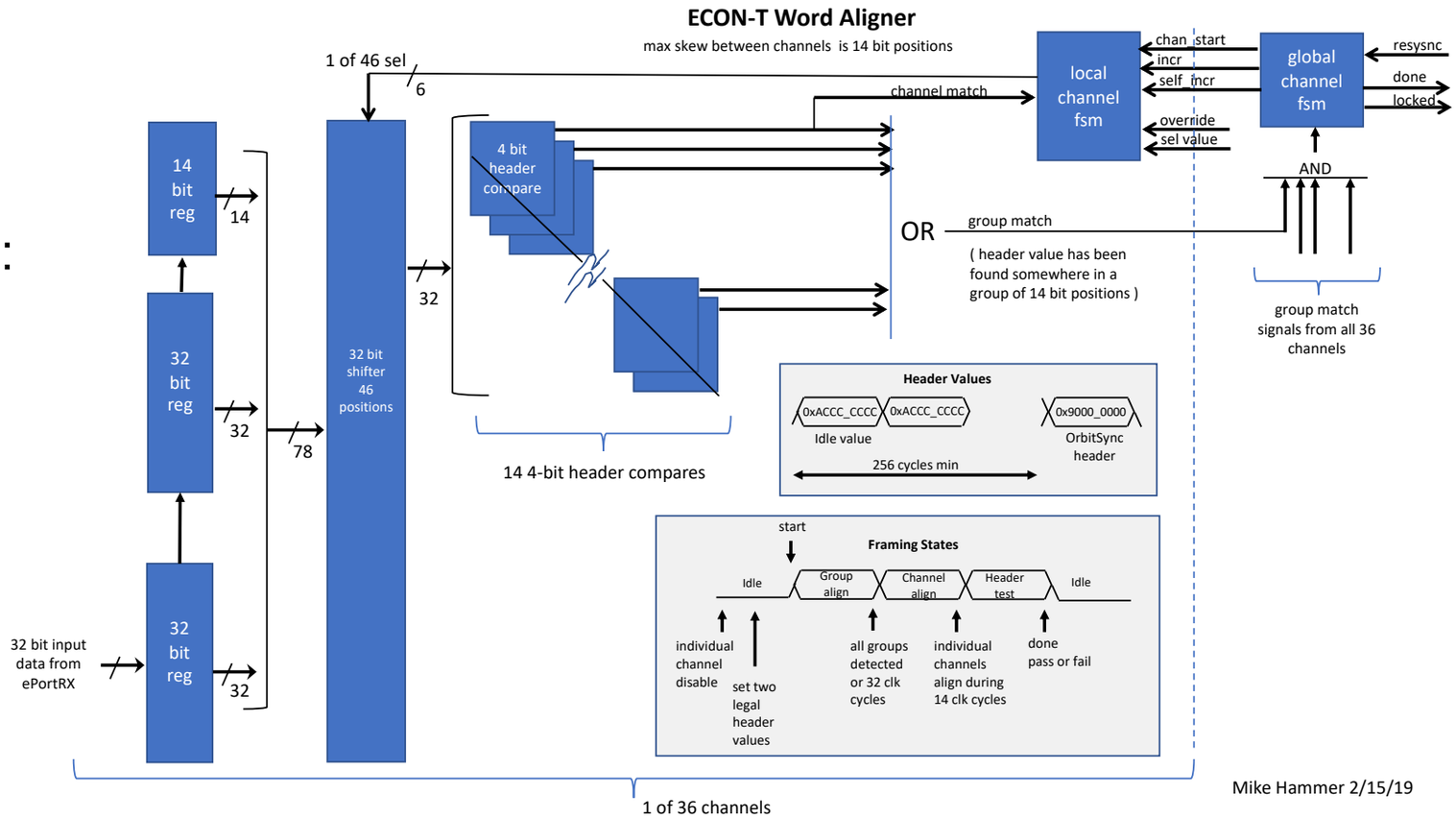
ECON TEST PLATFORM (physical)



Recent ECON technical progress

1.28 Gbps receivers

- ePortRx (from lpGBT) performs bit aligment
- Word aligner aligns for all elinks:
  - 32-bit word boundaries
  - LHC orbit signals
- Includes built-in PRBS comparator for testing receiver



Status

- RTL complete
- Full implementation in progress
  - including triplication and scan chains
  - serves as commissioning of full design chain (RTL ➔ schematic ➔ layout)

Verification

- Excellent progress setting up verification framework
  - Based on industry standard **System Verilog + Universal Verification Methodology**
  - **Universal Verification Components** (UVCs) implemented for all basic registers, fast commands, i2c, ePortRx, Word Aligner.
  - **Test bench implemented** implemented.
  - Successfully **passing data** sequences through test bench.
  - **Configuration makefile system** developed to allow efficient testing with multiple parties.

Screenshot of UVM structure for FastCommand coverage

```
covergroup FastCommand_Bits_cg @(negedge FastCommand_interface_IO.FCmdClk_p);
  bitPoint    : coverpoint {FastCommand_interface_IO.FCmdData_p, FastCommand_interface
    bins          bitZero   = {2'b01};
    bins          bitOne    = {3'b10};
    illegal_bins  illegal   = default;
  }
endgroup

covergroup FastCommand_Trans_cg @(posedge caughtNewTrans);
  goodCommands : coverpoint captured_fCommWord {
    bins Idle                     = { FCOM_IDLE                     };
    bins OrbitSync                = { FCOM_ORBITSYNC                };
    bins L1A_Normal               = { FCOM_L1A_NORMAL               };
    bins L1A_Normal_OrbitSync     = { FCOM_L1A_NORMAL_ORBITSYNC     };
    bins L1A_Full                 = { FCOM_L1A_FULL                 };
    bins L1A_Full_OrbitSync       = { FCOM_L1A_FULL_ORBITSYNC       };
    bins OrbitCountReset_OrbitSync = { FCOM_ORBITCOUNTRESET_ORBITSYNC };
    bins CalibrationReq           = { FCOM_CALIBRATIONREQ           };
    bins CalibrationL1A_L1A_Normal = { FCOM_CALIBRATIONREQ_L1A_NORMAL };
    bins CalibrationL1A_L1A_Full  = { FCOM_CALIBRATIONREQ_L1A_FULL   };
    bins Resync_L1A_Full          = { FCOM_RESYNC_L1A_FULL          };
    bins Link_Reset               = { FCOM_LINK_RESET               };

    illegal_bins Forbidden_0110   = { FCOM_FORBIDDEN_0110           };
    illegal_bins Forbidden_1100   = { FCOM_FORBIDDEN_1100           };
    illegal_bins Forbidden_1101   = { FCOM_FORBIDDEN_1101           };
    illegal_bins Forbidden_1110   = { FCOM_FORBIDDEN_1110           };
  }
  badCommands : coverpoint captured_fCommWord {
  bins bad_000                  = { [8'b000_00000: 8'b000_11111] };
  bins bad_001                  = { [8'b001_00000: 8'b001_11111] };
  bins bad_010                  = { [8'b010_00000: 8'b010_11111] };
  bins bad_011                  = { [8'b011_00000: 8'b011_11111] };
  bins bad_100                  = { [8'b100_00000: 8'b100_11111] };
  bins bad_101                  = { [8'b101_00000: 8'b101_11111] };
  bins bad_111                  = { [8'b111_00000: 8'b111_11111] };
  }
  syncBit : coverpoint captured_fCommWord0;
endgroup
```

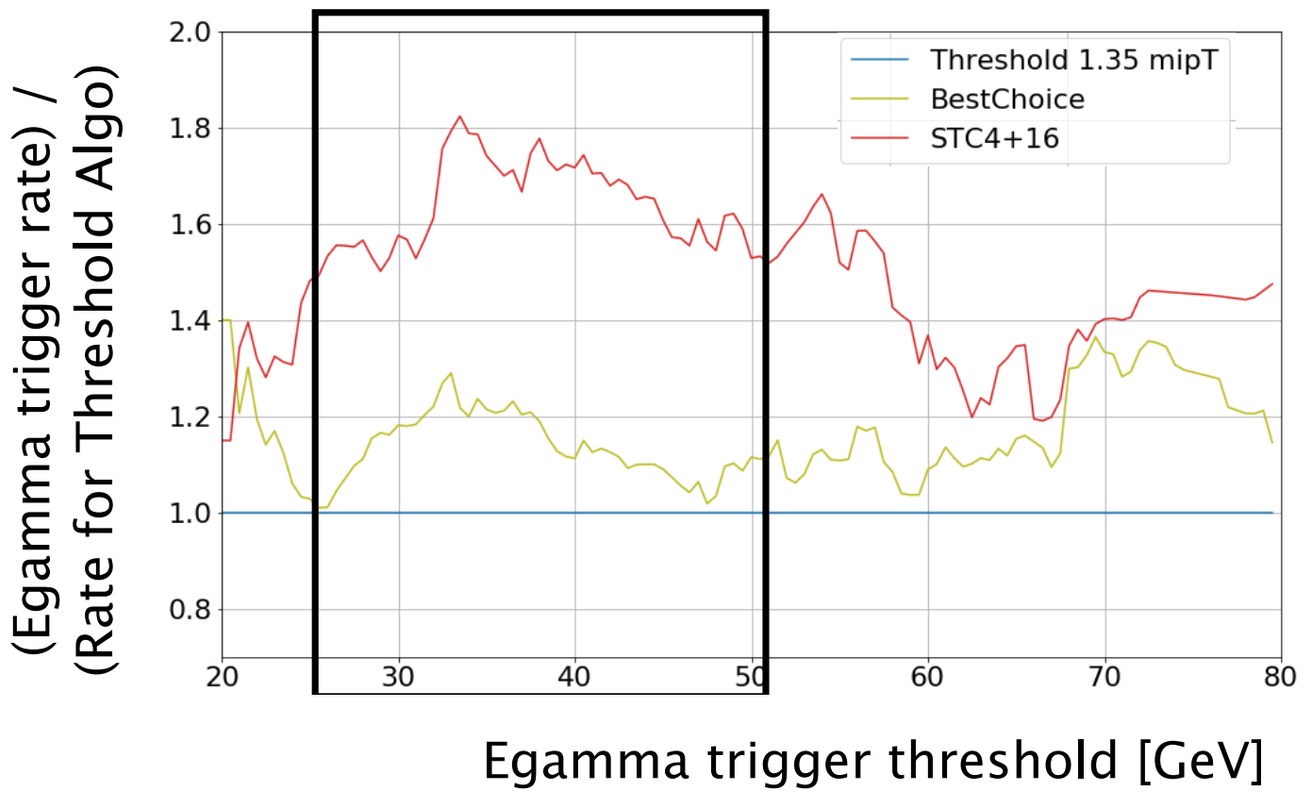
Block status

- RTL complete for
  - ePortRx
  - Word aligner (synthesis complete)
  - Switch matrix (synthesis complete)
  - Fast command interpreter/handler
  - Slow control via I2C
- Design in progress for
  - 1.28 Gbps transmitter
  - Latency control for ECON-T
  - Trigger algorithms for ECON-T
  - Zero suppression algorithm for ECON-D

Trigger algorithms

- Comprehensive, 1.5-year study of trigger algorithms completed this summer. Studied:
  - Performance for electrons/photons, taus, jets, VBF jets at 0, 140, and 200 PU
  - Resolution and discrimination (w.r.t. pions, PU, etc) ➔ trigger rates and thresholds

- Considered 3 algorithms for selecting trigger cell (TC) data:
  - **Threshold** (Variable length / variable format): transmit all TC with charge exceeding programmable threshold
  - **Best choice** (Fixed length / variable format) : sort TC and transmit N TC with highest charge
  - **Super TC** (Fixed length / fixed format) : combine TC laterally into "Super TC," transmit charge and position data for all Super TC



- Two viable options:
  - **Threshold** in ECAL and HCAL
  - **Best Choice** in ECAL + **Super TC** in HCAL

Design maturity & path to CD-2

Charge #1,2,7

- Documented in cms-doc-13417
- ECON conceptual design is complete
  - ECON selected over lpGBT-based alternative based on value engineering principles.
  - ECON & system architecture optimized settling on 12-in/14-out architecture
  - Development plan understood and on track.
  - Risks determined and documented.
- ECON preliminary design in nearly complete
  - Interfaces identified
  - QA plan developed
  - Lessons learned incorporated
  - RLS + contingency analysis developed
  - Baseline design/architecture chosen
  - Component designs/methods ~67% complete
- Path to CD-2 is clear for ECON
  - Design will be complete, verified, and ready for submission in May 2020

Summary

- ECON is required to manage transmission of data off detector.
- Based on external/internal reviews and system optimization, ECON design has been **significantly simplified**.
- ECON **design maturity** is nearing full "preliminary" status.
- ECON is on track for **CD-2 readiness** in May 2020.
- Cost, schedule, and risks are understood.

Additional material

Radiation requirements

Charge #2

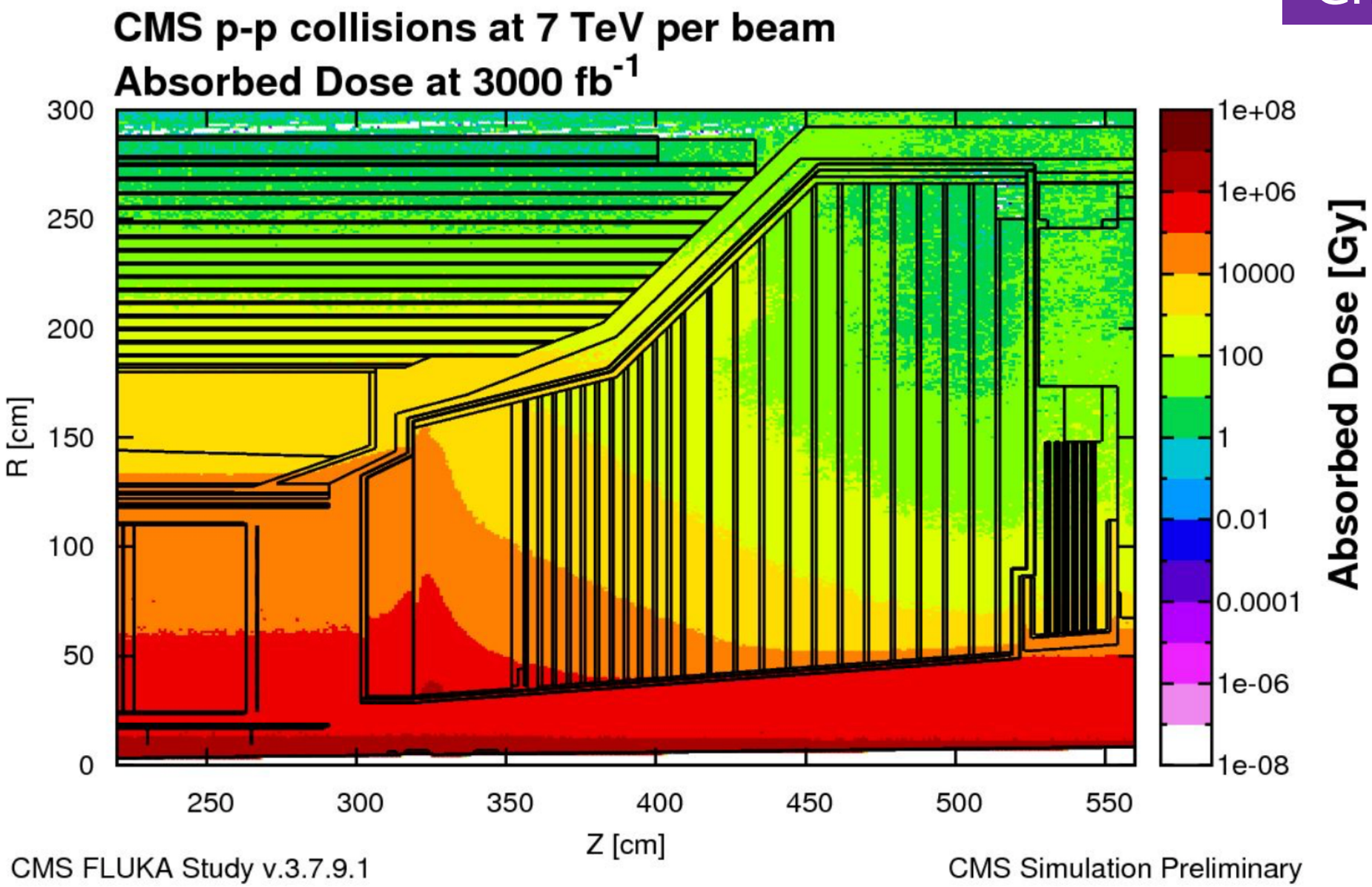


Figure 1.1: Dose of ionizing radiation accumulated in HGCAL after an integrated luminosity of3000 fb^{-1}, simulated using the FLUKA program, and shown as a two-dimensional map in the radial and longitudinal coordinates, r and z.

Radiation requirements

Charge #2

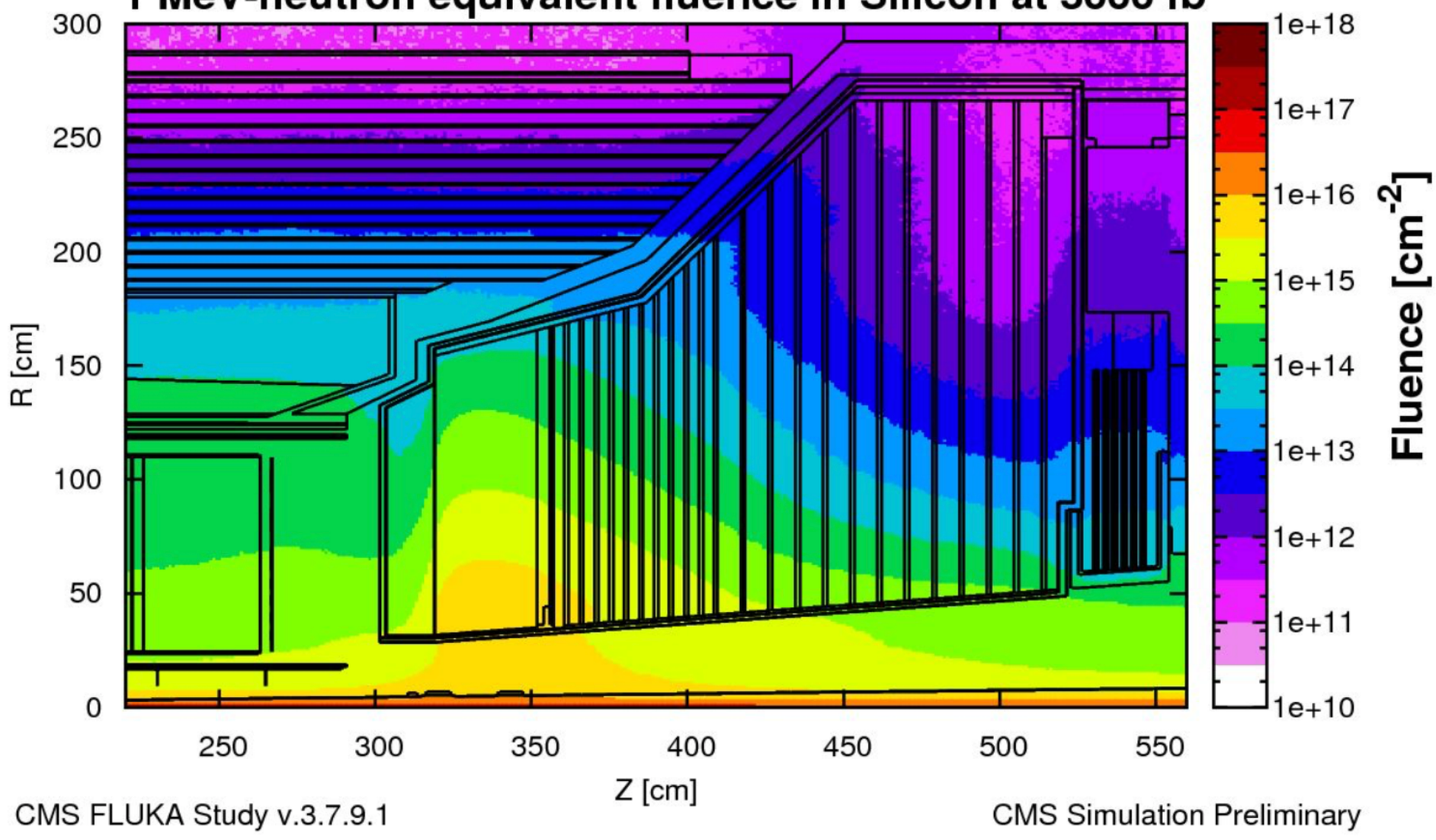


Figure 1.2: Fluence, parameterized as a fluence of 1 MeV equivalent neutrons, accumulated in HGCAL after an integrated luminosity of3000 fb^{-1}, simulated using the FLUKA program, and shown as a two-dimensional map in the radial and longitudinal coordinates, r and z.

ESH

Charge #6

- All ES&H aspects of the HL LHC CMS Detector Upgrade Project will be handled in accordance with the Fermilab Integrated Safety Management approach, and the rules and procedures laid out in the Fermilab ES&H Manual (FESHM).

- We are following our Integrated Safety Management Plan (cms-doc-13395) and have documented our hazards in the preliminary Hazard Awareness Report (cms-doc-13394).

- In general, safety is achieved through standard Lab/Institute practices
  - No construction, accelerator operation, or exotic fabrication
  - No imminent peril situations or unusual hazards
  - Items comply with local safety standards in site of fabrication and operation
  - Site Safety officers at Institutes identified in the SOW

- Specific hazards are ionizing radiation during ASIC testing and mechanical hazards during operation of robotic ASIC tester.

ECON MPW activities

ity ID	Activity Name	Start	Finish	Planned Duration	Planned Total Cost	Planned Labor Units
ES10071	ECE: ECON p1 : 1 receiver simulation	26-Apr-19	21-Jun-19	40d	$67,567.98	440h
ES10070	ECE: ECON p1 : 1 receiver verilog	01-Mar-19	25-Apr-19	40d	$67,567.98	440h
ES10010	ECE: ECON p1 : 1 transmitter simulation	01-Mar-19	25-Apr-19	40d	$49,140.35	320h
ES30035	ECE: ECON p1 : 2 control/monitoring verilog	01-Mar-19	10-May-19	50d	$73,710.53	480h
ES30031	ECE: ECON p1 : 2 DAQ data handling verilog	03-Jun-19	10-Sep-19	70d	$42,997.81	280h
ES30180	ECE: ECON p1 : 2 TRG data handling verilog	03-Jun-19	10-Sep-19	70d	$42,997.81	280h
ES30170	ECE: ECON p1 : 3 DAQ data handling implementation	11-Sep-19	19-Dec-19	70d	$44,167.36	280h
ES30036	ECE: ECON p1 : 3 TRG data handling implementation	11-Sep-19	19-Dec-19	70d	$44,167.36	280h
ES30032	ECE: ECON p1 : 3 control/monitoring implementation	13-May-19	22-Jul-19	50d	$73,710.53	480h
ES30033	ECE: ECON p1 : 3 receiver implementation	24-Jun-19	01-Oct-19	70d	$119,837.79	780h
ES30033A	ECE: ECON p1 : 3 receiver integration	02-Oct-19	12-Nov-19	30d	$53,986.83	340h
ES30034	ECE: ECON p1 : 3 transmitter implementation	26-Apr-19	05-Aug-19	70d	$85,995.62	560h
ES30034A	ECE: ECON p1 : 3 transmitter integration	06-Aug-19	12-Nov-19	70d	$87,290.47	560h
ES30037B	ECE: ECON p1 : 3 verification blocks	06-Aug-19	19-Nov-19	75d	$176,358.85	1130h
ES30037D	ECE: ECON p1 : 3 verification feedback	21-Feb-20	26-Mar-20	25d	$61,926.07	390h
ES30037A	ECE: ECON p1 : 3 verification framework	26-Apr-19	05-Aug-19	70d	$162,777.42	1060h
ES30037C	ECE: ECON p1 : 3 verification full chip	20-Nov-19	20-Feb-20	60d	$142,906.32	900h
ES30037	ECE: ECON p1 : 3 verification spec	01-Mar-19	25-Apr-19	40d	$92,138.16	600h
ES30038	ECE: ECON p1 : 4 full chip assembly	20-Nov-19	06-Feb-20	50d	$88,919.49	560h
ES30039	ECE: ECON p1 : 5 finalize for fab	27-Mar-20	07-May-20	30d	$60,973.36	384h
ES10320	ECE: ECON p1 : HGROC-DV2 fab, package, basic test	04-Feb-20	05-Aug-20	130d	$0.00	0h
ES10420	ECE: ECON p1 : HGROC-DV2 incorporate into sys rad test	06-Aug-20	01-Feb-21	120d	$0.00	0h
ES10270	ECE: ECON p1 : radiation test	22-Sep-20	20-Jan-21	80d	$0.00	640h
ES10150	ECE: ECON p1 : submit for fab	08-May-20	08-May-20	1d	$0.00	0h
ES10210	ECE: ECON p1 : submit for packaging	13-Aug-20	13-Aug-20	1d	$0.00	0h
ES10480	ECE: ECON p1 : system radiation test	02-Feb-21	15-Feb-21	10d	$0.00	640h
ES30140	ECE: ECON p1 : test parts (GS2)	22-Sep-20	16-Nov-20	40d	$0.00	0h
ES10240	ECE: ECON p1 : test parts (PD)	22-Sep-20	16-Nov-20	40d	$0.00	320h
ES10230	ECE: ECON p1 : vendor delivers packaged parts	21-Sep-20	21-Sep-20	1d	$55,989.40	0h
ES10200	ECE: ECON p1 : vendor delivers unpackaged parts	12-Aug-20	12-Aug-20	1d	$157,283.20	0h
ES10160	ECE: ECON p1 : vendor fabs	11-May-20	11-Aug-20	65d	$0.00	0h
ES10220	ECE: ECON p1 : vendor packages	14-Aug-20	18-Sep-20	25d	$0.00	0h

ECON production activities

Activity ID	Activity Name	Start	Finish	Planned Duration	Planned Total Cost	Planned Labor Units
ES10520	ECE: ECON v1 : adjust and finalize design	21-Jan-21	19-May-21	85d	$96,526.75	560h
ES10530	ECE: ECON v1 : submit for fab	20-May-21	20-May-21	1d	$0.00	0h
ES10580	ECE: ECON v1 : vendor delivers unpackaged parts	24-Aug-21	24-Aug-21	1d	$752,393.73	0h
ES10540	ECE: ECON v1 : vendor fabs	21-May-21	23-Aug-21	65d	$0.00	0h
ES10521	ECE: ECON v1 : verify design	21-Jan-21	19-May-21	85d	$137,895.36	800h
ES10590	ECE: ECON v1: submit for packaging	25-Aug-21	25-Aug-21	1d	$0.00	0h
ES10650	ECE: ECON v1: system radiation test	25-Oct-21	22-Feb-22	80d	$0.00	320h
ES30010	ECE: ECON v1: test balance of parts (GS1)	22-Nov-21	22-Feb-22	60d	$0.00	0h
ES30020	ECE: ECON v1: test balance of parts (GS2)	22-Nov-21	22-Feb-22	60d	$0.00	0h
ES30000	ECE: ECON v1: test balance of parts (PD)	22-Nov-21	22-Feb-22	60d	$0.00	320h
ES10630	ECE: ECON v1: test parts (first 25%) (GS1)	25-Oct-21	19-Nov-21	20d	$0.00	0h
ES10640	ECE: ECON v1: test parts (first 25%) (GS2)	25-Oct-21	19-Nov-21	20d	$0.00	0h
ES10620	ECE: ECON v1: test parts (first 25%) (PD)	25-Oct-21	19-Nov-21	20d	$0.00	320h
ES10610	ECE: ECON v1: vendor delivers packaged parts	22-Oct-21	22-Oct-21	1d	$568,144.62	0h
ES10600	ECE: ECON v1: vendor packages	26-Aug-21	21-Oct-21	40d	$0.00	0h
ES30111	T5 - ECE - Concentrator ASIC ready for CD2 (Technical)		08-May-20	0d	$0.00	0h
ES10660	T5 -- First 25% of production ECON available for PCB assembly	22-Nov-21		0d	$0.00	0h

ECON Milestones

DOE-CD1-402.4.7.1 CE - Concentrator ASIC		01-Mar-19	23-Feb-22	748d	$4,444,957.04	21312h
ES30125	ECE - T4 - Final ECON submission		20-May-21	0d	$0.00	0h
ES30190	ECE - T5 - 1 ECON data handling start	03-Jun-19*		0d	$0.00	0h
ES10000	ECE - T5 - 1 ECON start	01-Mar-19*		0d	$0.00	0h
ES30110	ECE - T5 - 4 ECON p1 : submit		08-May-20	0d	$0.00	0h
ES10280	ECE - T5 - 5 ECON p1 : complete		20-Jan-21	0d	$0.00	0h
ES30120	ECE - T5 - 8 ECON v1 : submit		20-May-21	0d	$0.00	0h
ES19990	ECE - T5 - 9 ECON : complete		23-Feb-22	0d	$0.00	0h
ES30037C1	ECE - T5 - ECON p1 Full chip verification complete		20-Feb-20	0d	$0.00	0h
ES30033A1	ECE - T5 - ECON p1 Receiver integration complete		12-Nov-19	0d	$0.00	0h
ES30111	T5 - ECE - Concentrator ASIC ready for CD2 (Technical)		08-May-20	0d	$0.00	0h
ES10660	T5 -- First 25% of production ECON available for PCB assembly	22-Nov-21		0d	$0.00	0h