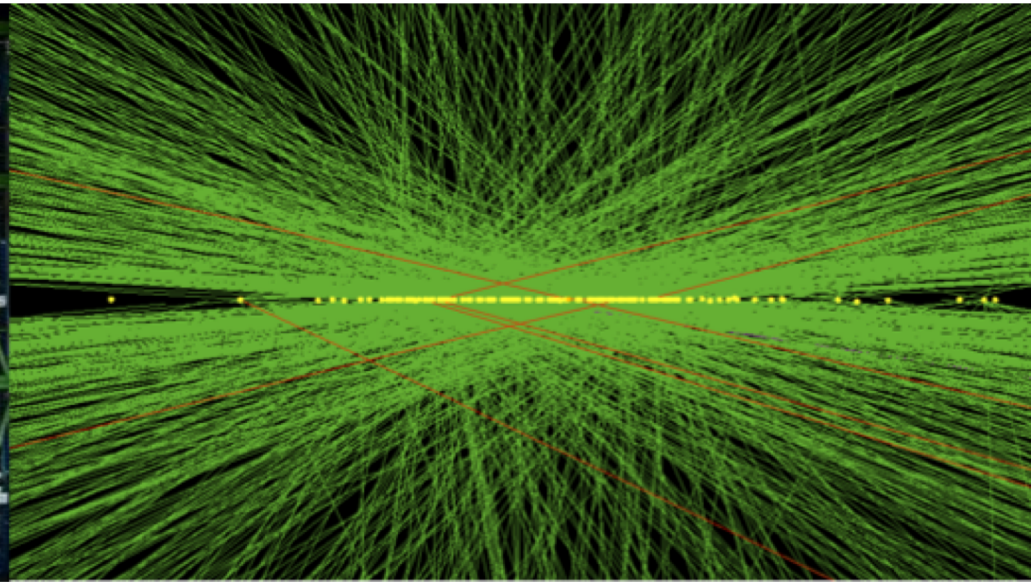
B0-6: In-depth: ETROC ASIC
402.8.4.2

Ted Liu
Fermilab

HL-LHC CMS CD-1 Review

23, October 2019

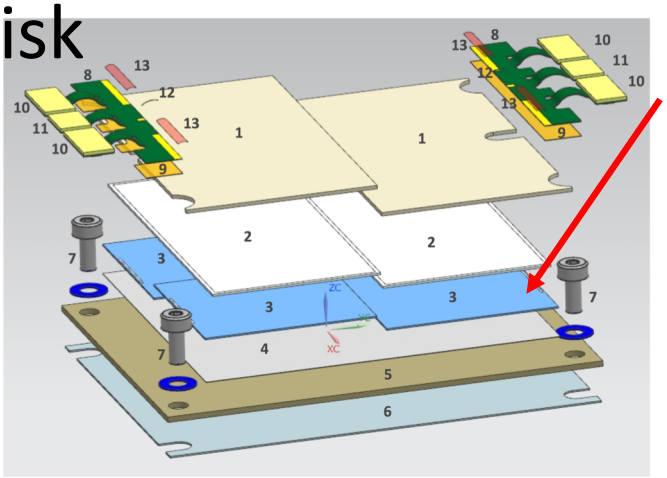


Brief Biographical sketch

- Ted Liu (Fermilab)
- Coordinator for front-end electronics in MTD/ETL
- L4 for ETL ASIC in US-MTD
- Relevant Expertise to ETL:
  - LBNC review committee member
    - DUNE cold electronics (with a few ASIC chips in 65nm and 130nm)
  - Tracking Trigger R&D for HL-LHC (AM based)
    - 3DIC Vertically Integrated Pattern Recognition AM (VIPRAM) chip R&D
    - ATCA based system demonstration for HL-LHC tracking trigger
  - God-parent committee for Pico-second timing project (U Chicago)
  - Review Committee chair for Fermilab Electrical Engineering
  - CDF Trigger Coordination (+ muon/calorimeter/SVT/L2 trigger upgrades)
  - Babar Drift Chamber Tracking Trigger project coordination
  - Belle Aerogel Cherenkov Particle Identification Detector
    - Preamp/front-end + SCA-based-TDC ASIC waveform readout system design
  - CLEO Time-Of-Flight calibration for Particle Identification
  - Silicon Drift Detector R&D with SCA readout (Switch Capacitor Array)

ETL ASIC (402.8.4.2) Outline

- Introduction
  - Methodology to approach the design
  - Overview of ETL ASIC (ETROC)
  - The development plan & strategy
- ***Development and technical progress***
  - ETROC0 (single pixel) design and prototype
  - ETROC1 (4x4 pixel) design and submission
  - ETROC2&3 (full functionality) design and status
- Schedule, cost, resource and risk
- Summary



Our Methodology to approach the design

- A three pronged approach is taken to consider the ASIC and the sensor together from the start to ***optimize the front-end design for LGAD behavior at end of operations*** (low signal size etc)
  1. Use the ***LGAD beam test data*** as input , to study different timing algorithms
     - *Leading Edge with Time Over Threshold (TOA/TOT)*
     - Constant Fraction Discrimination (CFD)
  2. Use ***LGAD simulation as input***, ***simulating different front-end design concepts***
  3. Simulate and optimize the expected performance of the actual ASIC implementation ***with post-layout simulation, using LGAD simulation as input***

The three-pronged design approach has been highly effective, making rapid progress since June 2018

ETROC: ETL Read-Out Chip

ETROC is bump-bonded to LGAD sensor, to handle a 16 × 16 pixel matrix, each 1.3 mm × 1.3 mm. chip size ~21mm x 21mm.

ASIC contribution to time resolution < ~40ps

Targeted signal charge (1MIP): ~ 6fC

TDC range: ~5ns TOA and ~10ns TOT

L1 buffer latency: 12.5 us

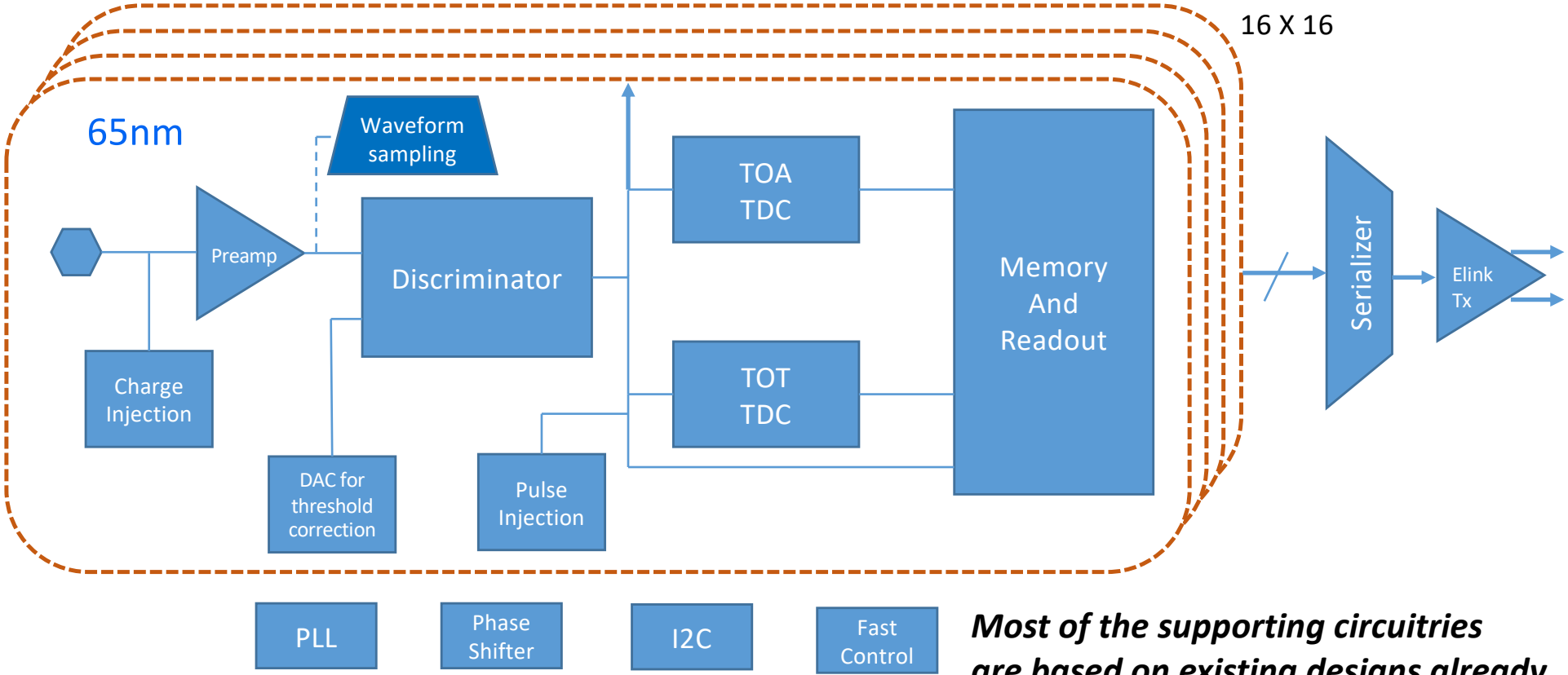
with power consumption < 1W/chip

Main challenging design work:

Preamp + discriminator

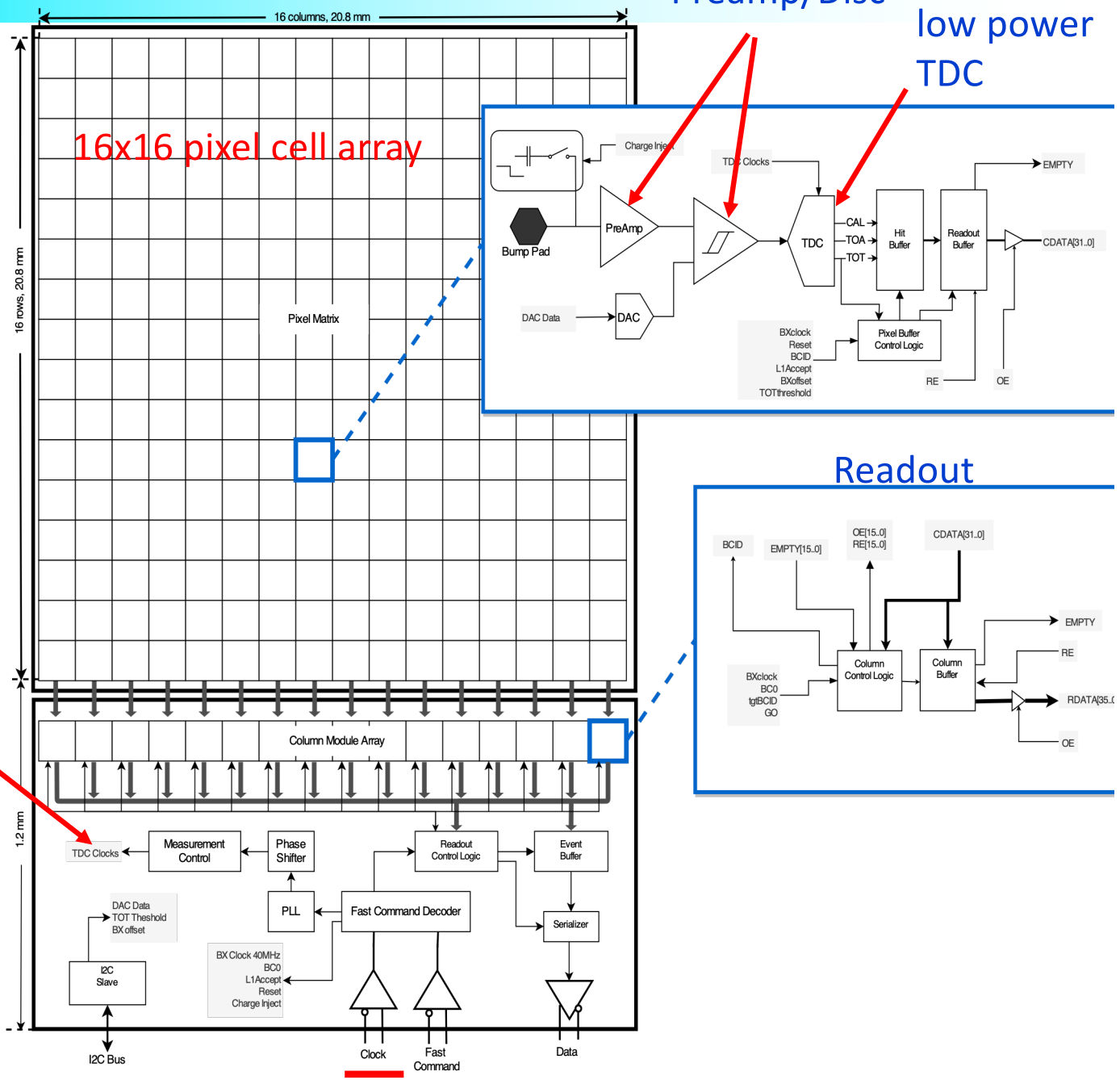
TDC

Clock distribution



Most of the supporting circuitries are based on existing designs already available

ETROC Overview (see CDR)



clock distribution all the way into each pixel

ETROC Development: *divide & conquer*

ETROC0: 1x1 pixel channel with preamp + discriminator (submitted Dec 2018)

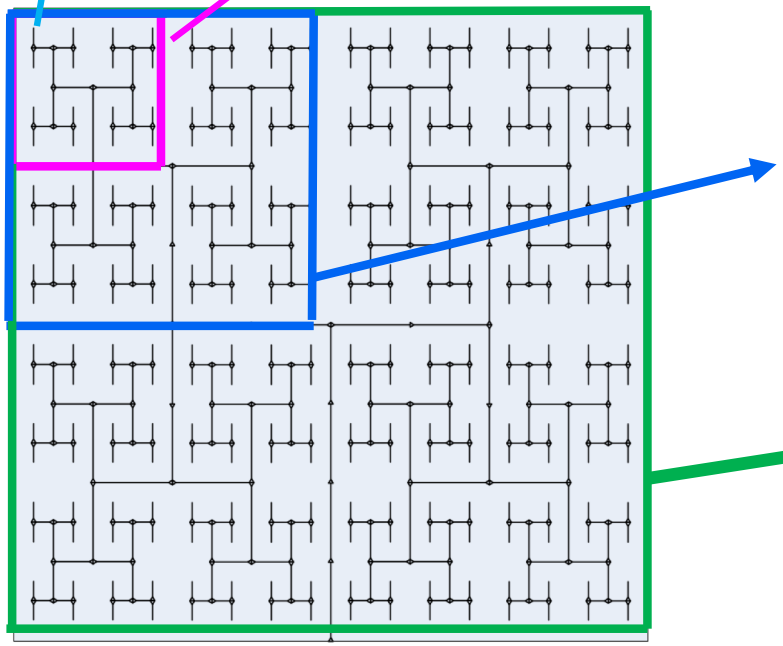
Goal: core front-end analog performance

the first prototype chip works well and agrees with simulation

ETROC1: 4x4 clock tree, preamp + discriminator + TDC (submitted Aug 2019)

Goal: full chain front-end with TDC, 4x4 clock tree

This is the first full chain precision timing prototype



16 x 16 clock H-Tree

ETROC2: 8x8, *full functionality*, and ¼ clock tree (Q1 2021)

Goal: supporting circuitries, 8x8 clock tree

PLL, phase shifter, fast/slow control, I/O, L1 buffer…

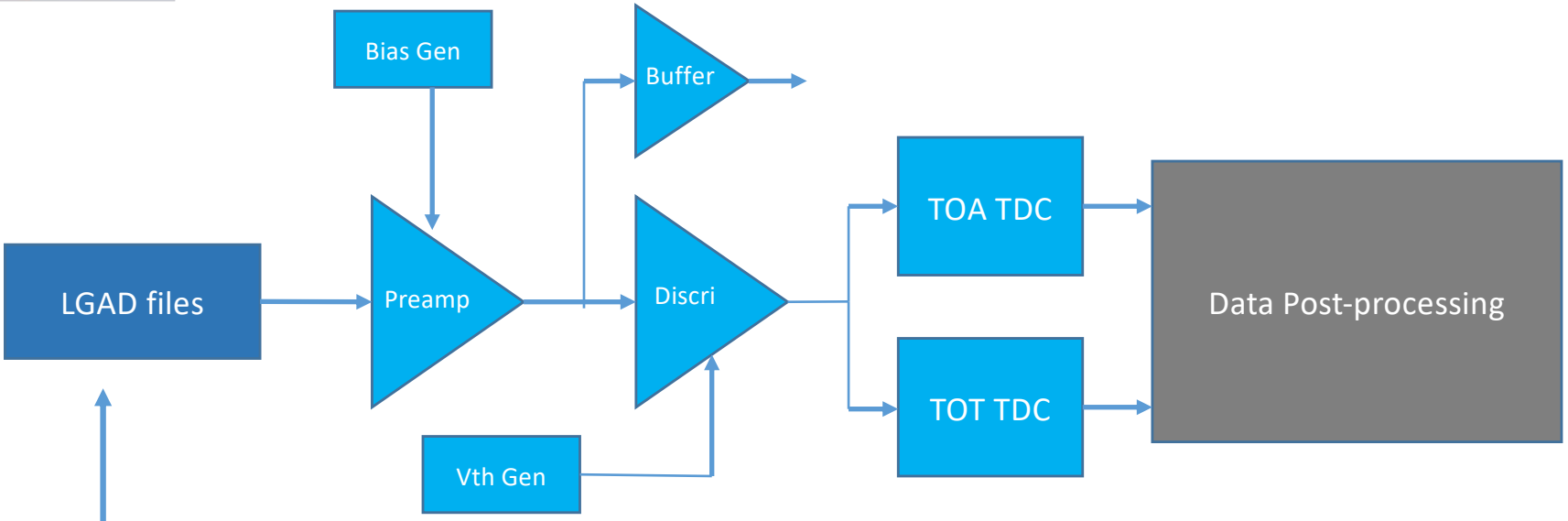
ETROC3: 16x16 (full size): (Q1 2022)

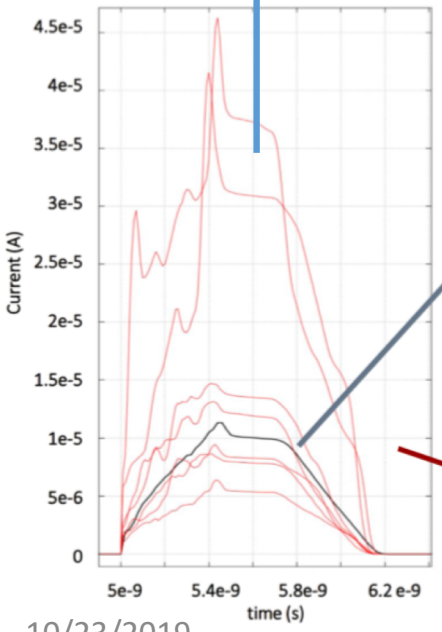
Goal: full size with full clock tree

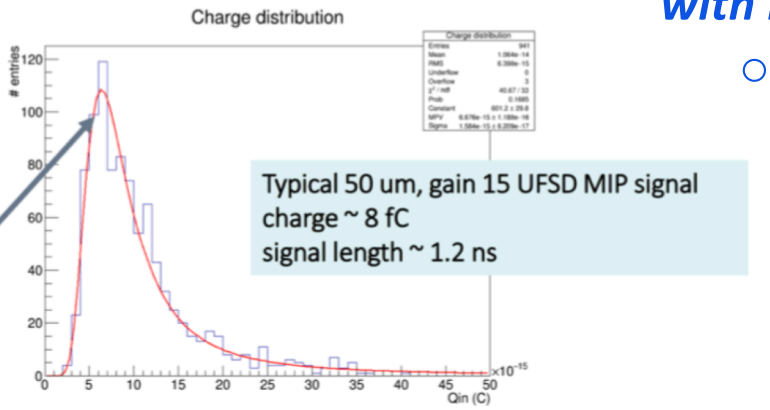
Production Q4 2022

Bottom-Up & Top-Down approach in parallel

How we approach the front-end design







Typical 50 um, gain 15 UFSD MIP signal
charge ~ 8 fC
signal length ~ 1.2 ns

Input to ASIC simulation

- ***With three cases: Pre-irrad, 5E14, 1E15 with realistic sensor bias voltage***
  - ***Preamp optimize for low signal size***
    - ***configurable/flexible design***

to allow performance optimization

A good flexible design is a balance between performance and power.

The design is optimized with LGAD gain at ~10

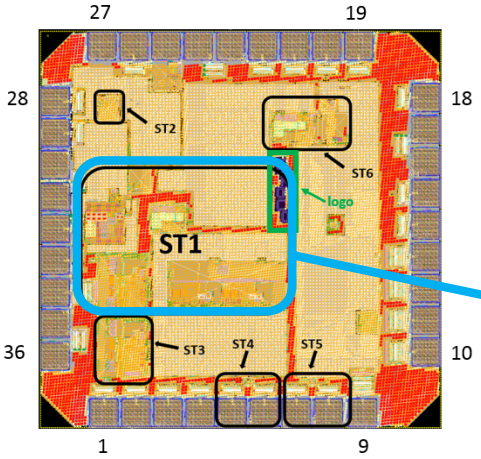
ETROC0: the First Prototype Chip

Submitted Dec 2018

Goal: core front-end analog performance

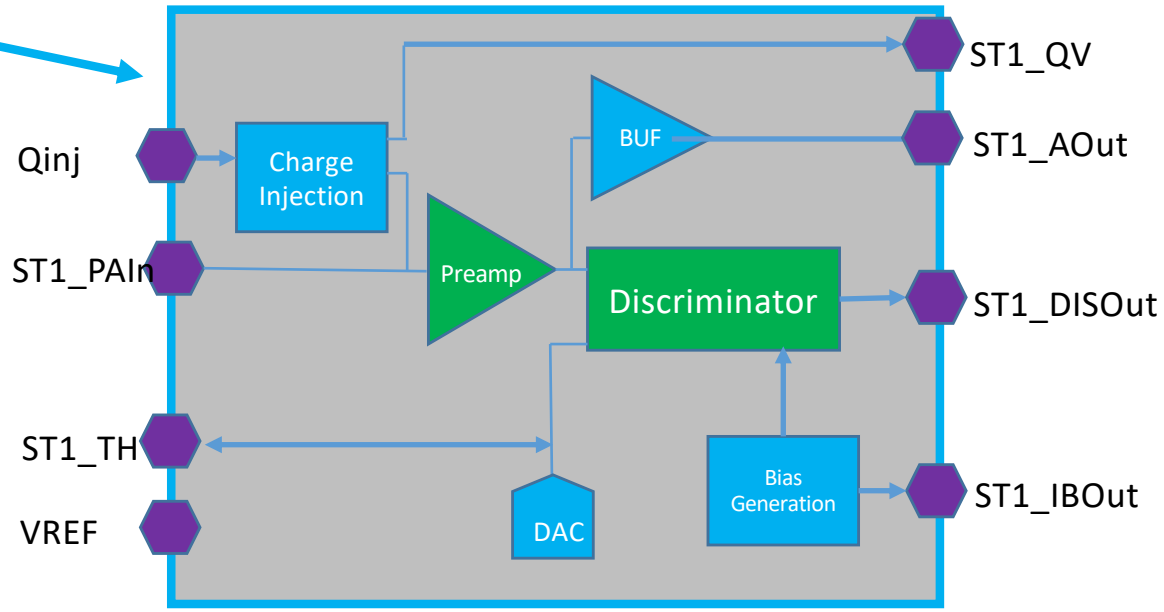
Studying performance with charge injection, then test with LGAD

ETROC0 chip

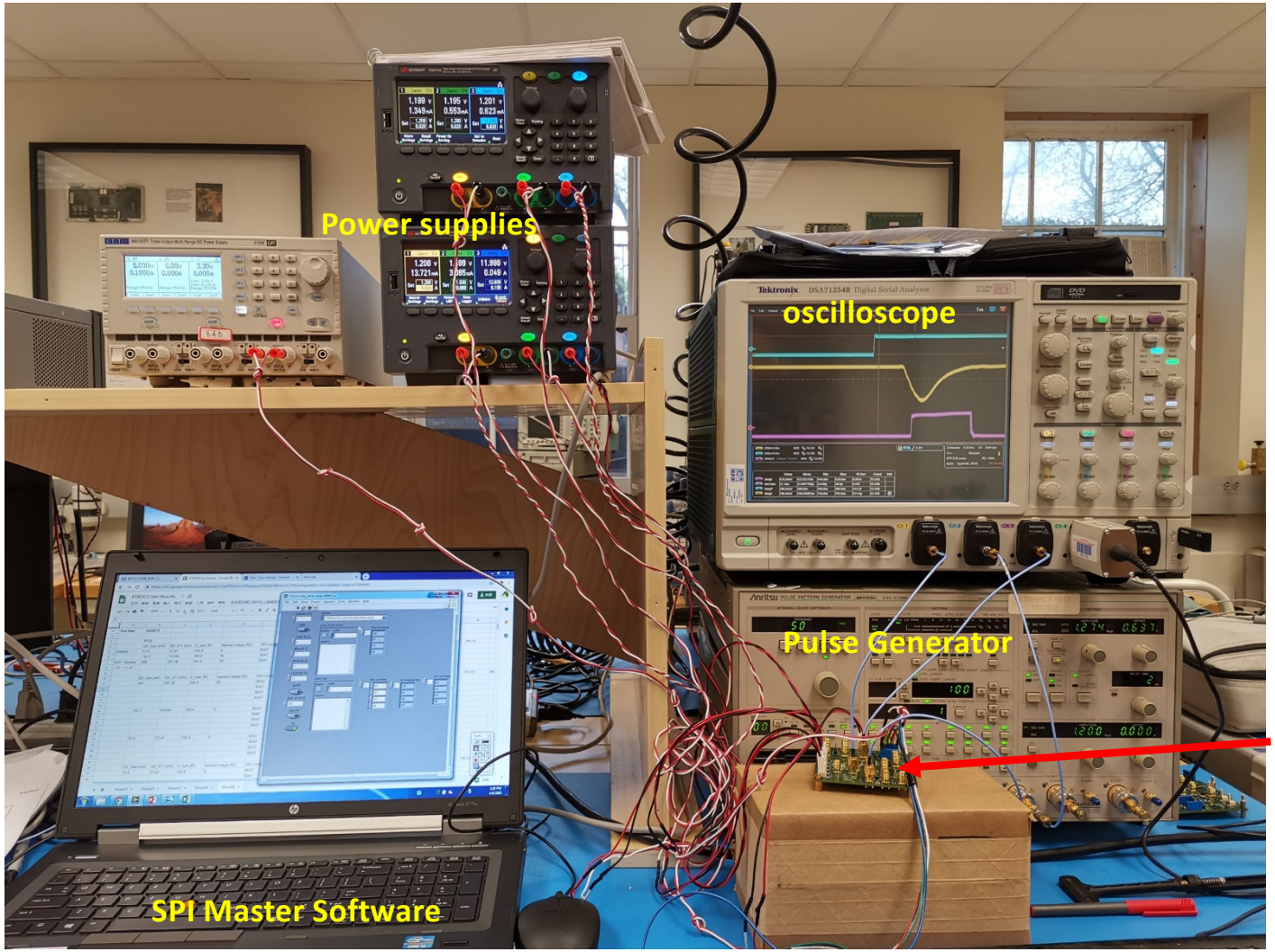


All individual blocks can be tested separately
Power consumption can be measured for each section separately

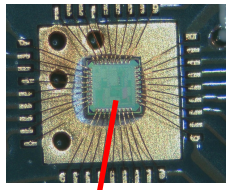
Test structure ST1: the full chain

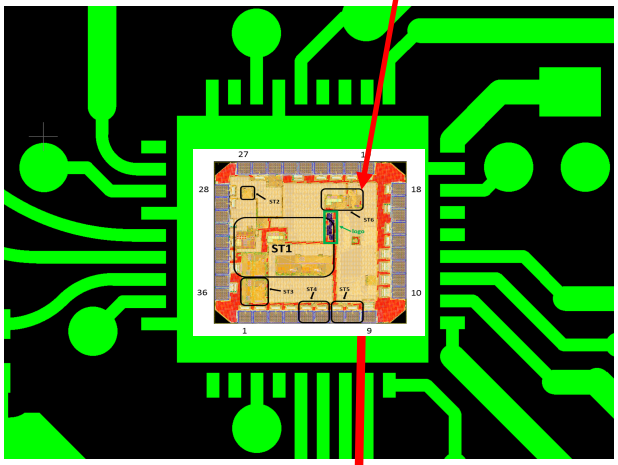


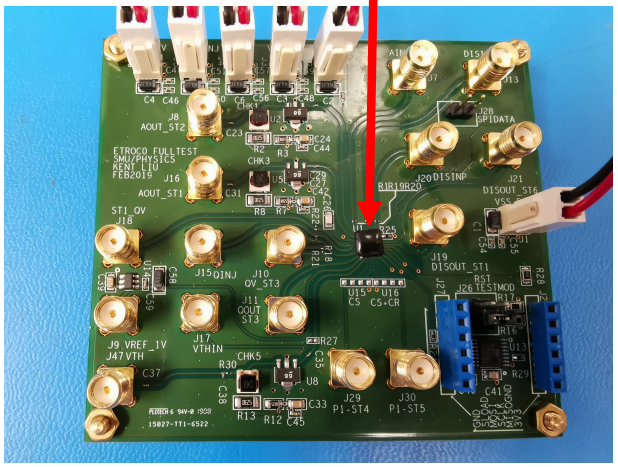
Performance study with charge injection



ETROC0



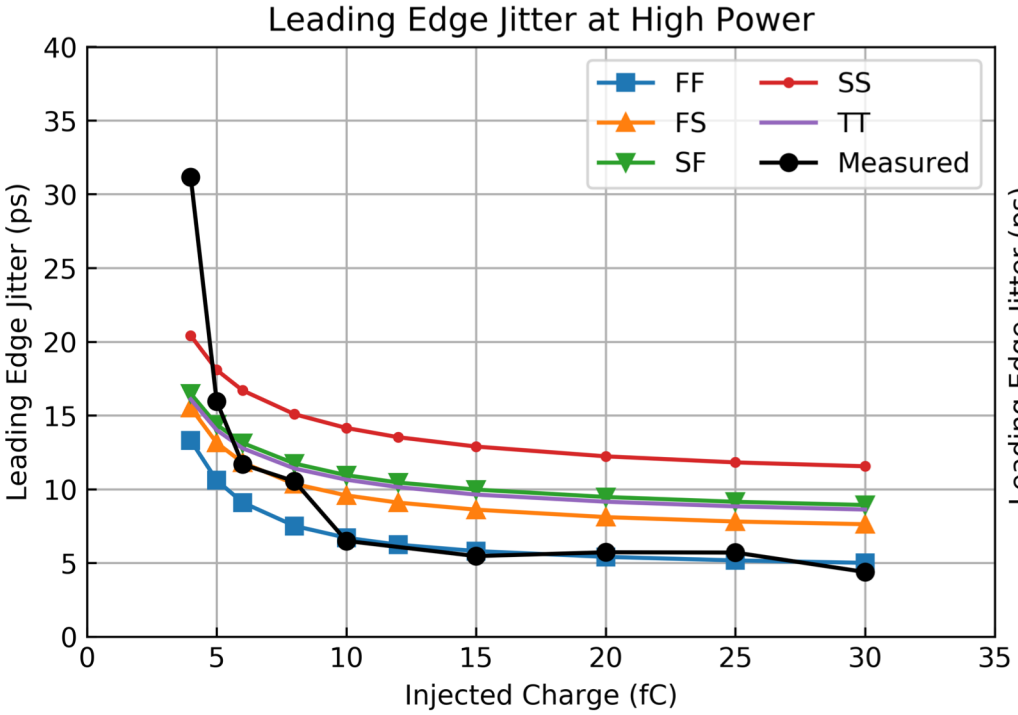


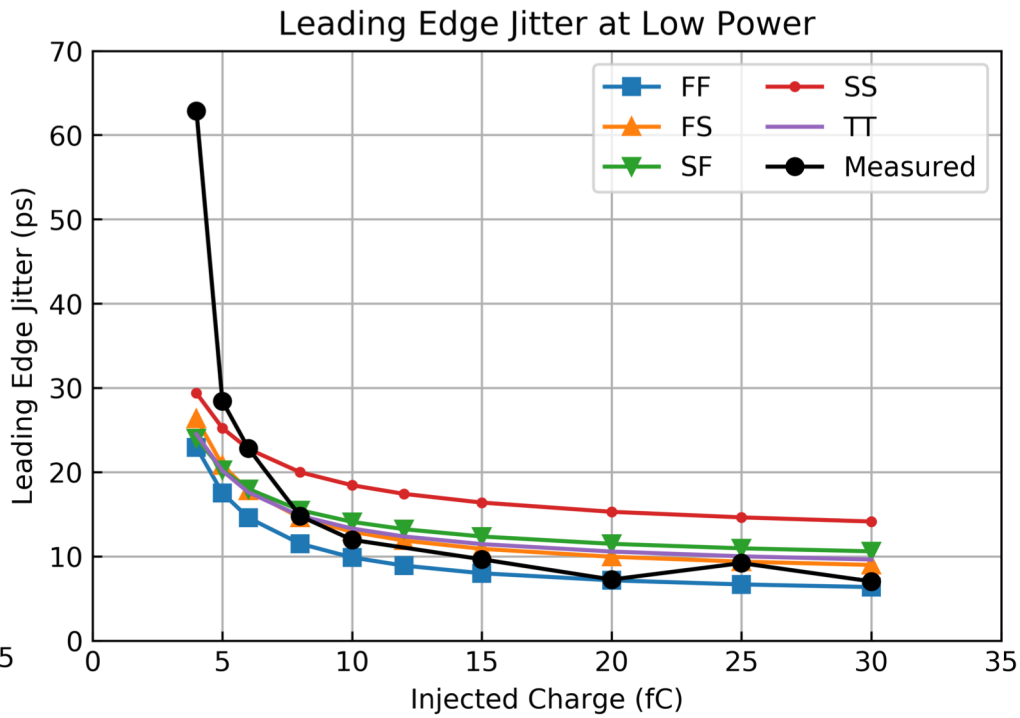


All functional testing results have been reproduced /confirmed at both SMU and FNAL teststands

ETROC0 jitter: measured vs simulation

ETROC0 post-layout simulation vs
testing results using 25ps risetime external pulse injection



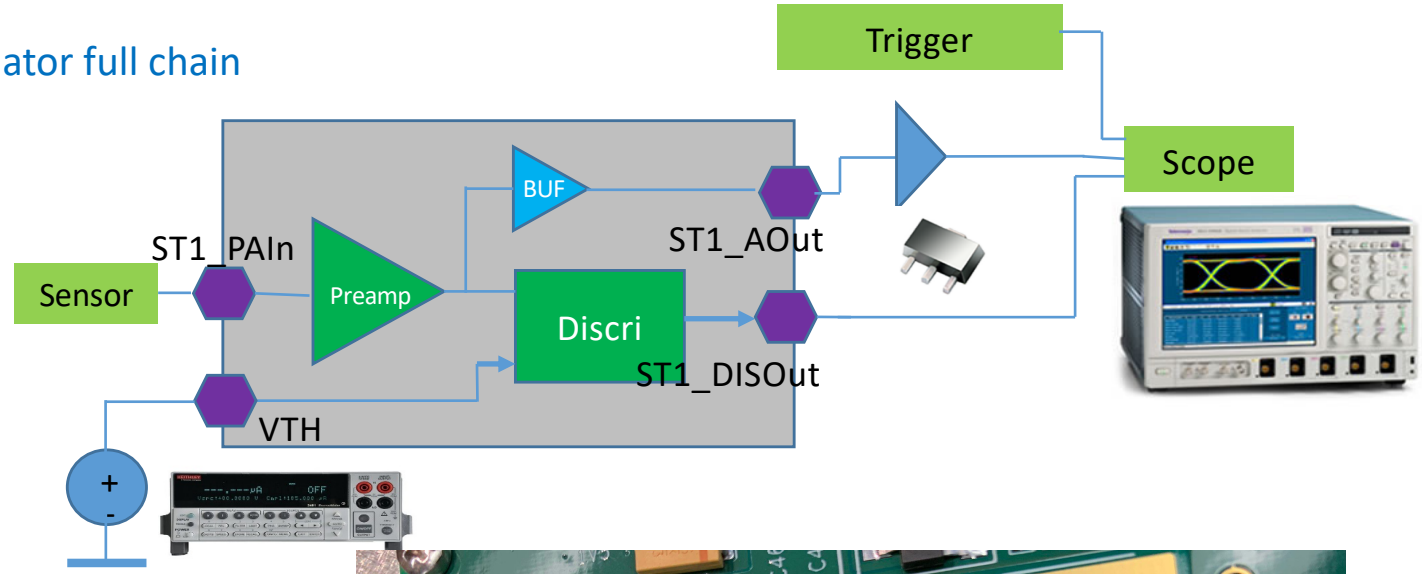


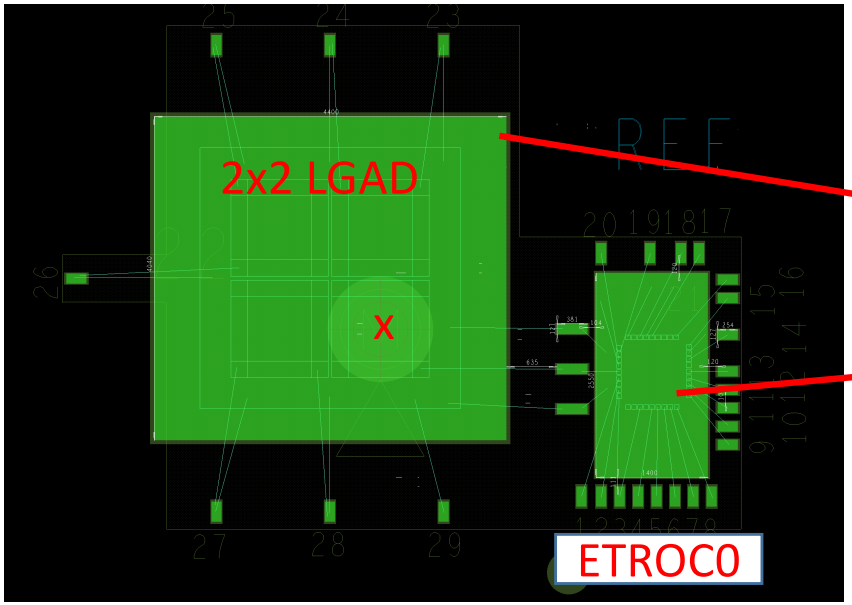
Jitter measurements agree with chip post-layout simulation

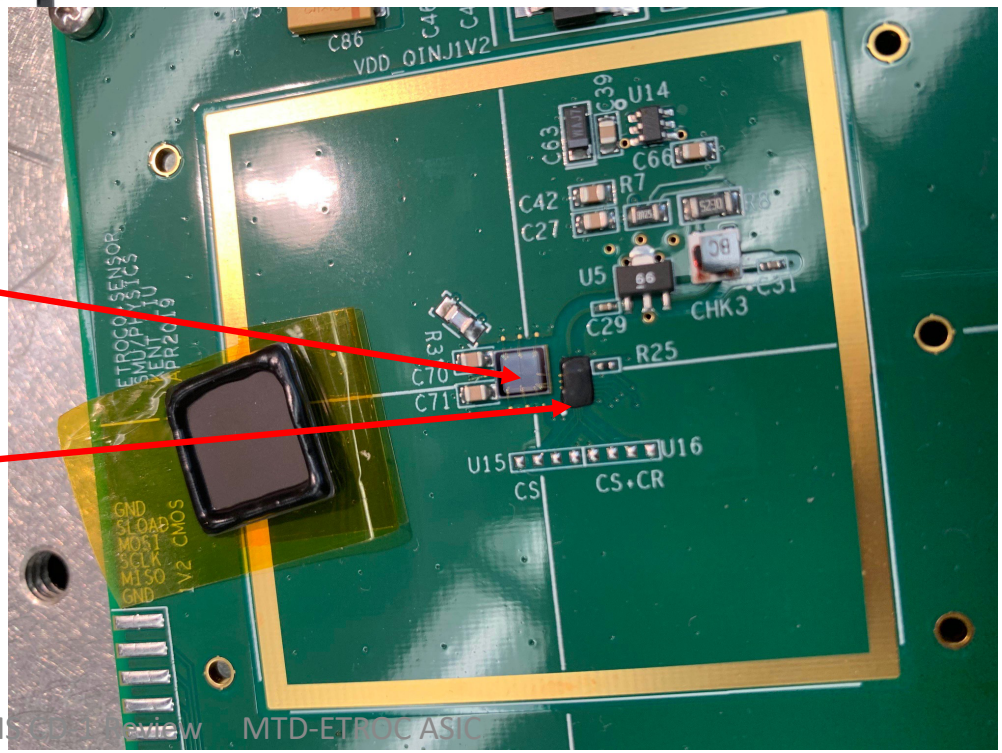
Power consumption for preamp and discriminator all match with simulation

Testing ETROC0 with LGAD

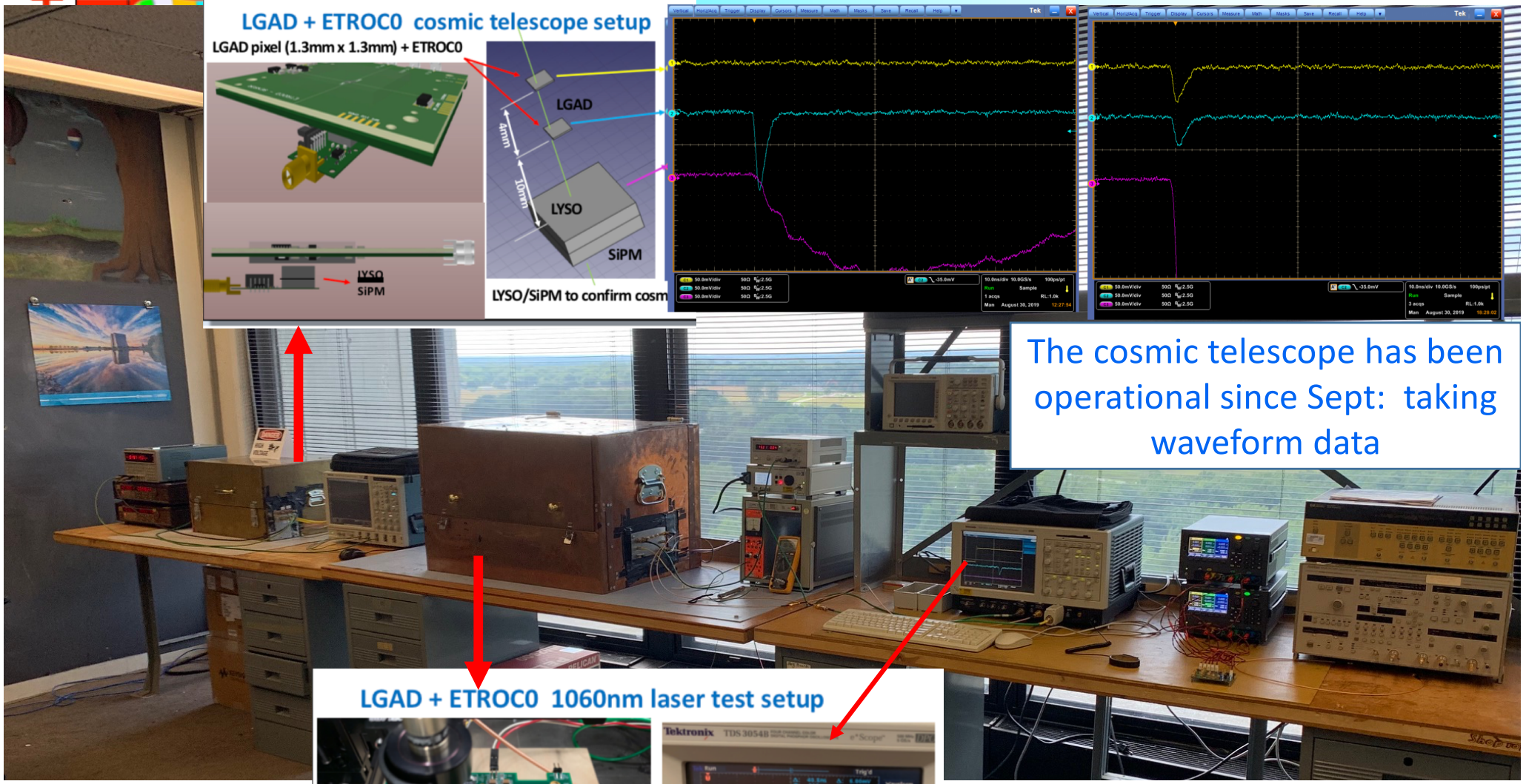
- New Test board design:
  - LGAD + preamp + discriminator full chain







LGAD+ETROC0 Test Stands at FNAL



The cosmic telescope has been operational since Sept: taking waveform data

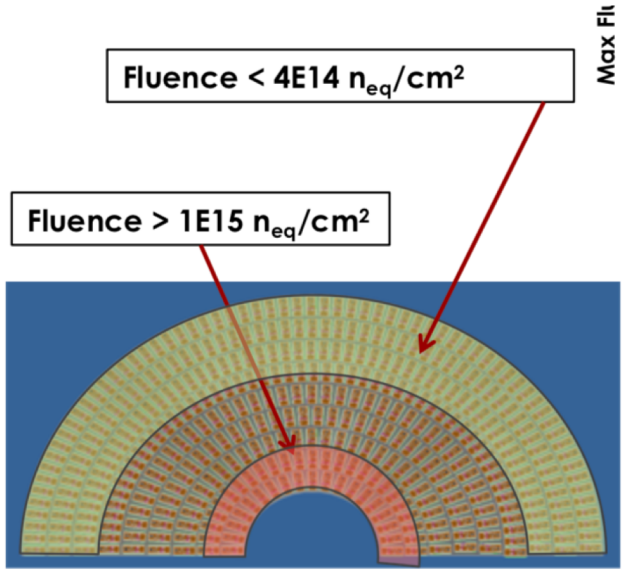
preparing for the upcoming beam test at FNAL (starting Dec 2019)

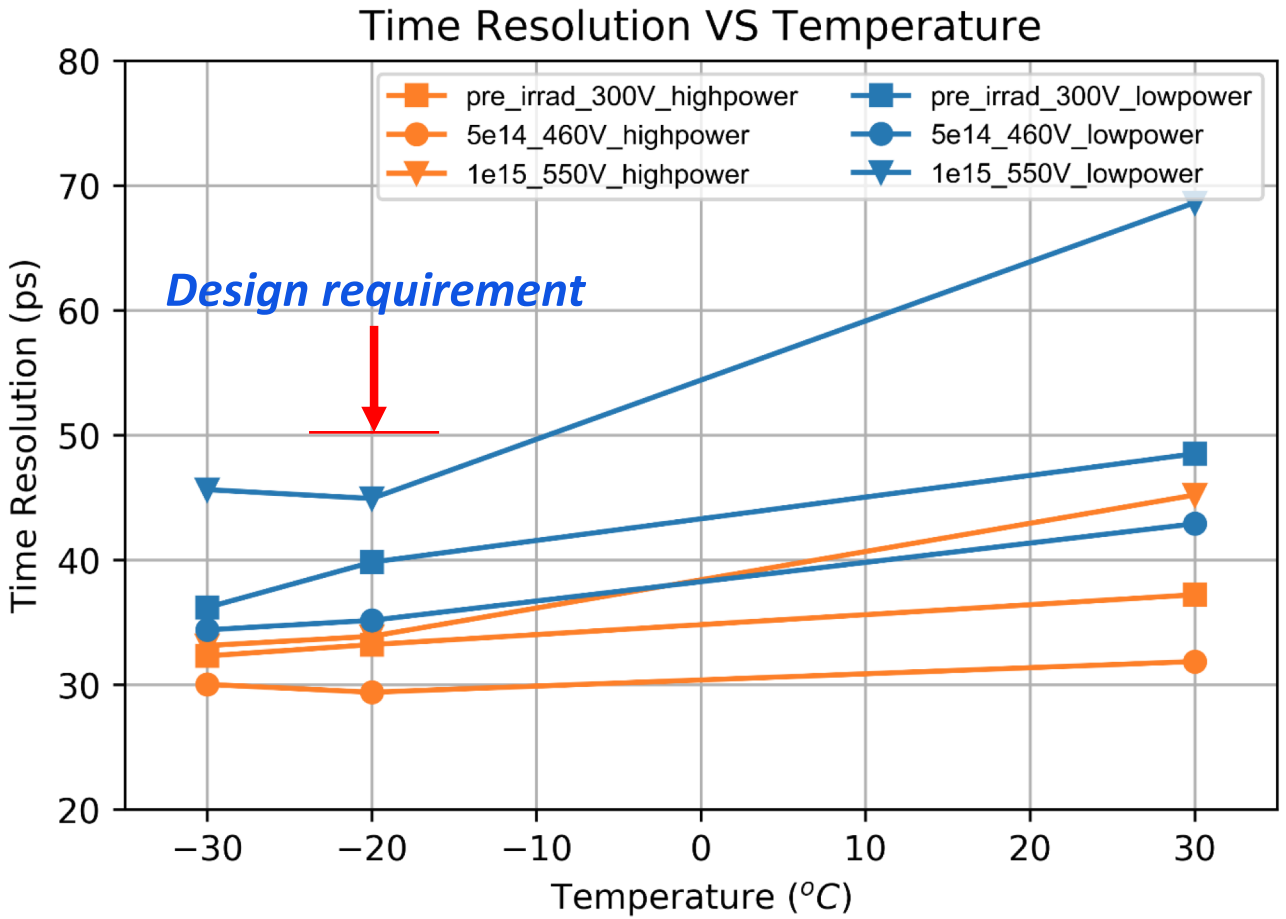
Full-chain post layout simulation: LGAD + Preamp + Disc

- Three irradiation levels for LGAD Sensor simulation: pre-irrad, 5e14, 1e15
  - Three representative cases of early, mid, late operations
- Two preamp bias current settings studied (low to high)
  - 0.35mA, 0.7mA, 1.05mA, 1.4mA

with preamp @ low power:
~ 35 ps @5e14

with preamp @ high power:
~ 35ps @1e15

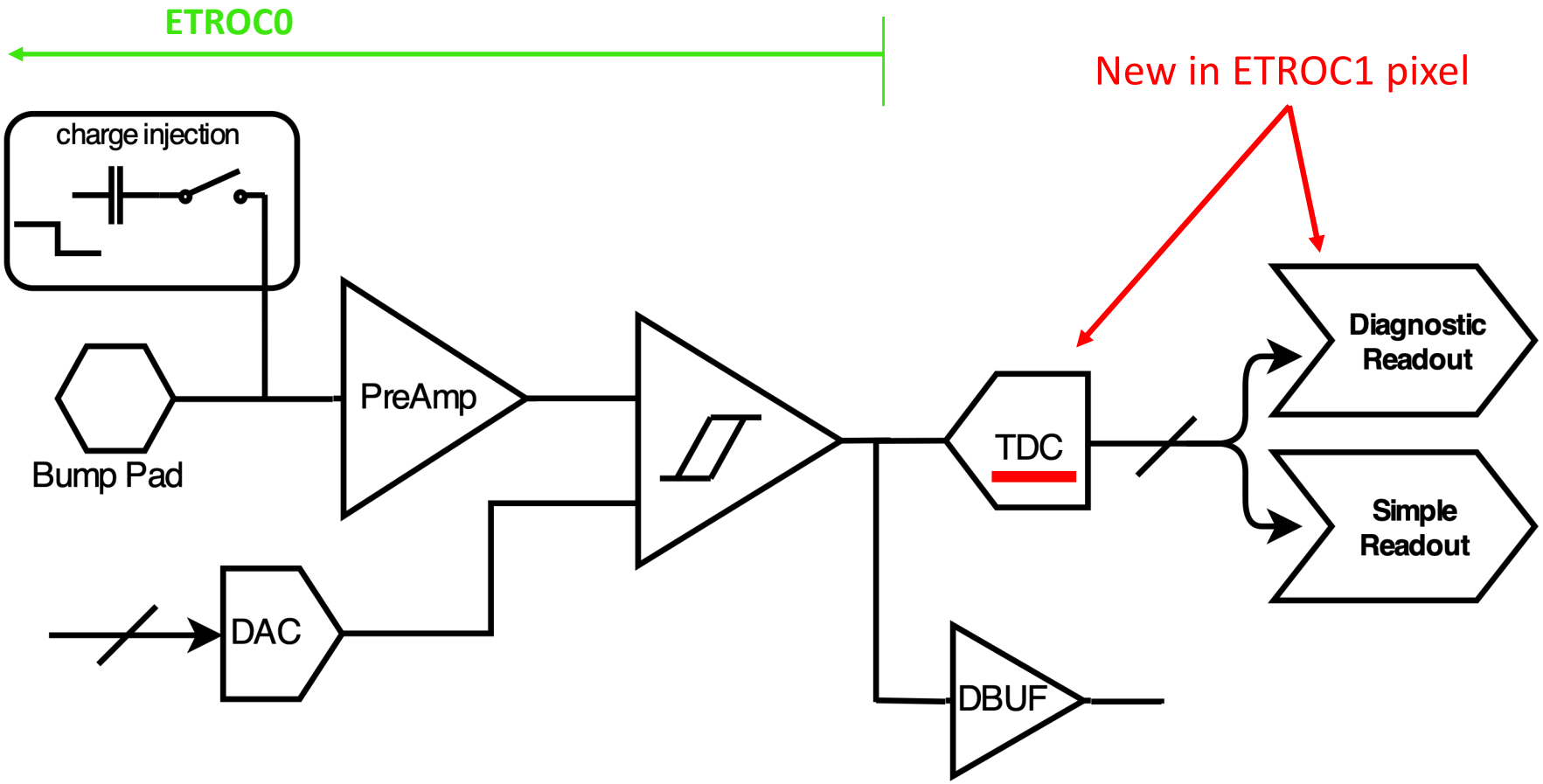




Post layout simulation results, to be validated in the upcoming beam test at FNAL (starting Dec 2019)

ETROC1 pixel: uses ETROC0 front-end

ETROC0 performance is as expected, it is used directly in ETROC1

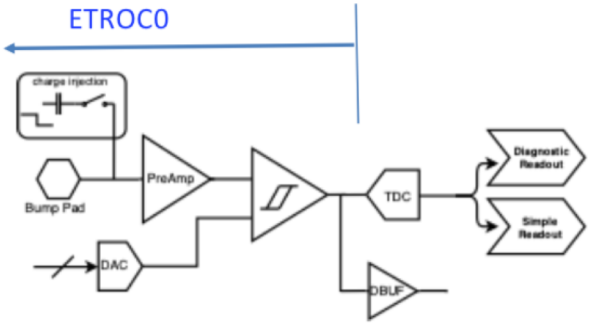


The TDC is brand new design (low power)
~ one year development effort

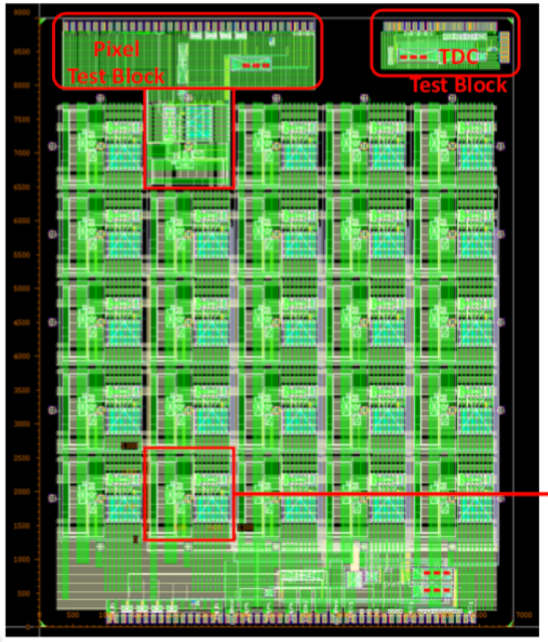
ETROC1 TDC Design

- TDC requirements
  - TOA bin size < ~30ps, TOT bin size < ~100ps
  - Lower power highly desirable
    - ***ETROC TDC design goal: < 0.2mW per pixel***
- ETROC TDC design optimized for low power
  - A simple delay line without the need for DLL's to control individual delay cells, with a cyclic structure to reduce the number of delay cells, to measure TOA & TOT at the same time
- ***In-situ delay cell self-calibration technique***
  - For each hit, will use two consecutive rising clock edges to record two time stamps, with a time difference of the known 320 MHz clock period: 3.125ns
  - Crucial to reach the required precision using a tapped delay line with uncontrolled delay cells (thus lower power)

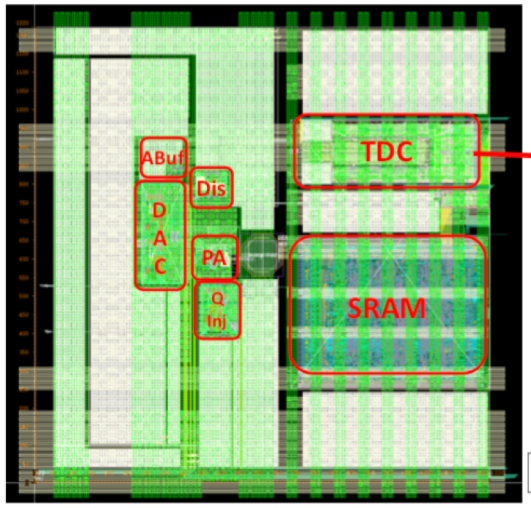
ETROC0



ETROC1 Top Layout

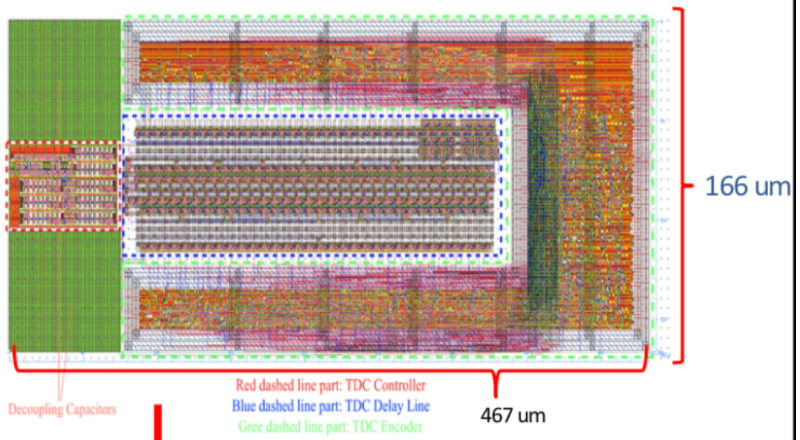


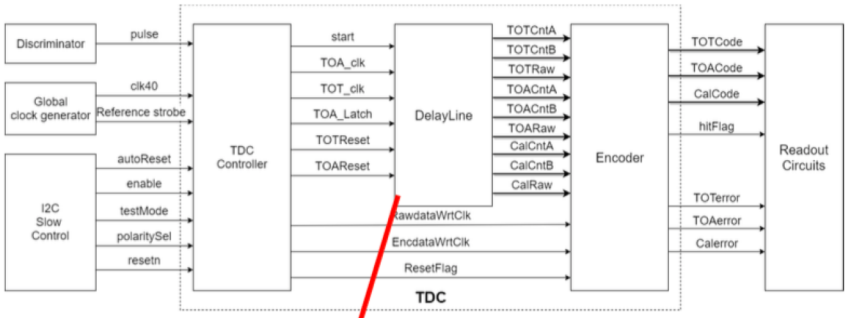
ETROC1 Single Pixel Layout



Extensive design verification has been done, mostly by EE students.

Low power TDC: <0.1mW





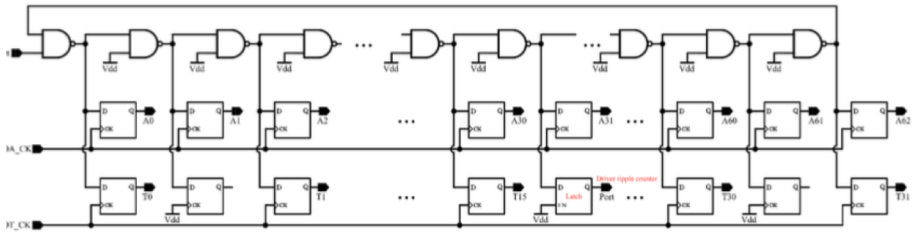
God-parent reviews in May and July 2019

ETROC1 submitted on time (Aug 28, 2019)

Expect chip delivery end of Nov 2019

More details in backup slides

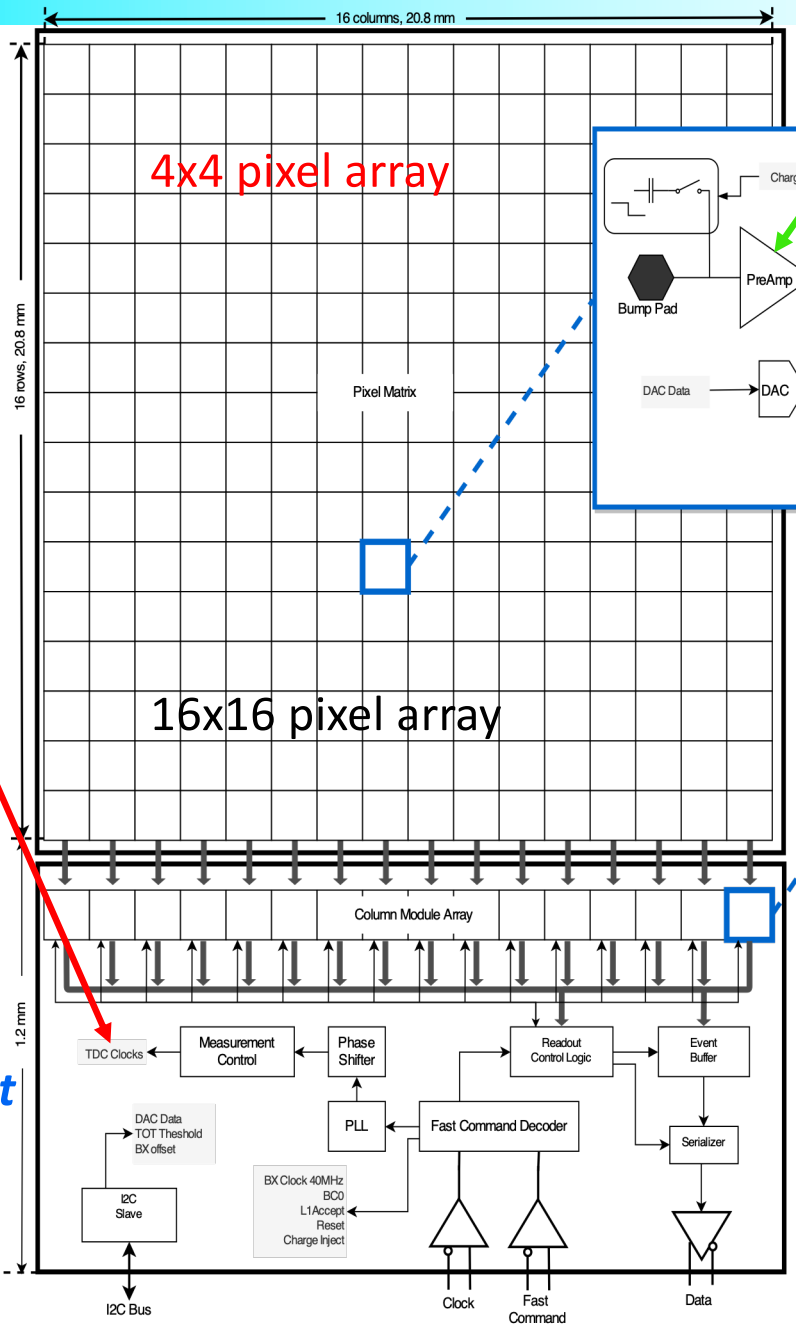
TDC core logic: gated ring oscillator

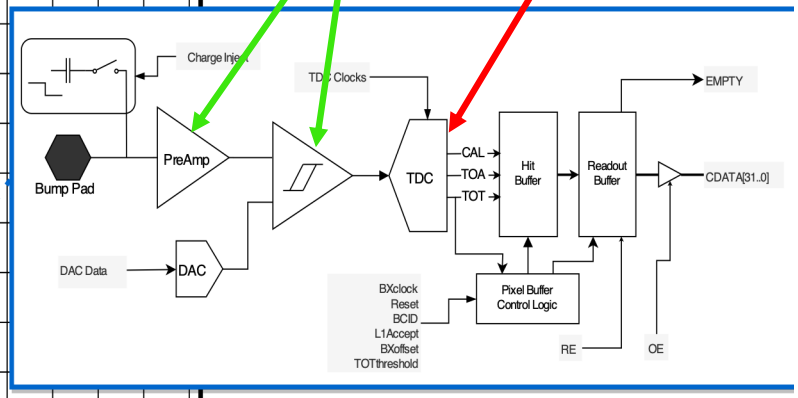


ETROC1 wrt ETROC

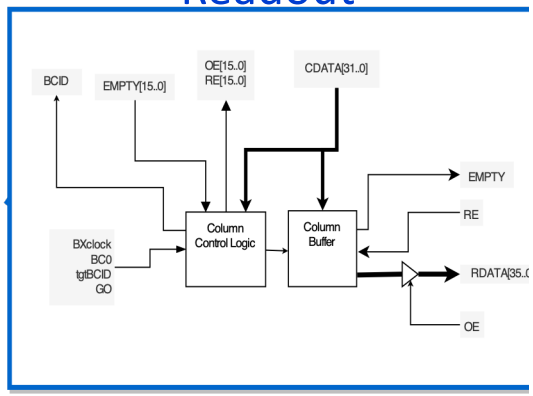
ETROC0
Preamp/Disc

low power
TDC





Readout



Simplified version of readout

clock distribution all the way into each pixel

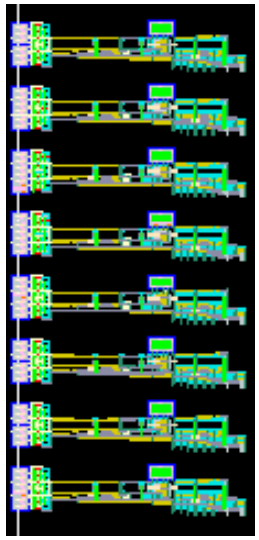
(4x4 clock distribution)

ALL critical components are implemented in ETROC1

The remaining components not in ETROC1 are supporting circuitries: full readout, PLL, Fast command decoding etc

ETROC2&3: already on going

- ETROC specification has been fully developed (CDR)
  - Most critical components implemented in ETROC0&1
- Full-chip clock distribution design study done
  - The textbook H-tree clock distribution works well
- Waveform sampling spec and design developed
  - For monitoring and calibration
  - Single channel ADC prototype received, works well
  - The core 2.56 GS/s waveform sampler at post-layout simulation stage
- The rest of supporting circuitries will be based on existing design blocks in 65nm from CERN



Area of
300um * 800um

People currently involved in ETROC (0&1)

ETROC presented at TWEPP 2019 (Sept 2-6, Spain)

The ETROC Project: Precision Timing ASIC Development for LGAD-based CMS Endcap Timing Layer (ETL) Upgrade

Tiehui Liu, Grzegorz Deptuch, Sergey Los, Sandeep Miryala, Jamieson Olsen, Luciano Ristori, Quan Sun, Jinyuan Wu
Fermi National Accelerator Laboratory, Batavia Illinois, USA
Datao Gong, Kent Liu, Tiankuan Liu, Hanhan Sun, Jingbo Ye, Li Zhang, Wei Zhang
SMU Physics, Dallas Texas, USA
Liang Fang, Tao Fu, Ping Gui, Xianshan Wen, Chi Zhang
SMU EE, Dallas Texas, USA
Siddhartha Joshi, Seda Ogrenci-Memik
Northwestern University, Evanston Illinois, USA
Sunil Dogra, Chang-Seong Moon, Jongho Lee
Kyungpook National University, Daegu, South Korea

POSTER-19-119-E

The Godparents Committee has been formed since July 2018

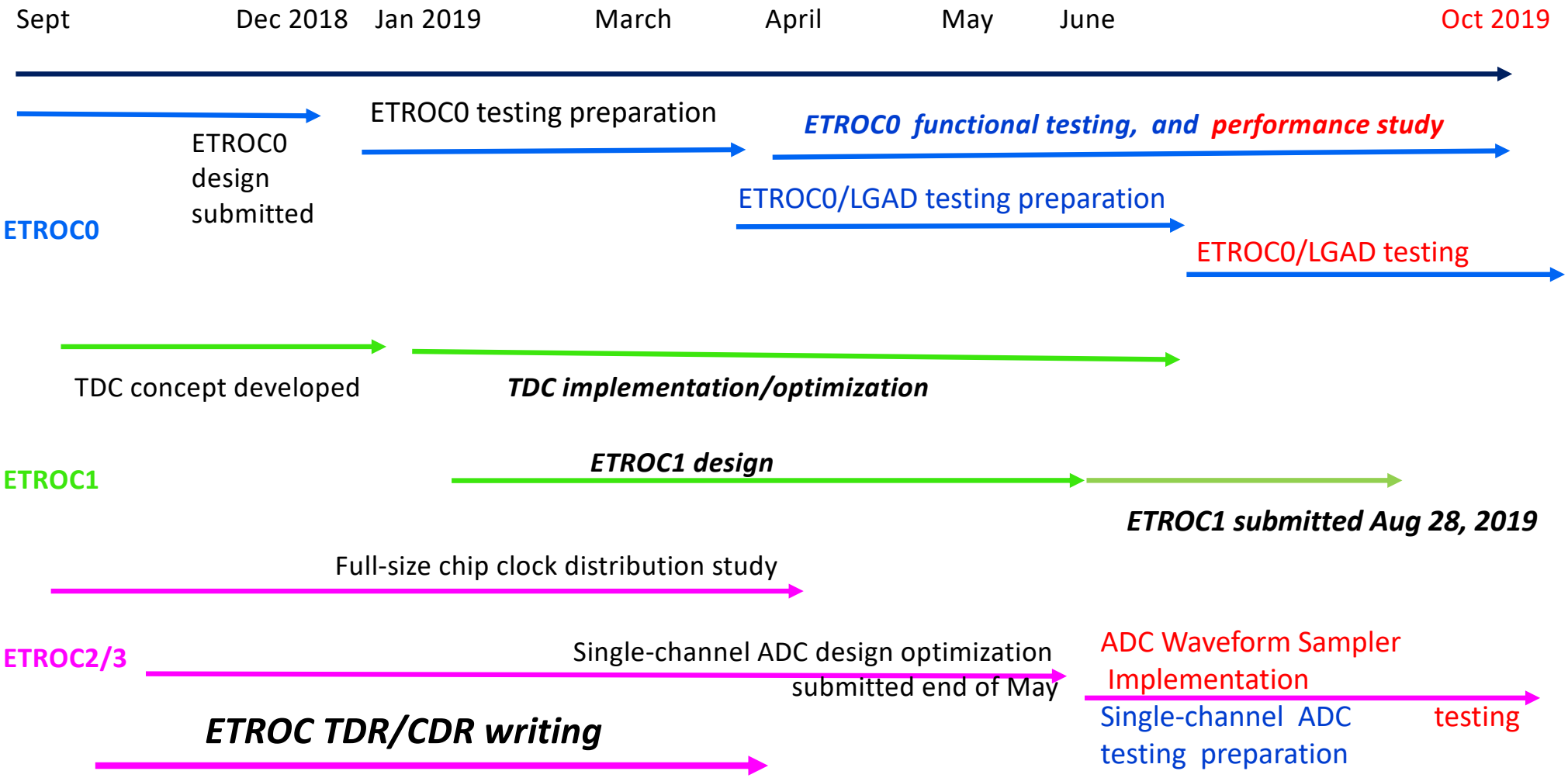
GP reviews so far: Sept 2018, Nov 2018, May 2019, July 2019, been highly valuable

ETL Timing ASIC Godparents Committee

David Christian[1], Gary Drake[1], Carl Grace[2], Christine Hu[3], Ron Lipton[1], Eric Oberla[4], Fukun Tang[4], Gary Varner[5]

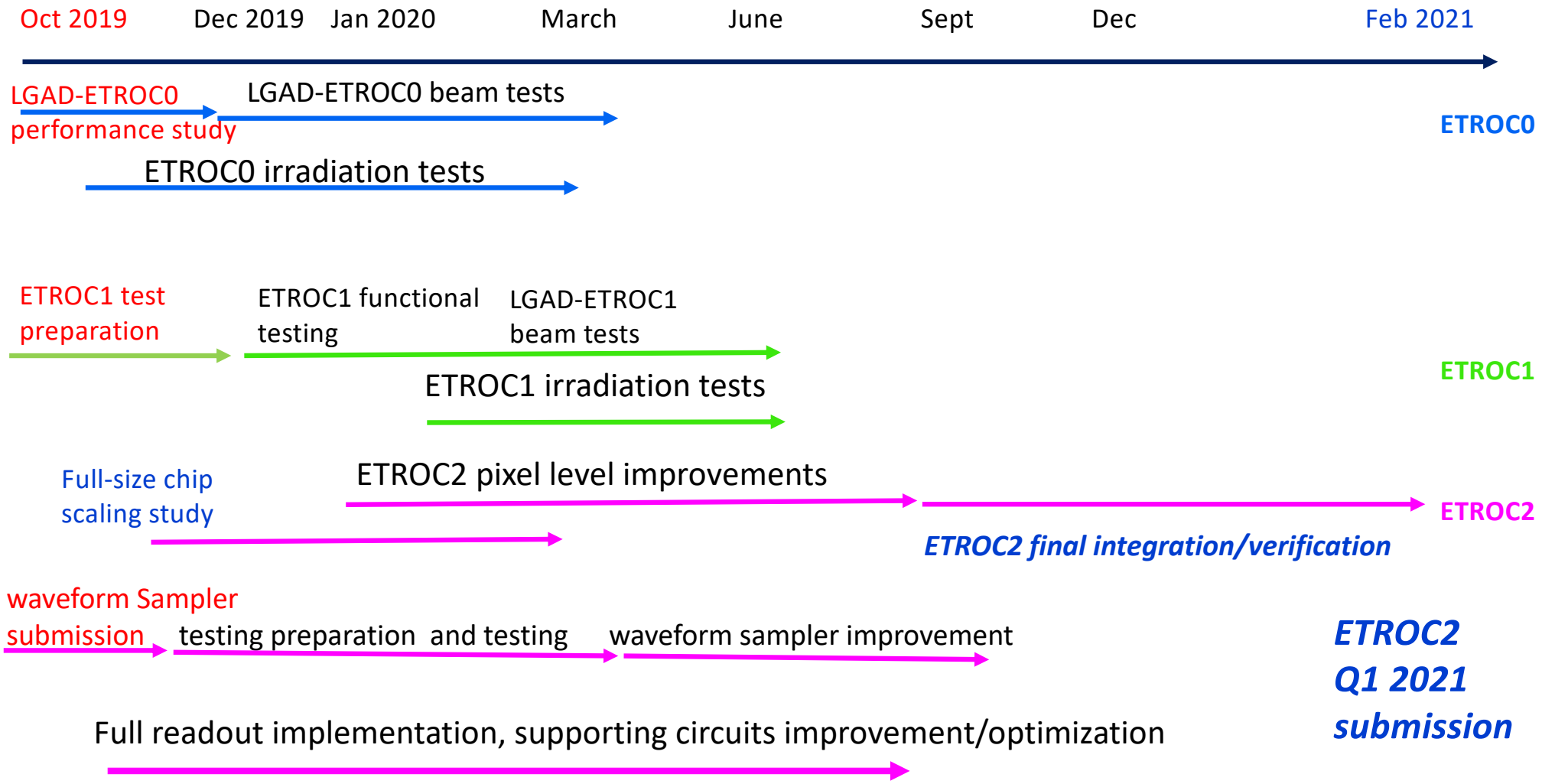
1. FNAL, 2. LBNL, 3. IN2P3, 4. University of Chicago, 5. University of Hawaii

ETROC activities over the past year (current activities)



Past year: making rapid progress with a strong team, proceeding just as we planned

Towards ETROC2 (current activities)



From ETROC2 to ETROC3

Feb 2021 March — June — Sept — Dec — March 2022

ETROC2

testing preparation → functional and beam tests → **ETROC2**

ETROC2 irradiation tests →

ETROC3 pixel level improvements →

supporting block improvements

Full-size chip initial Implementation & verification → **ETROC3**

ETROC3 optimization/verifications

Main task: design verification & verification

ETROC3 March 2022 submission

Overall expected ETROC performance

LGAD+ preamp/discriminator + TDC bin	35 ps
Time-walk correction residual	< 10 ps
Internal clock distribution	< 10 ps
System clock distribution	< 15 ps
Per hit total time resolution	41 ps
Per track (2 hits) total time resolution	29 ps

With safety margin:
design specification is
~ 35ps per track,
~ 50ps per track at end of life

Circuit component	Power per channel [mW]	Power per ASIC [mW]
Preamplifier (low-setting)	0.67	171.5
Preamplifier (high-setting)	1.25	320
Discriminator	0.71	181.8
TDC	0.2	51.2
SRAM	0.35	89.6
Supporting circuitry	0.2	51.2
Global circuitry		200
Total (low-setting)	2.13	745
Total (high-setting)	2.71	894

With safety margin:
design specification is
< ~ 1W per chip

Costs for ETROC2&3

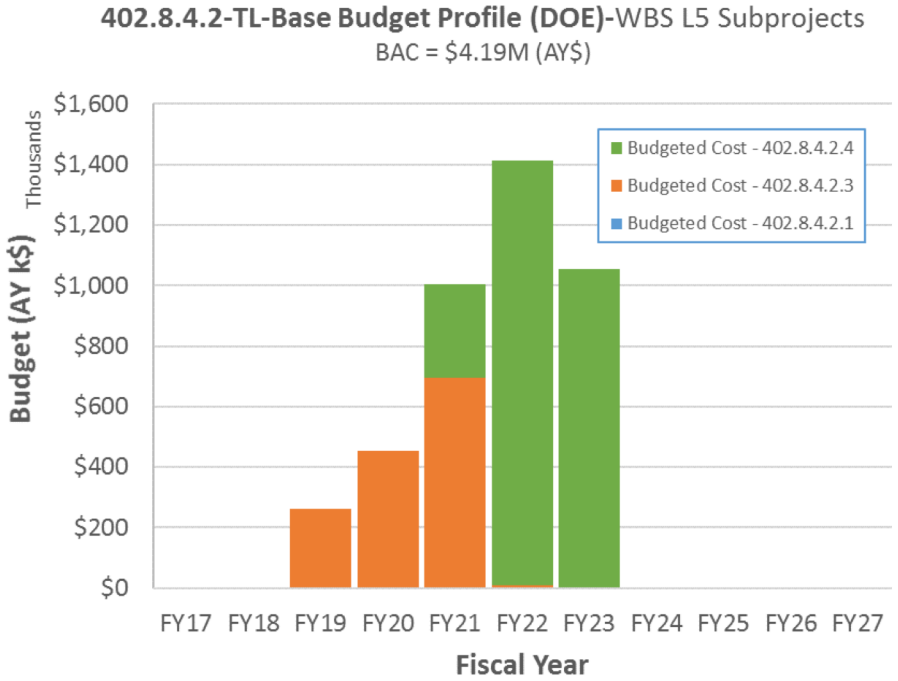
Funds to cover ETROC2 and ETROC3 development

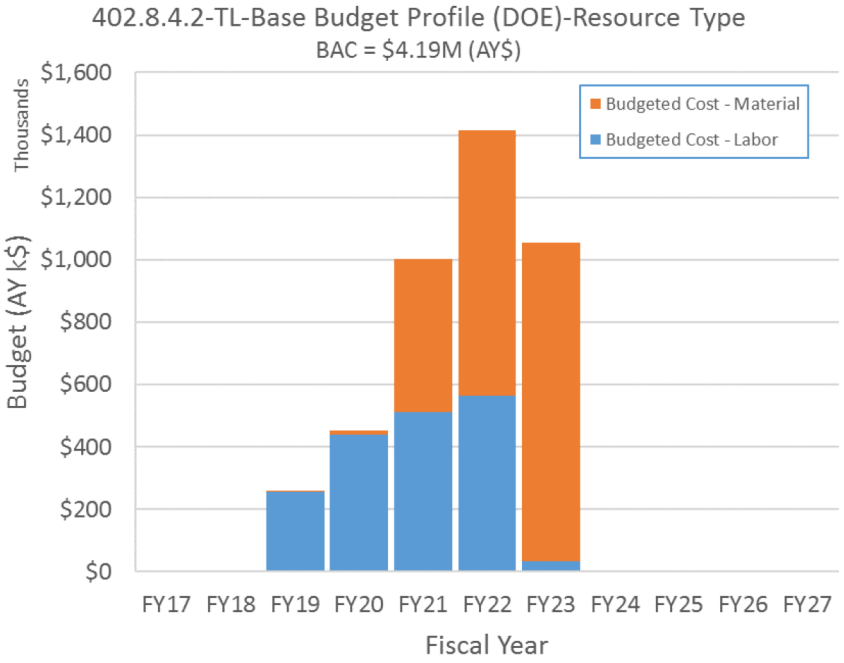
Labor Resource Type	Hours	FTE
ASIC Design and Testing Engineers	8702	4.93
SMU EE Graduate Students	13250	7.49

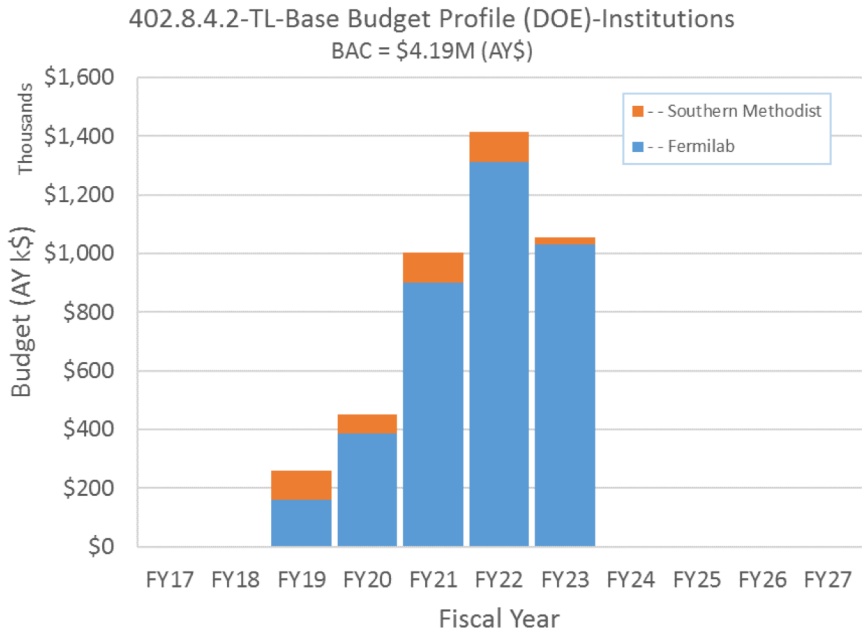
M&S Item	Base Cost (k$)
ETROC2 (8x8)	401
ETROC3 (Mask set)	780
ETROC3 Production	886

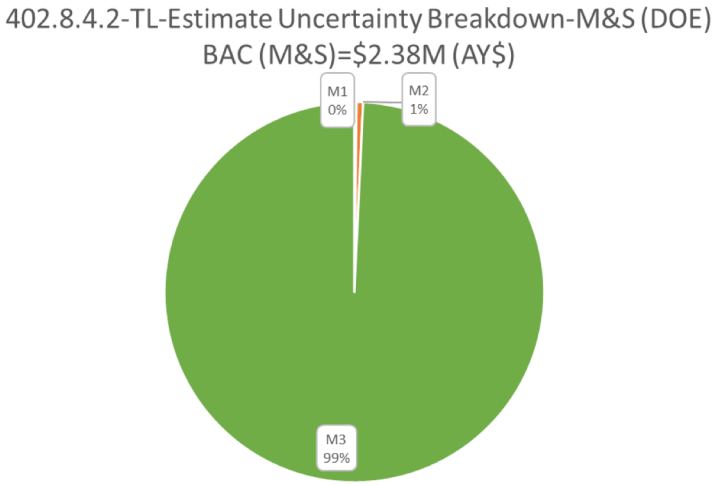
+ funding to cover costs for irradiation, testing hardware, travel

Base Budget Profile









ETL Risks (related to ETL ASIC)

WBS / Ops Lab Activity : 402.8 TL - Timing Layer (general risks) (2)

Risk Rank : 2 (Medium) (1)						
RT-402-8-91-D	TL - Shortfall in Timing Layer scientific labor	30 %	0 -- 0 -- 611 k$	0 months	61	0.0
Risk Rank : 1 (Low) (1)						
RT-402-8-90-D	TL - Key Timing Layer personnel need to be replaced	25 %	45 -- 135 -- 261 k$	0 -- 0 -- 3 months	37	0.3

RI-ID	Title	Probability	Cost Impact	Schedule Impact	P * Impact (k$)	P * Impact (months)
WBS / Ops Lab Activity : 402.8 TL - Timing Layer (general risks) (2)						
WBS / Ops Lab Activity : 402.8.3 BTL - Barrel Timing Layer (14)						
WBS / Ops Lab Activity : 402.8.4 ETL - Endcap Timing Layer (10)						
Risk Rank : 3 (High) (1)						
RT-402-8-01-D	ETL - Additional FE ASIC prototype cycle is required	40 %	500 -- 600 -- 700 k$	4 -- 5 -- 6 months	240	2.0
Risk Rank : 2 (Medium) (5)						
RT-402-8-03-D	ETL - FE ASIC does not meet specs - needs another pre-prod run	10 %	874 -- 930 -- 986 k$	6 -- 7.5 -- 9 months	93	0.8
RT-402-8-55-D	ETL - Schedule delay in submitting ETROC2	30 %	55 -- 110 -- 165 k$	2 -- 4 -- 6 months	33	1.2
RT-402-8-02-D	ETL - ETL module facility unavailable	50 %	20 k$	2 months	10	1.0
RT-402-8-10-D	ETL - Sensor quality problem during production	15 %	28 -- 52 -- 109 k$	2 -- 3 -- 6 months	9	0.6
RO-402-8-01-D	ETL - Use AltiROC	10 %	-720 k$	-8 months	-72	-0.8
Risk Rank : 1 (Low) (4)						
RT-402-8-54-D	ETL - Schedule delay in submitting ETROC3	20 %	27.5 -- 55 -- 82.5 k$	1 -- 2 -- 3 months	11	0.4
RT-402-8-53-D	ETL - Integration facility at CERN runs out of components	25 %	21 k$	3 months	5	0.8
RT-402-8-31-D	ETL - Storage-related degradation of LGADs	10 %	18 k$	3 months	2	0.3
RT-402-8-51-D	ETL - Problem with vendor provision of module components	5 %	0 -- 15 -- 30 k$	1 -- 2 -- 3 months	1	0.1

Summary of ETL ASIC (ETROC)

- A strong team making rapid technical progress
  - ASIC specification extensively studied and fully developed
  - ETROC0: Front-end design with good performance
  - ETROC1: submitted on schedule in Aug 2019
- R&D achieved
  - Critical front-end design prototyped
  - Clock tree and waveform sampler designs advanced
- R&D needed to be done before production
  - Continue to validate/improve the front-end design with ETROC0&1

Concluding remark: rapid progress made since summer 2018, with a strong team on the way for ETROC production Q4 2022