B06 - 402.4.5.1.2
CE – Silicon Module Motherboards
Nadja Strobbe (University of Minnesota) L4 Manager
HL LHC CMS CD-1 Review
October 23, 2019
Outline

- Technical Aspects of CE — Silicon Module Motherboards
  - Conceptual Design
  - Scope and U.S Deliverables
  - Progress since June 2018 IPR
  - QA/QC

- Managerial aspects of CE — Silicon Module Motherboards
  - Cost, Schedule, and Risks

- Summary
Who am I?

- **Nadja Strobbe**: L4 Manager for CE – Silicon Module Motherboards (402.4.5.1.2)
  - Assistant Professor of Physics at University of Minnesota
  - **Detector experience**: Phase 1 Upgrade of CMS HCAL
    - Led QC of production HB on-detector readout (QIE) boards (2018)
    - Coordinate HE/HB test beam at CERN (2017)
    - Characterization and QC of 45k QIE ASICs for HF, HE, HB (2016-2017)
    - Coordinate full system radiation tests for HE (2015-2016)
  - **Physics: Searches for new physics**
    - SUSY Analyses Combination Coordinator (2018-2019)
    - L3 Convener of CMS SUSY MC group (2015)

- **Other crucial personnel for this area**
  - **Erich Frahm (UMN)**: senior electrical engineer
    - Designer of uHTR card for Phase 1 Upgrade, Test beam read-out systems for CE 2018 Test beam
  - **Paul Rubinov (FNAL)**: senior electrical engineer
    - Front end electronics Group Leader at FNAL (until 2017), Design of front-end electronics for several projects, including Minerva, Central Fiber Tracker in DZero, and more
Conceptual Design
### Purpose of the Si Motherboards
- Host the concentrator ASIC (ECON)
- Provide connection between the Silicon Modules and the off-detector DAQ, trigger, and control electronics (via lpGBT link)

### Important constraints
- Very limited physical space vertically (minimize air gap between calorimeter absorbers)
  - Use low-profile connectors
- Radiation tolerance
  - Especially relevant for optical driver (VTRX+), which cannot be in the innermost section of the cassette
- Support transfer of required data volume, i.e. #elinks, for good physics performance
Motherboards implemented as “engine+wagons” model

**Engine:**
- Hosts the lpGBT and VTRX+ optical components
- Small and complex board, with fine-pitch components
- Only 2-3 variants

**Wagon:**
- Up to 2 wagons per engine, spanning up to 3 modules each
- Hosts ECONs and slow control chip (GBT-SCA)
- Multiple (15+) designs to handle geometric complexity between and within layers
- Large, but simple board
• Data links
  • Modules send TRIG/DAQ data to ECON: 12 inputs per ECON at 1.28 Gbps
  • ECON concentrates: up to 14 elinks from ECON to lpGBTs at 1.28 Gbps
    • depending on data volume from given module
  • lpGBT takes up to 7 inputs, and has one data output link at 10.24 Gbps
  • Engine contains:
    1-2 DAQ lpGBT, 2-4 TRIG lpGBT, 1-2 VTRX+
    • depending on layer and location within layer
    • 1 VTRX+ takes 1-3 TRIG and 1 DAQ link

• Detailed accounting of elinks complete
  • Propagated to connector pin count and pin assignments
Fast and Slow control requirements

- Both sets of signals sent to lpGBT via 2.56 Gbps link (via VTRX+)
- Fast clock distributed via lpGBT on engine to ECON on wagon and HGCROC on module
- Slow control distributed via lpGBT on engine to the GBT-SCA on wagon
  - I2C to ECON and HGCROC
  - Temperature measurements
  - Voltage measurements, e.g. for sensor bias, DC/DC supply voltage
  - Enable, reset, error signals

Necessary signals all identified and accounted for in connector pin-outs
- Mechanical checks
  - Successful alignment of 3 connectors during/after temperature cycles

- Studies of signal transmission
  - Shows successful transmission over long distances
R&D Achieved

- First version of Engine designed and produced, including low-profile flex connectors
- Details of Engine+Wagon design in development
  - Minimizing number of different wagon designs by taking advantage of symmetries between detector layers
  - Current estimate of 3085 engines and 6170 wagons for CE-H
Produce fully functional prototype 1, which allows for cost estimate based on quotes ahead of CD-2

- Complete engine design
- At least one complete wagon design
  - using FPGA instead of ECON
  - Can extrapolate cost to other wagon designs
- Will be part of Major System Prototype 1

Second prototype

- Assemble full cassette
- Include multiple wagon designs
- Validate final design including ECON

Note: Engineers have experience with scripting for PCB design tools: improved reliability and reduced engineering time
Quality Assurance and Quality Control

- **QA**
  - Prototyping: build and evaluate prototypes for all boards
  - Minimize complexity of large boards, especially those that come in a # of variations

- **QC**
  - Engine: Crucial component, will feed signals into each board and read them out to verify proper functionality
  - Wagon: mainly checking continuity of signals through the board and its connectors
    - Evaluating trade-off between doing visual inspection and relying on vendor for PCB check ⇔ using a fixture to test continuity and risk breaking the low-profile connectors
  - Careful tracking of all boards using database and machine-readable ID
    - Allows for follow-up checks in case a problem is identified, e.g. during cassette assembly
  - Reviewing balance of paid & unpaid labor before CD-2
    - Good experience with undergraduates in the past
Cost and Schedule
## Cost

<table>
<thead>
<tr>
<th>WBS</th>
<th>Direct M&amp;S ($)</th>
<th>Labor (Hours)</th>
<th>FTE</th>
<th>Direct + Indirect + Esc. ($)</th>
<th>Estimate Uncertainty ($)</th>
<th>Total Cost ($)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DOE-CD1-402.4 402.4 CE - Calorimeter Endcap</td>
<td>21,051,786</td>
<td>332579</td>
<td>188.11</td>
<td>40,672,474</td>
<td>10,143,585</td>
<td>50,816,059</td>
</tr>
<tr>
<td>(at DOE CD1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DOE-CD1-402.4.5.1.2 CE - Silicon Motherboards</td>
<td>2,245,755</td>
<td>7688</td>
<td>4.35</td>
<td>3,600,258</td>
<td>1,296,667</td>
<td>4,896,926</td>
</tr>
</tbody>
</table>

402.4.5.1.2-CE-Base Budget Profile (DOE)-Resource Type

BAC = $3.60M (AY$)

- **Direct M&S breakdown**
  - 40%: Components from CERN (lpGBT, VTRX+, GBT-SCA)
  - 50%: PCB and assembly for production boards
### RT-402-4-23-D CE - Si Motherboard complexity is much higher than expected

- **Risk added after 2018 review**
  - **Was at higher level during Feb Director’s Review**
  - **Now risk has been reduced because of work done in defining and simplifying the design since then**
  - **Expect to retire the risk before CD-2**
Cassette construction is done per sector

Need steady supply of engines and each variety of wagon
- Prototype 1 completed by April 2020
- Prototype 2 completed by March 2021
  - With prototype ECON
- Production
  - Design finalized by September 2021
  - First batch of motherboards to be assembled in Dec 2021
    - First batch of ECONs available in Nov 2021
  - First batch tested by Feb 2022, ahead of cassette assembly which starts in June 2022
  - Flexibility in adjusting engine/wagon assembly & testing schedule to mitigate effect of late arrival of parts, e.g. ECON
Many advances in the Silicon Module Motherboard area since previous review

- Completed thermal mockup study
- Settled on Engine+Wagons concept
- Designed and produced first engine prototype
- Overall detailed concepts, including services, have been significantly advanced

Significant work left in this area, but we are on track to be ready for CD-2 and CD-3
- Backup
Risks

RT-402-4-15-D CE - Motherboard and interface board fabrication failure

| Risk Rank: | 1 (Low) | Scores: Probability: 2 (L) ; Cost: 1 (L) ; Schedule: 1 (L) | Risk Status: | Open |
| Summary: | If larger than expected failure rate is identified during motherboard and interface board production then the cassette assembly will slow down and may jeopardize the delivery of cassettes to CMS on time. |
| Risk Type: | Threat |
| WBS: | 402.4 CE - Calorimeter Endcap |
| Probability (P): | 10% |
| Risk Area: | Technical Risk / Quality |
| Cost Impact: | Schedule Impact: |
| PDF | 2-point - flat range | PDF | 1-point - single value |
| Minimum | 73 k$ | Minimum | N/A |
| Most likely | N/A | Most likely | 3.0 months |
| Maximum | 193 k$ | Maximum | N/A |
| Mean | 133.0 k$ | Mean | 3 months |
| P * <Impact> | 13.0 k$ | P * <Impact> | 0.3 months |
| Basis of Estimate: | The cost impact (10 - 130k$) is based on the assumption that at maximum 10% of the motherboards for the whole detector have to be produced due to Motherboard failures. The base cost includes an additional 10% spare motherboards on top of that needed for the detector. These spares partly cover more minor failures and yield of individual components, or motherboard variants, and may not cover a more significant failure covered by this risk where the production motherboards are done in two batches. We assume a failure scenario where 10% of the motherboards would need to be produced and assembled to ensure that we have sufficient spares to cover lost motherboards of any of the variants by the end of the production. The duration impact (3 months) is based on the assumption that another vendor might be needed to be qualified to take over the production, or some specific variants have to be made again beyond what was ordered for spares. The L3 burn rate due to the delay of downstream activities is $21k/month [CMS-doc-13481]. Min cost = $10k + 3 months * $21k burn rate = $73k. Max cost = $130k + 3 months * $21k burn rate = $193k. |
| Cause or Trigger: | |
| Impacted Activities: | |
| Start date: | 1-Jan-2021 | End date: | 12-Dec-2023 |
| Risk Mitigations: | Thoroughly qualify the design through the cassette prototype program and, as appropriate, focused mockups. Qualify several vendors for board fabrication such that they can pickup production if one vendor fails. Require a rigorous QA/QC program by the vendor. Begin motherboard and interface board production in advance of cassette assembly to ensure a buffer of components so that interruption of the supply does not affect cassette production. Design cassette assembly sites to allow rework without interrupting production flow. |
| Risk Responses: | Depending on the schedule and which motherboard variants need to be replaced we may need to order a new round of motherboards and assembly. If other delays or this delay causes this task to be on the critical path we will accelerate the cassette production and testing. The possibility of needing to accelerate the cassette production is covered by a separate risk. |
| More details: | CMS-doc-13481 |